SONY®

VIDEOCORDER

BVH-3000PS
BVH-3100PS

BVH-3000PS

BVH-3100PS

BVH-3000PS/3100PS with this optional part installed: side panel kit.

MAINTENANCE MANUAL

Volume 1 1st Edition (Revised 5)

BVH-3000PS Serial No. 10001 and Higher
BVH-3100PS Serial No. 10001 and Higher

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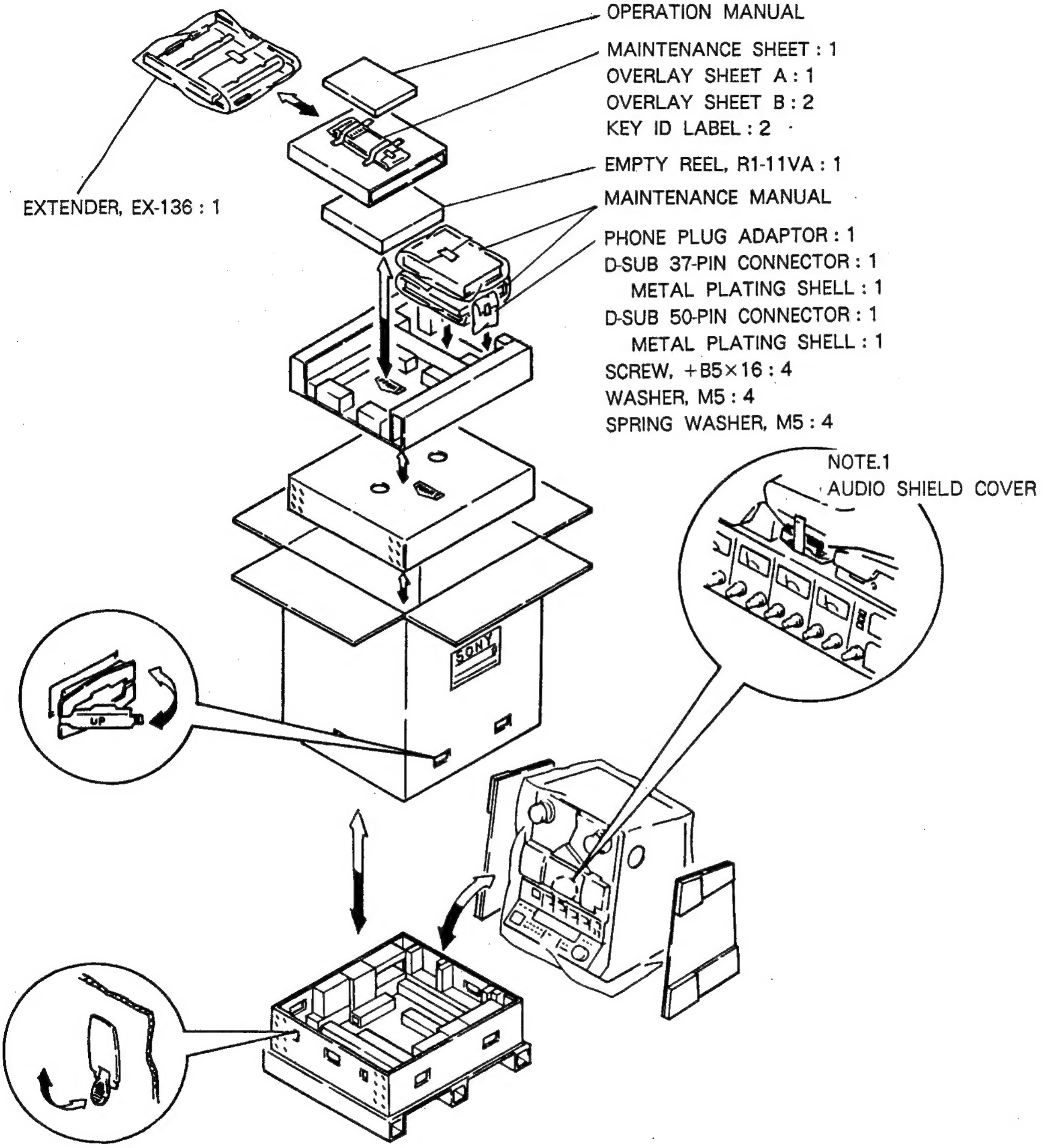
Volume 2

SECTION 1
INSTALLATION

1-1. UNPACKING AND REPACKING



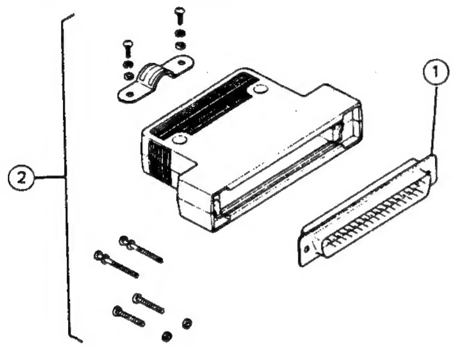
Note 1 : Before the unit leaves the factory, the audio shield cover is taped to prevent it from dropping out. Before using the unit, remove this tape.

1-2. ACCESSORIES

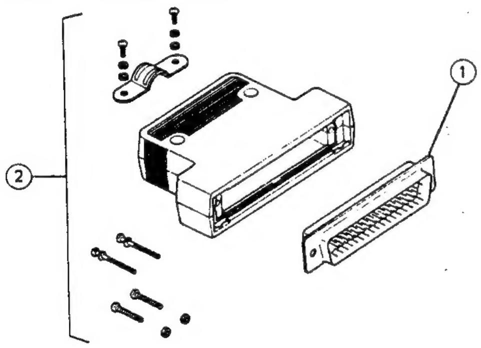
1-2-1. Accessories Supplied

11.75" Empty Reel Sony R1-11VA : 1
Empty reel for automatic tape threading.

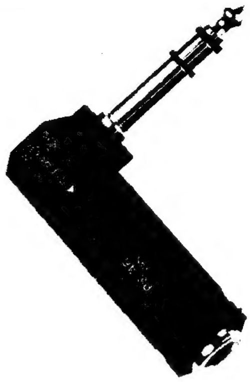
D-sub 37-pin Connector (Male)
A plug for [MONITOR SELECT] connector and consists of the following parts. Used for controlling each [AUDIO MONITOR], [PICTURE MONITOR], and [WAVEFORM MONITOR] selector remotely.
①D-sub 37-pin Connector (Male) : 1
②Metal Plating Shell : 1



D-sub 50-pin Connector (Male)
A plug for [REMOTE-3] connector and consists of the following parts. Used for connecting a parallel type remote controller to the VTR.
①D-sub 50-pin Connector (Male) : 1
②Metal Plating Shell : 1



Phone Plug Adapter : 1
If headset is connected through this adapter, the plug will project less.



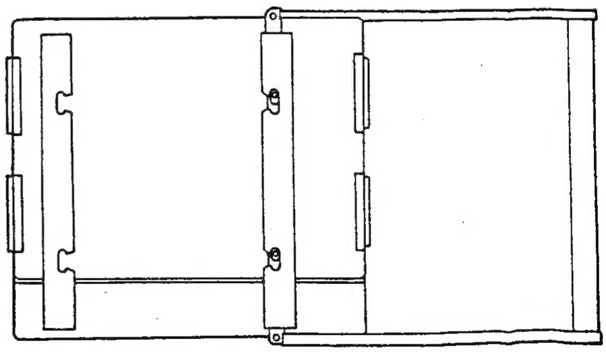
Screws B5×16 : 4
Washers M5 : 4
Spring Washers M5 : 4
Used when VTR is mounted in the Sony Console Unit or 19" rack.

Maintenance Sheet : 1
Used for recording the history of the upper drum replacement or maintenance. Usually, stick this label inside the bottom lid. When mounting the VTR in a console unit, stick it on the flap door. When mounting the VTR in a rack, stick it to the appropriate place according as necessity.

Operation Manual : 1 (for U/C), 3 (for PS)
English version is provided with the USA/Canadian model. English version, French version and German version are provided with the European model.

Maintenance Manual : 2
Vol-1 and Vol-2 are provided with the unit.

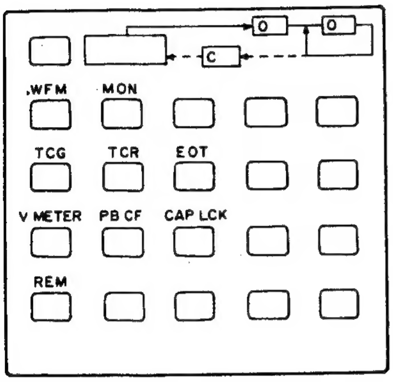
Extender EX-136 : 1
Used for checking and repairing the plug-in circuit board in the card rack.



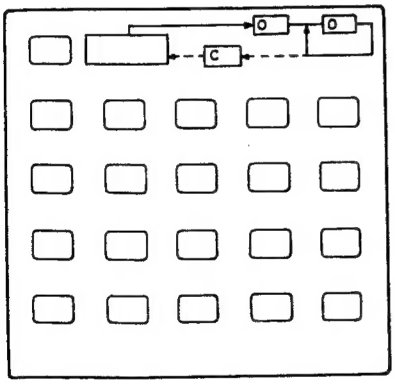
Overlay sheet A : 1
Overlay sheets B : 2
Key ID labels : 2

Overlay sheet A is for the preset menu which is assigned at the factory to numerical keys 0 to 8 of the 21 keys on the control panel.
Overlay sheets B are used when the user changes the assignment of the preset menu.
The key ID labels are the ID labels for the menu bonded to overlay sheets B.
Use the above overlay sheets by placing them over the 21 keys on the control panel.

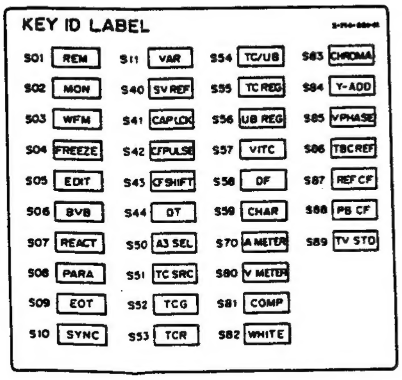
Overlay sheet A Sony Part No. 3-714-847-01



Overlay sheet B Sony Part No. 3-714-847-11

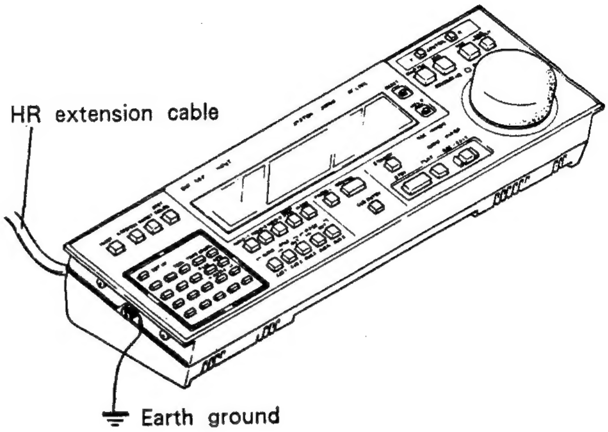


Key ID label Sony Part No. 3-714-851-01



1-2-2. Optional Accessory

HR Extension Cable Sony Part No. 1-559-524-11
This is an extension cable (10m in length) to control remotely the BVH-3000/3100 VTR using the VTR's function control panel. This cable is supplied in the same way as ordinary repair parts.
Connect a wire from the chassis of the control panel to the earth as shown below. The earth ground will prevent the static noise from causing malfunction.



1-3. POWER REQUIREMENTS

Power Line Voltage
AC 100 to 120V ±10% (for UC model)
AC 100 to 240V ±10% (for PS model)

Power Line Frequency 50/60Hz

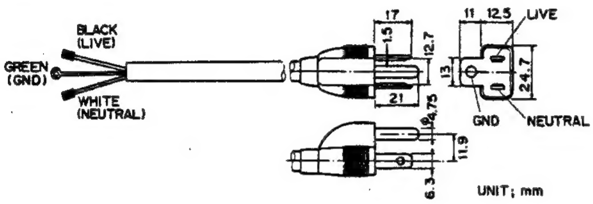
Power Consumption 500W max.

Note 1. Includes the BKH-3010 or 3050 (3020 or 3060).

Note 2. When the power switch turn to ON, approx. 10A input current for AC 100V or 6A for AC 240V will flow and the surge currents will be three or four times as much.

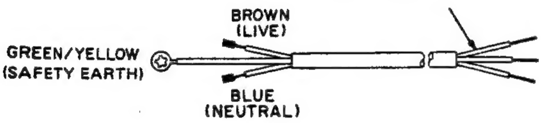
Power Cord Approx. 2.4m in length

for UC



for PS

An AC plug should be locally prepared and mounted.



1-4. INSTALLATION CONDITIONS

Operating Temperature	+5℃ to +40℃
Storage Temperature	−20℃ to +60℃
Humidity	10% to 90% (noncondensing)

Mount on a flat, stable base.

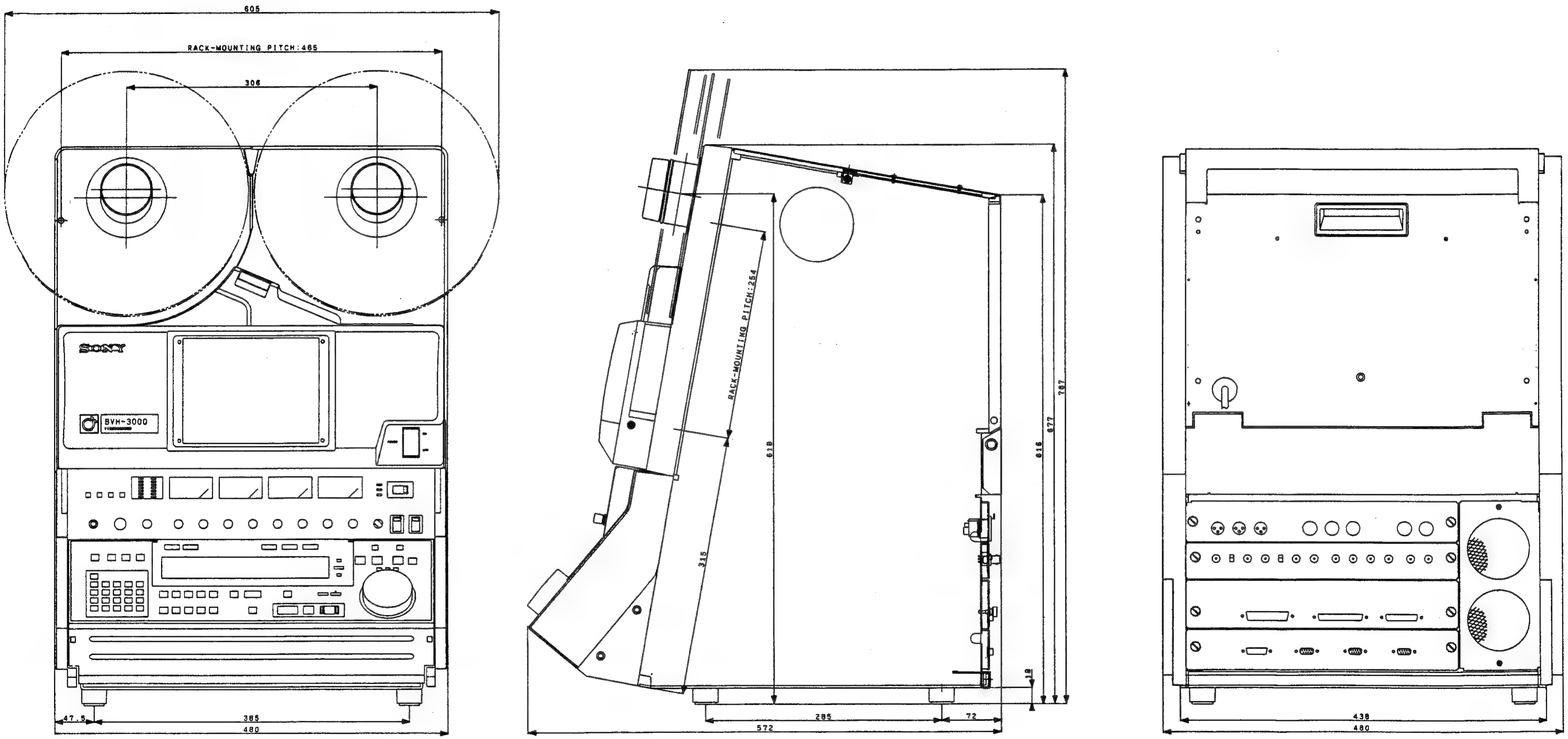
The BVH-3000/3100 total weight is approx. 72kg, including the BKH-3001 and BKH-3010 (BKH-3050, 3020 or 3060). The total weight of the SU-910A Console Unit and SUA-911 Monitor Console Unit is approx. 246kg including the BVH-3000/3100 and monitors etc.

Do not install in the following types of location.

- Places exposed directly to sun light or powerful light
- Dusty places
- Places subjected to vibration
- Places exposed to strong electric or magnetic fields

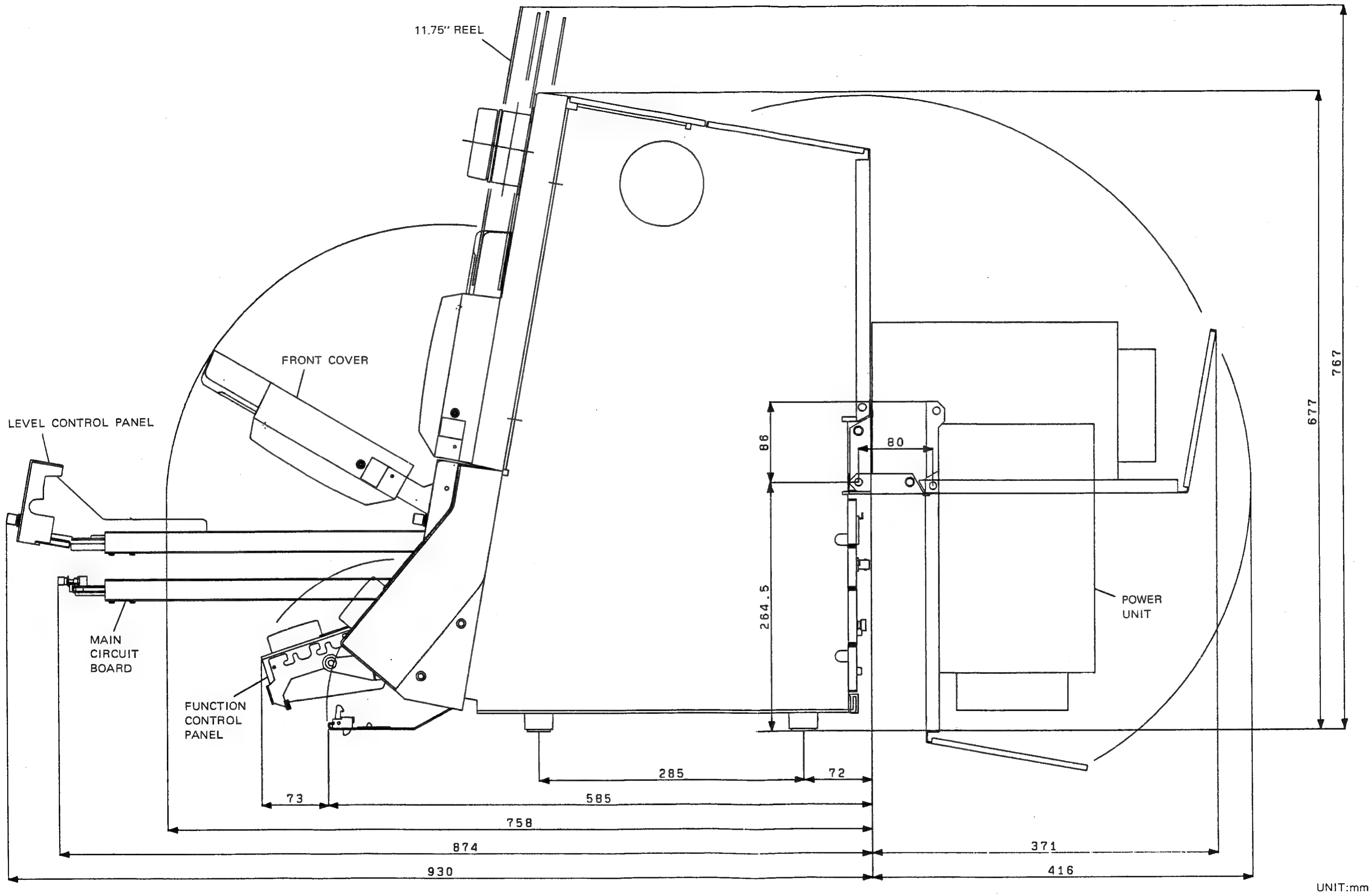
1-5. INSTALLATION SPACE

External Dimensions

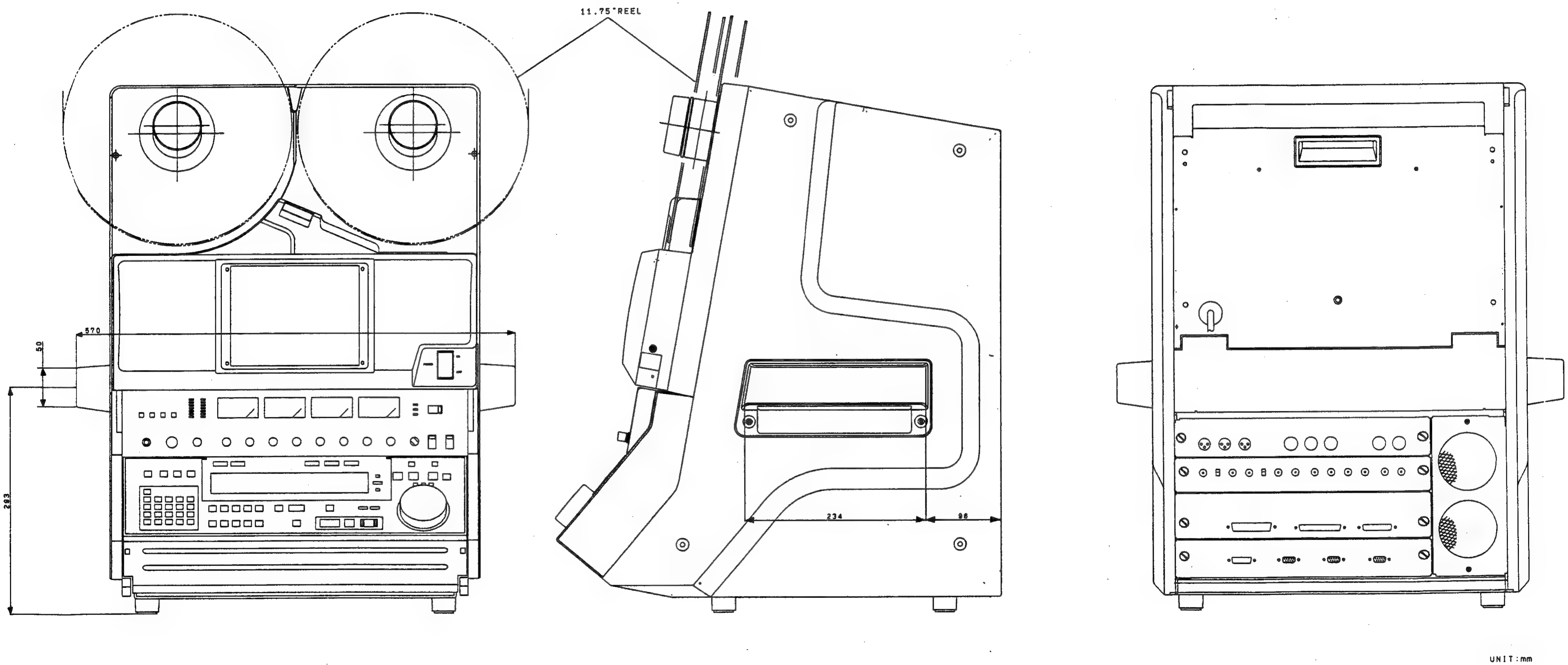


UNIT:mm

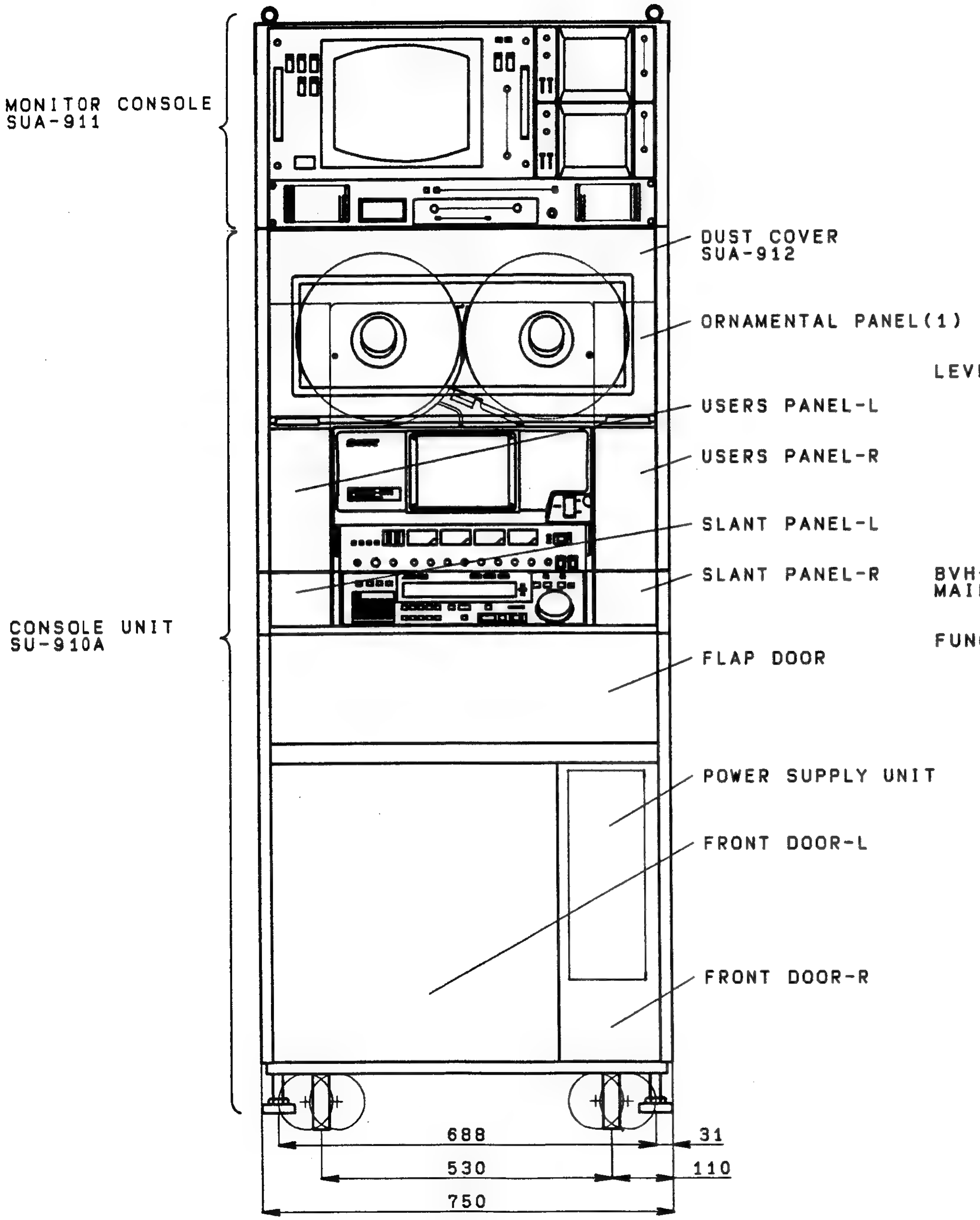
Working Space

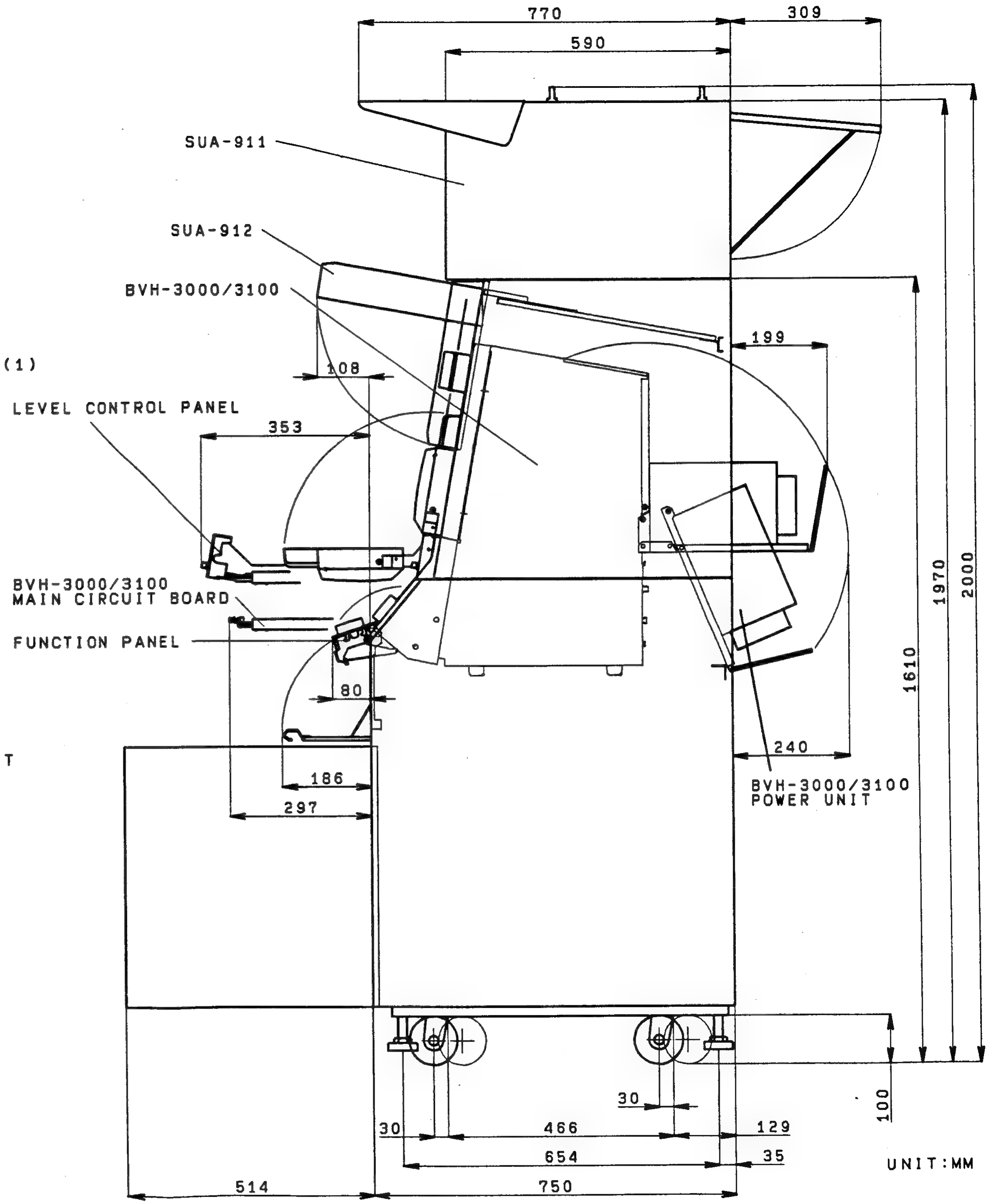


External Dimensions: When mounting BKH-3001

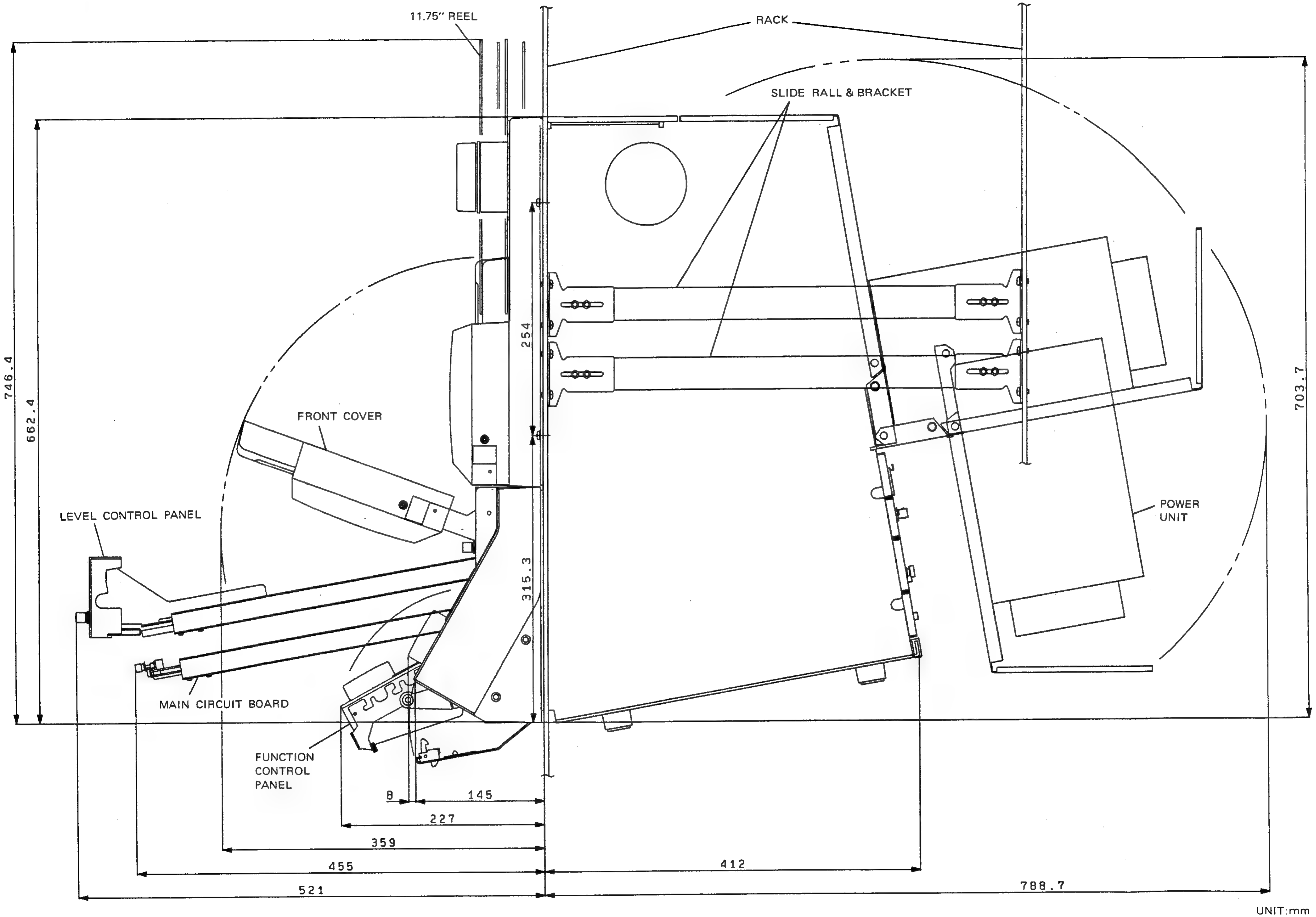


External Dimensions/Working Space: When mounting to SU-910A

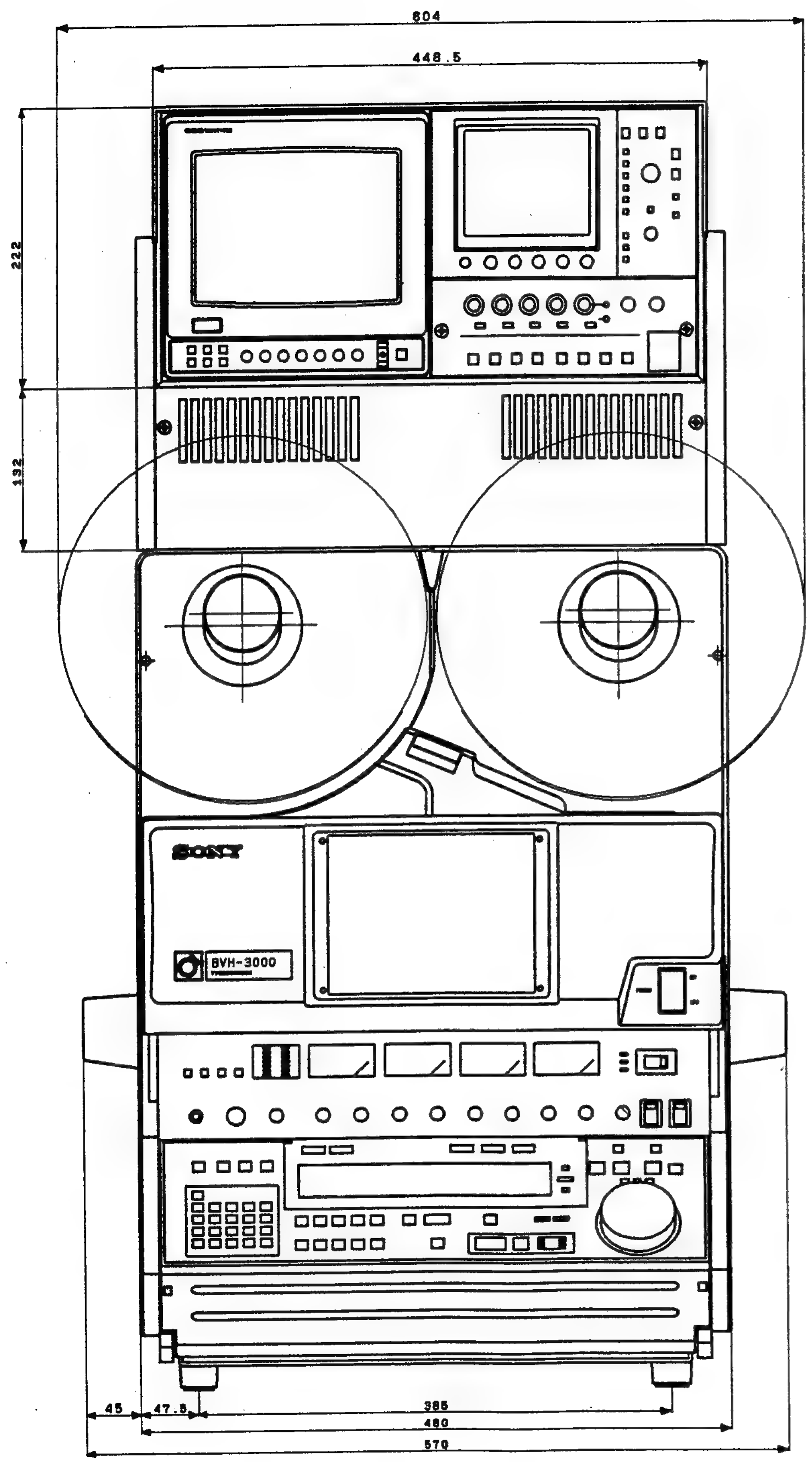


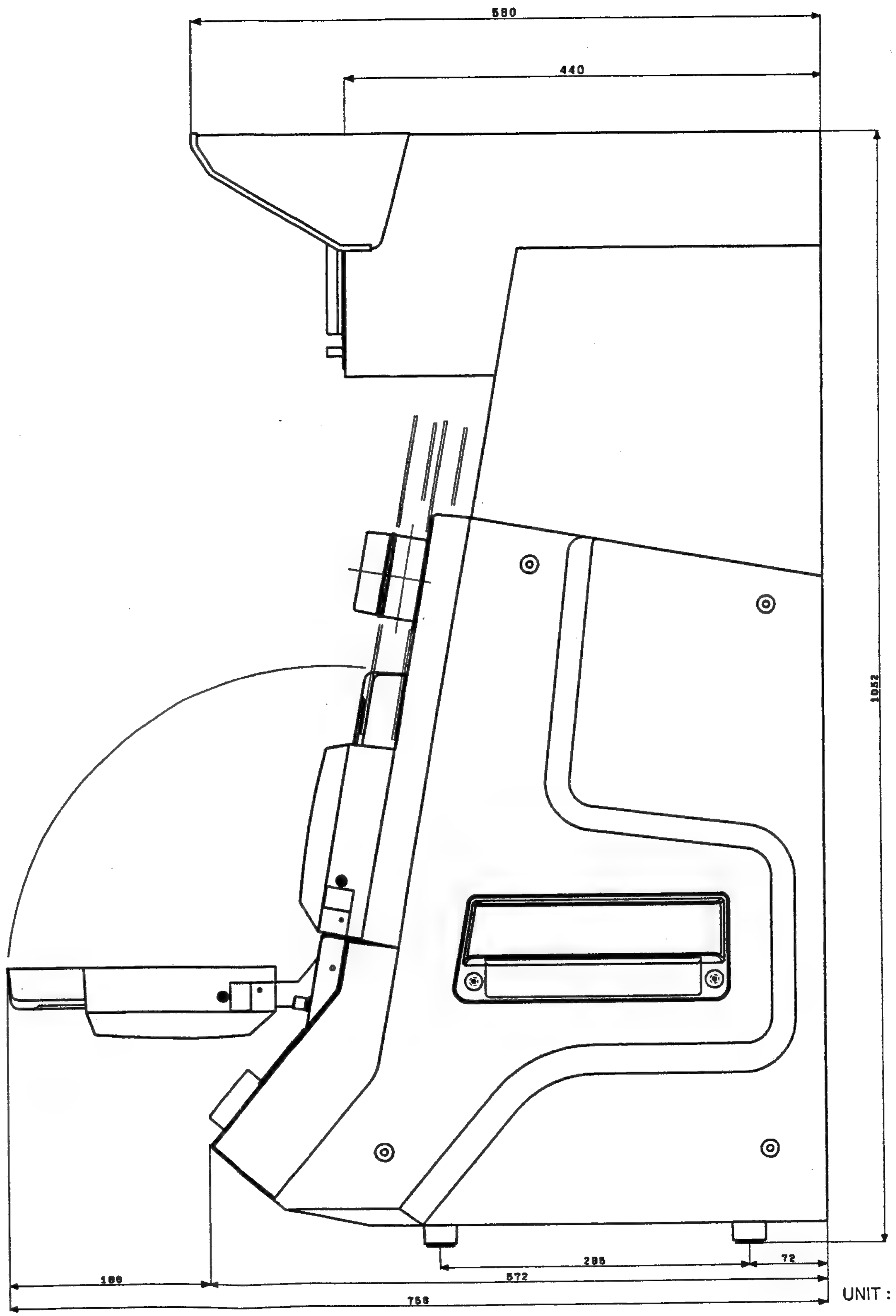


External Dimensions/Working Space: When rack-mounting



External Dimensions : When mounting SU-L200/SUA-L201





UNIT : mm

1-6. RACK MOUNTING

Prepare the following parts for rack-mounting.

Slide Rails : 2 pairs
One pair consists of two inner members and two outer members.
Manufactured by Accuride
Model 201 (20" in length)*
or Model 203 (20" in length)*

Brackets : 8
Manufactured by Accuride
#5355-2*

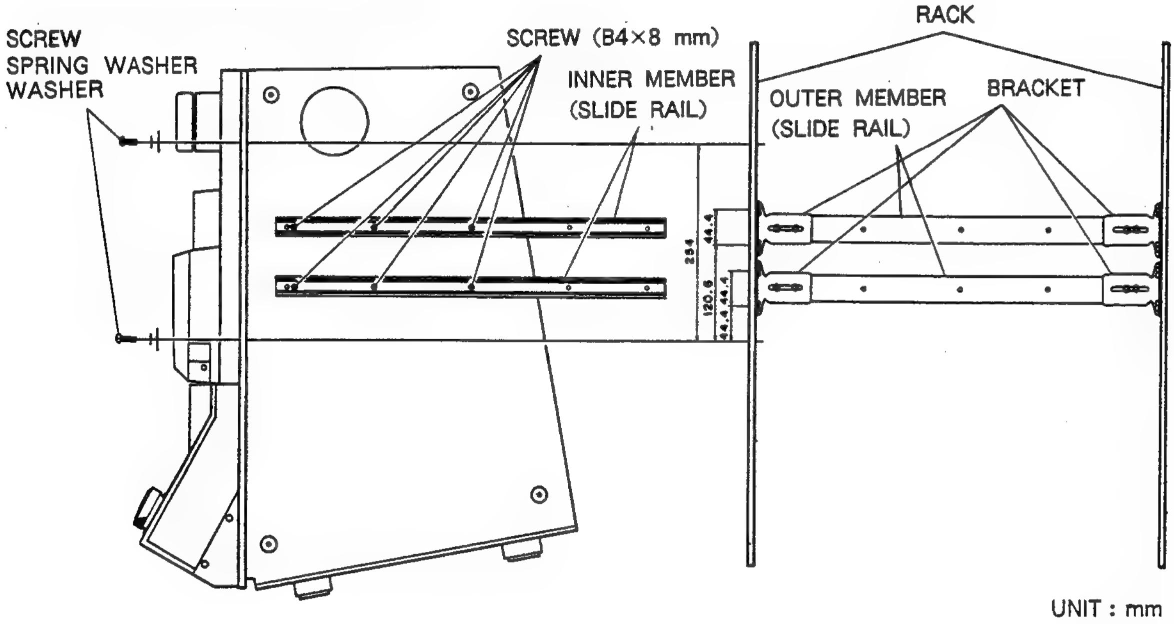
* Accuride slide rail Model 305 (20") and Bracket #5356 can be used also.

Inner Member Fixing Screws : 12
+B4×8 (Sony part No. 7-682-561-04)

VTR Fixing Screws and Washers
Screws +B 4×8 : 4
Washers M5 : 4
Spring washers M5 : 4
These are supplied to the VTR. However, if they do not fit the rack to be used, prepare appropriate parts. The diameter of the head of screws and washers must be less than 11.5mm.

Other Screws and Nuts
Be sure to use the parts recommended by the slide rail manufacturer.

Fit the slide rails and mount the VTR in the rack.



1-7. INITIAL SETTING

1-7-1. Initial Setting Menu

Initial settings are set by the menu operation. The contents of setting menu can be saved and restored by a NOVRAM (nonvolatile RAM) according to the individual need.
For details, refer to the operation manual.

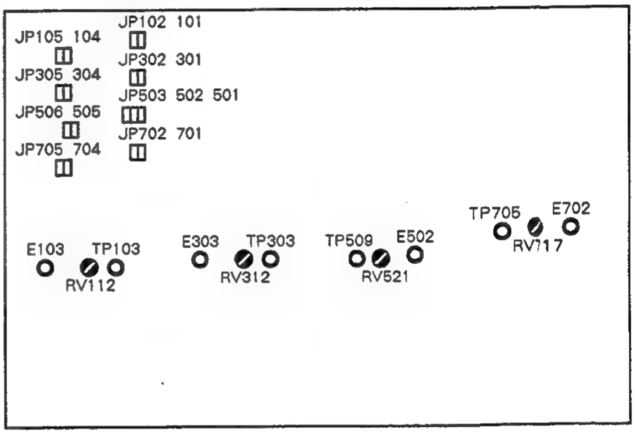
1-7-2. Altering the Input Impedance of Audio

The line input impedance of audio CH-1, 2 and 3 (and 4 for PS-A4 model) is set to 600 Ω when shipped. However, the AU-88 board remodeled as shown below makes 47k Ω, 10k Ω or 150 Ω impedance possible.

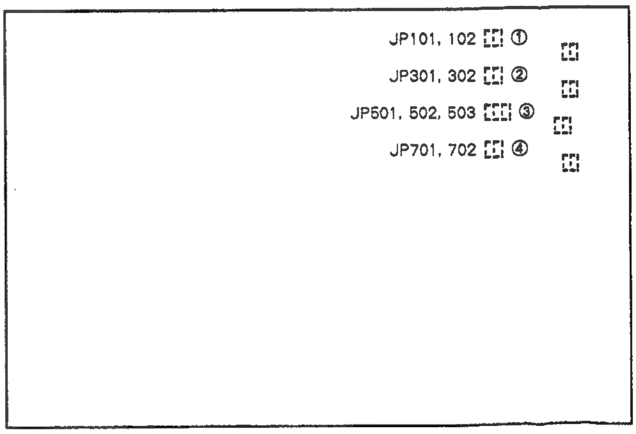
Input impedance	Jumper plug				Trace
	CH-1	CH-2	CH-3	CH-4	each CH
	JP101 /102	JP301 /302	JP501 /502 /503	JP701 /702	①, ②, ③, ④
47k Ω			JP501		⊖
10k Ω	JP101	JP301	JP502	JP701	⊖
600 Ω	JP102	JP302	JP503	JP702	⊖
150 Ω	JP102	JP302	JP503	JP702	⊕

⊖: Leave open.
⊕: Short (Solder).

AU-88 BOARD : COMPONENT SIDE



AU-88 BOARD : SOLDER SIDE



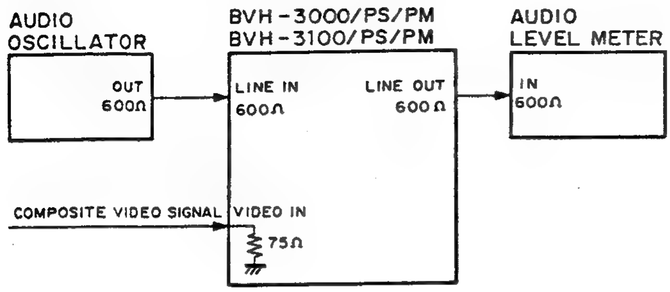
1-7-3. Altering the Reference Level of Audio Input /Output

The line input/output reference level of audio CH-1, 2 and 3 (and 4 for PS-A4 model) is set to +8dB when shipped. However, they can be altered as follows.
Altering the jumper plug settings on the AU-88 board make it possible to change the line input reference level from +8dB to −12dB.

Reference input level	Jumper plug			
	CH-1	CH-2	CH-3	CH-4
	JP104/105	JP304/305	JP505/506	JP704/705
+8dB	JP104	JP304	JP505	JP704
−12dB	JP105	JP305	JP506	JP705

And also, the following adjustments make it possible to change the line input/output reference level from +8dB to your studio level.

(1) Connect the equipment as shown below.



(2) Set the menu and switches as follows.

NR-26 board (option BKH-3080)

NORM/SETUP switch :	NORM
CH1 PB CAL/UNCAL switch :	CAL
CH2 PB CAL/UNCAL switch :	CAL
A/OFF/SR switch :	OFF

Level control panel

AUDIO LINE OUT level control :	Preset
AUDIO 1, 2, 3/4 REC level controls :	Preset
AUDIO 1, 2, 3/4 PB level controls :	Preset
REC INHIBIT switches :	OFF

Function cotrol panel

TAPE/IN key :	TAPE/EE

Menu

S50. A3 INPUT SELECT :	LINE

Also perform the following settings for the PS-A4 model :

S10. SYNC/A4 SELECT :	A4

(3) Set the VTR to the EE (STOP) mode and supply the 1kHz signal with the reference level at your studio to the AUDIO LINE INPUT connector.

(4) Line input level setting
Adjust the REC level preset controls, which are located on the bottom of the level control panel, so that the level at each of the following points is 77.46mVrms.

CH-1 : TP103-E103/AU-88
CH-2 : TP303-E303/AU-88
CH-3 : TP509-E502/AU-88
CH-4 : TP705-E702/AU-88

(5) Line output level setting
Adjust the controls shown below so that the line output level is equal to your studio reference level.

CH-1 : RV112/AU-88
CH-2 : RV312/AU-88
CH-3 : RV521/AU-88
CH-4 : RV717/AU-88

1-8. I/O INTERFACE

1-8-1. Matching Connectors and Cables

BVH-3000/3100 Connectors Used for	Type	Matching Connectors Cables Type	Sony Part No.
REMOTE connector panel			
REMOTE-1	D-sub, 15-pin, Female	CVK-1 Cable Assy	1-560-409-00 (Note 1)
TBC	D-sub, 15-pin, Male	RM Flat Cable Assy	1-933-305-00 (Note 2)
REMOTE-2A IN, OUT	D-sub, 9-pin, Female	D-sub, 9-pin, Male	1-508-158-XX
REMOTE-2B IN/OUT		RCC-5G Cable Assy	Optional Accessory (Note 3)
		RCC-10G Cable Assy	Optional Accessory (Note 3)
		RCC-30G Cable Assy	Optional Accessory (Note 3)
REMOTE-3	D-sub, 50-pin, Female	D-sub, 50-pin, Male	1-565-516-11 (Note 4)
MONITOR SELECT	D-sub, 37-pin, Female	D-sub, 37-pin, Male	1-565-515-11 (Note 5)
		MS Flat Cable Assy	1-933-306-00 (Note 6)
VIDEO Connector Panel			
	BNC	BNC	
AUDIO Connector Panel			
AUDIO-1, 2, 3, 4 INPUT	XLR, 3-pin, Female	XLR, 3-pin, Male	1-508-084-00 (Note 7)
AUDIO-1, 2, 3, 4 OUTPUT	XLR, 3-pin, Male	XLR, 3-pin, Female	1-508-083-00 (Note 8)
(Note : AUDIO-4 is for PS-A4 model only.)			
Level Control Panel			
HEADPHONES	6 φ Phone Jack	6 φ Phone Plug	

(Note 1) CVK-1 Cable Assy 1-556-409-00
One cable (40cm in length) is supplied to BKH-2016 Sony CCJ Converter.

(Note 2) RM Flat Cable Assy 1-933-305-00
One cable (2m in length) is supplied to BK-2006 or 2007 Sony TBC Remote Control Unit and SUA-911 Sony Monitor Console.

(Note 3) RCC-5G/10G/30G Cable Assy
Used for connecting the two BVH-3000/3100 or connecting the BVH-2XXX, BVU-8XX or BVW-XX to the BVH-3000/3100. The length of the cables are 5m, 10m and 30m.
The BVU-8XX, BVW-XX has the RCC-5G as an accessory.

(Note 4) D-sub 50-pin Male Connector 1-565-516-11
(Note 5) D-sub 37-pin Male Connector 1-565-515-11
Each one connector is supplied to BVH-3000/3100.

(Note 6) MS Flat Cable Assy 1-933-306-00
SUA-911 Sony Monitor Console is equipped with one cable, 1.85m in length.

(Note 7) XLR 3-pin Male Connector 1-508-084-00
Equivalent to CANNON XLR-3-12C.

(Note 8) XLR 3-pin Female Connector 1-508-083-00
Equivalent to CANNON XLR-3-11C.

SECTION 2
SERVICE INFORMATION

2-1. PRINCIPAL COMPONENTS LOCATION

TAPE TRANSPORT: HEAD, MOTOR SENSOR, SOLENOID etc.

H1 HEAD, FULL ERASE (NTSC)
HEAD, V/S ERASE (PS)
H2 HEAD, AUDIO/CTL ERASE
H3 HEAD, AUDIO/CTL R/P
H4 HEAD, AUDIO MONITOR

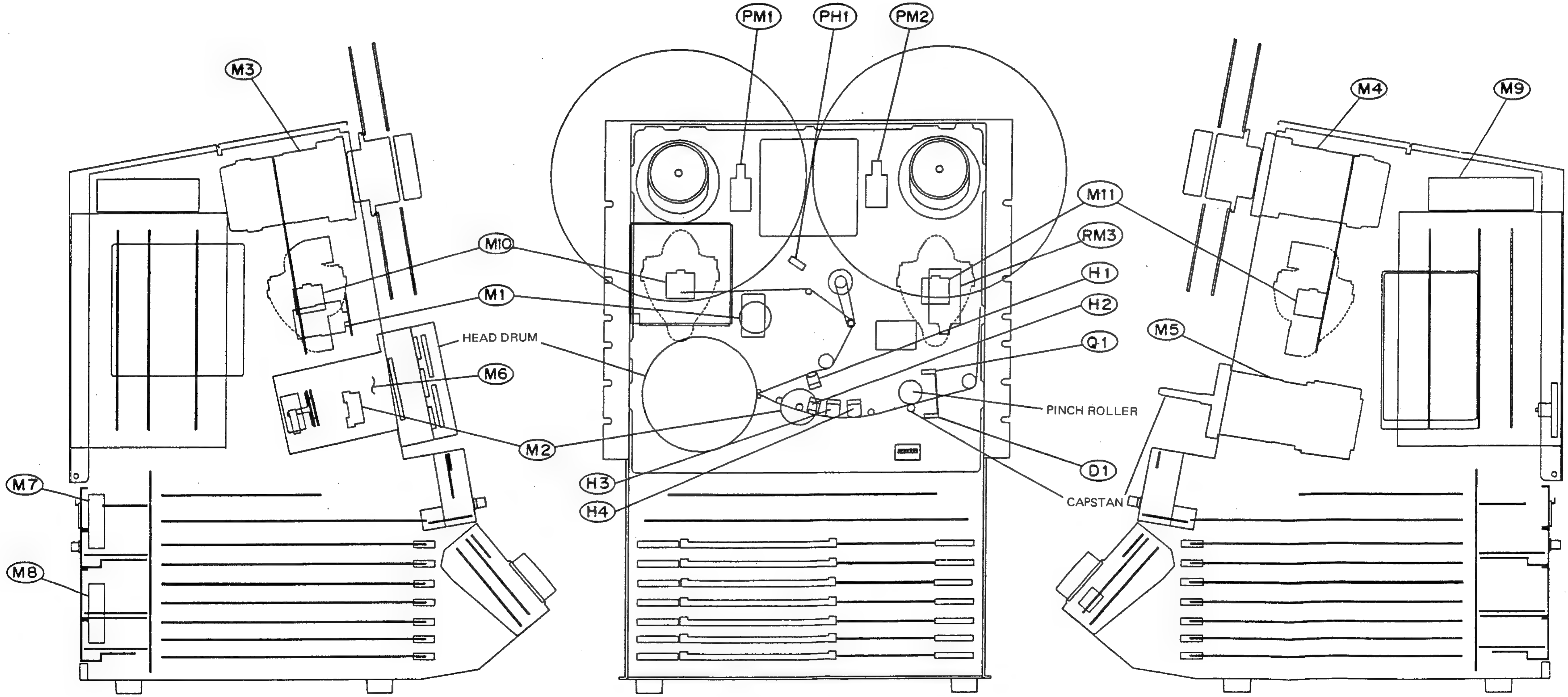
M1 MOTOR, THREADING
M2 MOTOR, IP (IMPEDANCE ROLLER)
M3 MOTOR, SUPPLY REEL
M4 MOTOR, TAKE-UP REEL
M5 MOTOR, CAPSTAN
M6 MOTOR, DRUM

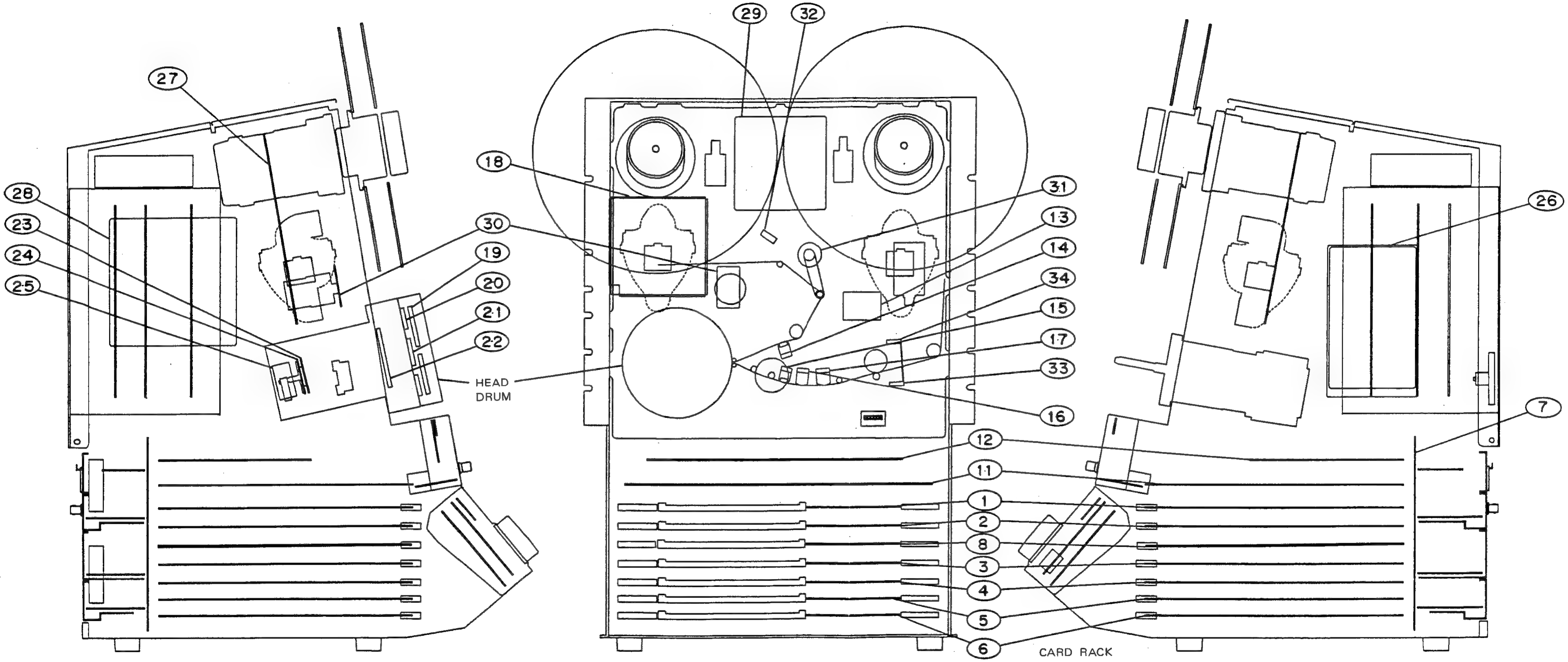
M7 MOTOR, FAN
M8 MOTOR, FAN
M9 MOTOR, FAN
M10 MOTOR, S-SIDE BLOWER
M11 MOTOR, T-SIDE BLOWER

PH1 PHOTOINTERRUPTER, FRONT COVER SENSOR

PM1 SOLENOID, SUPPLY REEL BRAKE
PM2 SOLENOID, TAKE-UP REEL BRAKE
PM3 SOLENOID, PINCH ROLLER

D1 LED, TAPE SENSOR
Q1 PHOTO TRANSISTOR, TAPE SENSOR




27
28
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21
22
HEAD DRUM
18
29
32
31
13
14
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15
17
33
16
26
7
12
11
1
2
8
3
4
5
6
CARD RACK

CARD RACK

1	VO−16 BOARD :	VIDEO MODULATOR/DEMODULATOR
2	CK−26/27 BOARD :	TBC (AD CONVERTER, CLOCK)
3	PR BOARD :	TBC (DA CONVERTER, PROCESSOR) : BKH−3010/3020/3050/3060
4	RD−6/7 BOARD :	REFERENCE SIGNAL GENERATOR, DT CONTROL
5	SY−103 BOARD :	SYSTEM CONTROL, TIME CODE
6	SV−90 BOARD :	SERVO, LOGIC CONTROL
7	MB−140 BOARD :	MOTHER BOARD
8	NR−26 BOARD :	AUDIO PROCESSOR : BKH−3080

TAPE TRANSPORT

11	AU−88 BOARD :	AUDIO REC/PB AMPLIFIER
12	AP−15 BOARD :	AUDIO PREAMPLIFIER, BIAS, ERASE
13	BC−12 BOARD :	AUDIO BIAS LEVEL ADJ.
14	FEH−1 BOARD :	FULL ERASE HEAD (NTSC)
14	HD−06 BOARD :	VIDEO/SYNC ERASE HEAD (PS)
15	CEH−2 BOARD :	AUDIO/CTL ERASE HEAD
16	HD−07 BOARD :	AUDIO/CTL R/P HEAD
17	HD−07 BOARD :	AUDIO MONITOR HEAD
18	RP−32 BOARD :	VIDEO/SYNC R/P AMPLIFIER
19	DR−13 BOARD :	VIDEO/SYNC PB AMPLIFIER
20	DR−14 BOARD :	ROTARY HEAD RELAYING
21	DR−15 BOARD :	ROTARY HEAD RELAYING
22	DR−16 BOARD :	ROTARY HEAD RELAYING
23	SL−07 BOARD :	SLIP RING RELAYING
24	SL−08 BOARD :	SLIP RING RELAYING
25	SR−36 BOARD :	SLIP RING RELAYING
26	DD−7 BOARD :	DT DRIVE
27	RM−43 BOARD :	REEL MOTOR DRIVER
28	CD−36 BOARD :	CAPSTAN MOTOR/DRUM MOTOR DRIVER
29	DS−19 BOARD :	TTP AUX
30	MC−29 BOARD :	THREADING MOTOR
31	DE−18 BOARD :	TENSION SENSOR
32	PS−143 BOARD :	FRONT COVER SENSOR
33	PS−143 BOARD :	TAPE SENSOR (LED)
34	PS−143 BOARD :	TAPE SENSOR (PHOTO TRANSISTOR)

LEVEL CONTROL PANEL

41	VR−51 BOARD :	METER／VR
42	MS−21 BOARD :	MONITOR SELECT
43	LP−34 BOARD :	METER LAMP
44	SW−195 BOARD :	SWITCH

FUNCTION CONTROL PANEL

51	EN−55 BOARD :	ENTRY KEY
52	KY−103 BOARD :	MAIN KEY
53	KC−14 BOARD :	KEY CONTROL
54	DP−63 BOARD :	SUB KEY
55	DET−3 BOARD :	SEARCH DIAL DETECTOR

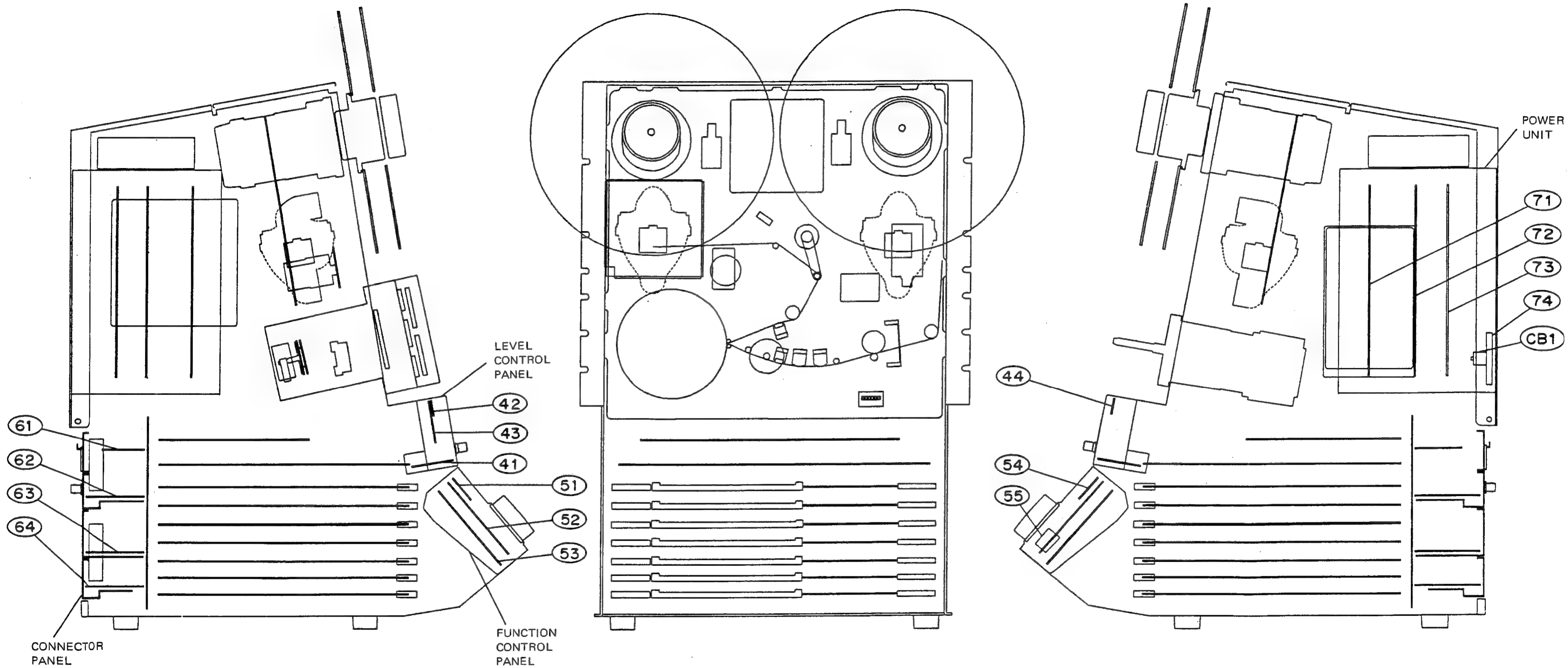
CONNECTOR PANEL

61	MA−26 BOARD :	AUDIO MONITOR AMPLIFIER
62	VS−30 BOARD :	VIDEO MONITOR
63	PA−56 BOARD :	PARALLEL REMOTE
64	SE−49 BOARD :	RS−422 INTERFACE
	SE−56 BOARD :	RS−232C INTERFACE : BKH−3002

POWER SUPPLY

71	SP−01 BOARD :	SWITCHING REGULATOR
72	SP−02 BOARD :	SWITCHING REGULATOR
73	SP−03 BOARD :	SWITCHING REGULATOR
74	AC−82 BOARD :	AC ASSY
CB1	BREAKER, 10A	

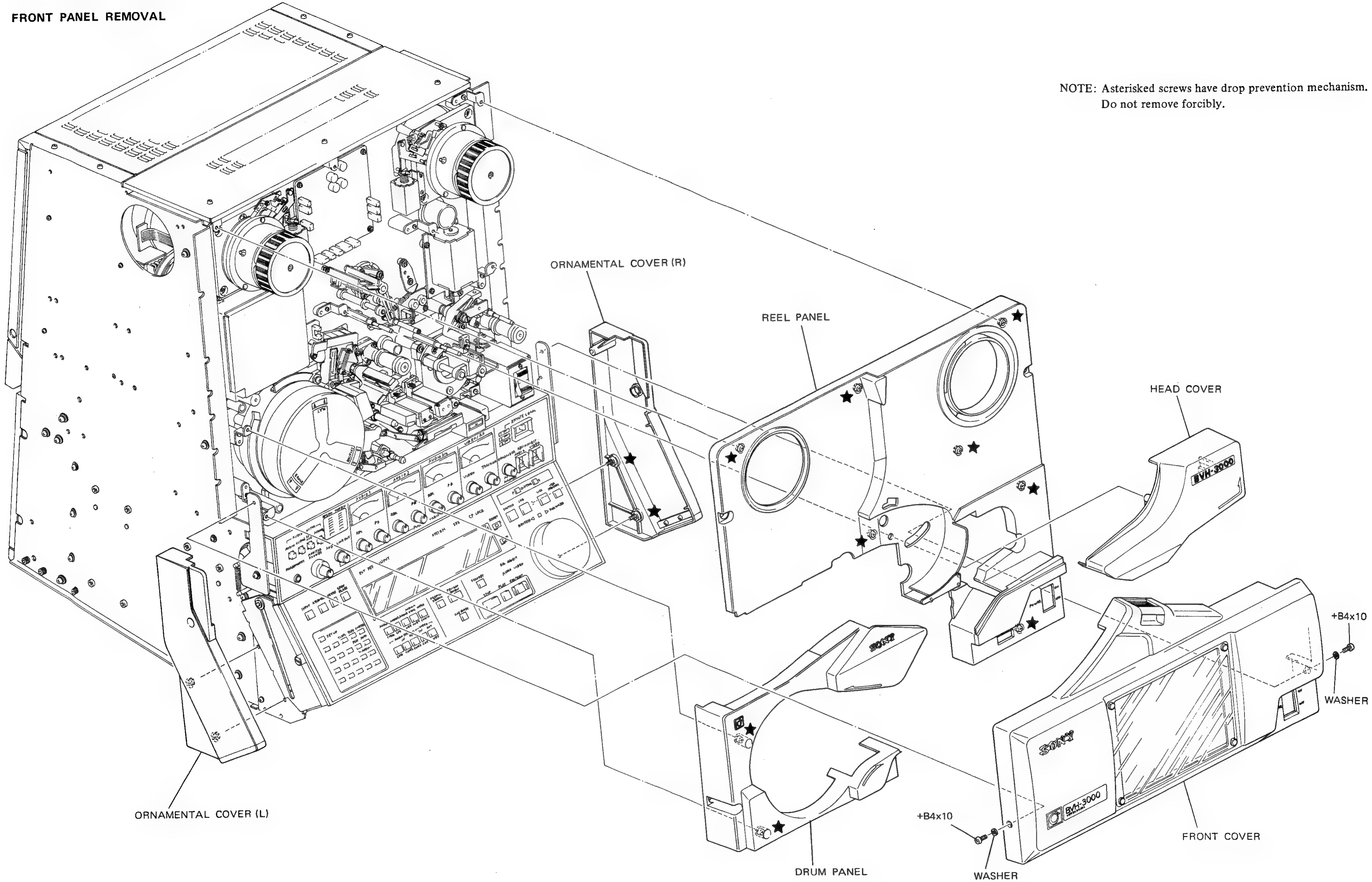
LEVEL CONTROL PANEL, FUNCTION CONTROL PANEL
CONNECTOR PANEL, POWER SUPPLY



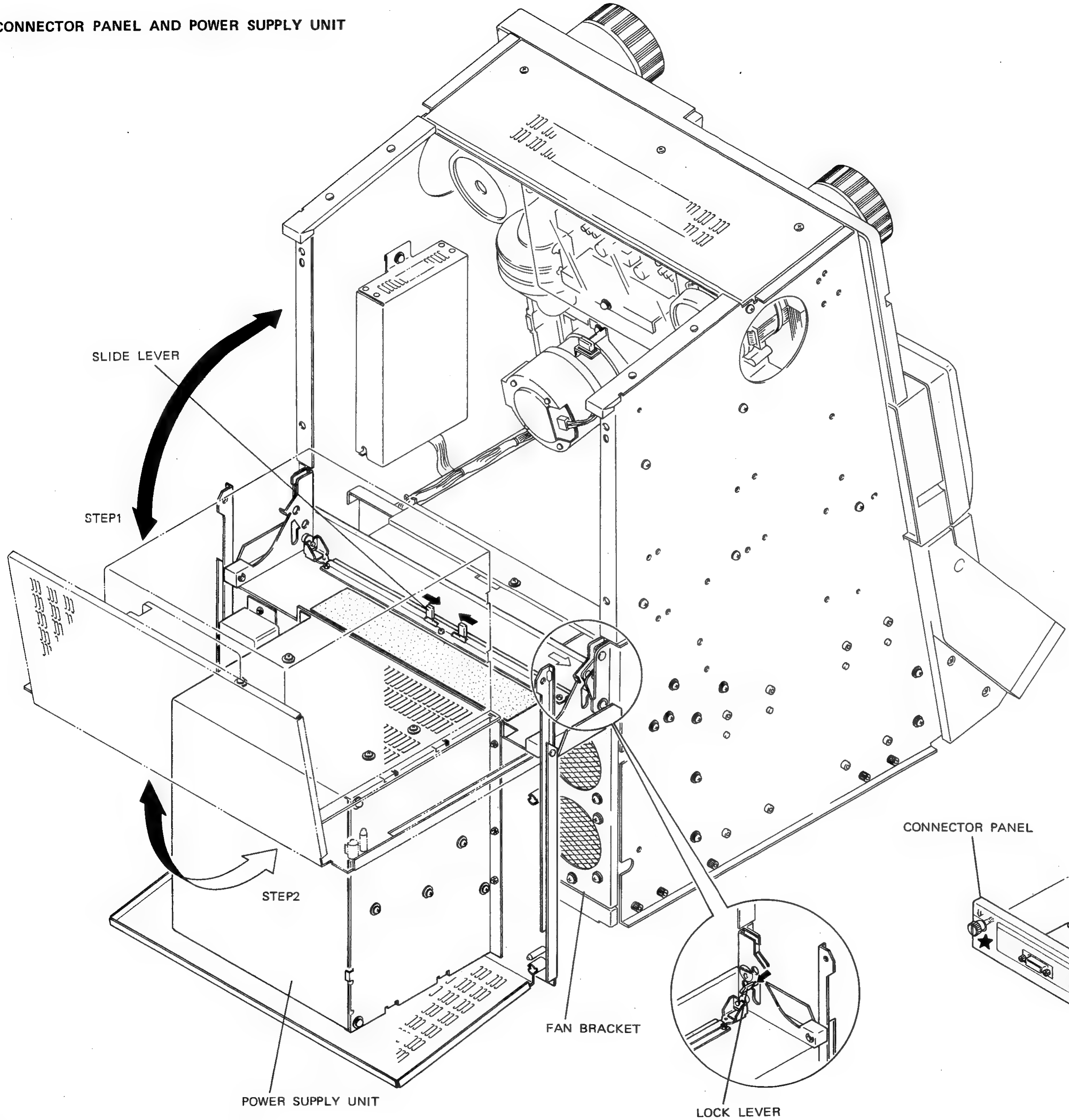
2-2. CABINET REMOVAL

FRONT PANEL REMOVAL

NOTE: Asterisked screws have drop prevention mechanism.
Do not remove forcibly.



OPENING OF THE CONNECTOR PANEL AND POWER SUPPLY UNIT



Opening the power supply unit

1. Adequately slacken the four screws marked ⇒, then open the power supply unit to STEP 1.
2. Push the slide lever in the direction of the arrow while retaining the power supply unit with the hand, then slowly lower the power supply unit to STEP 2.

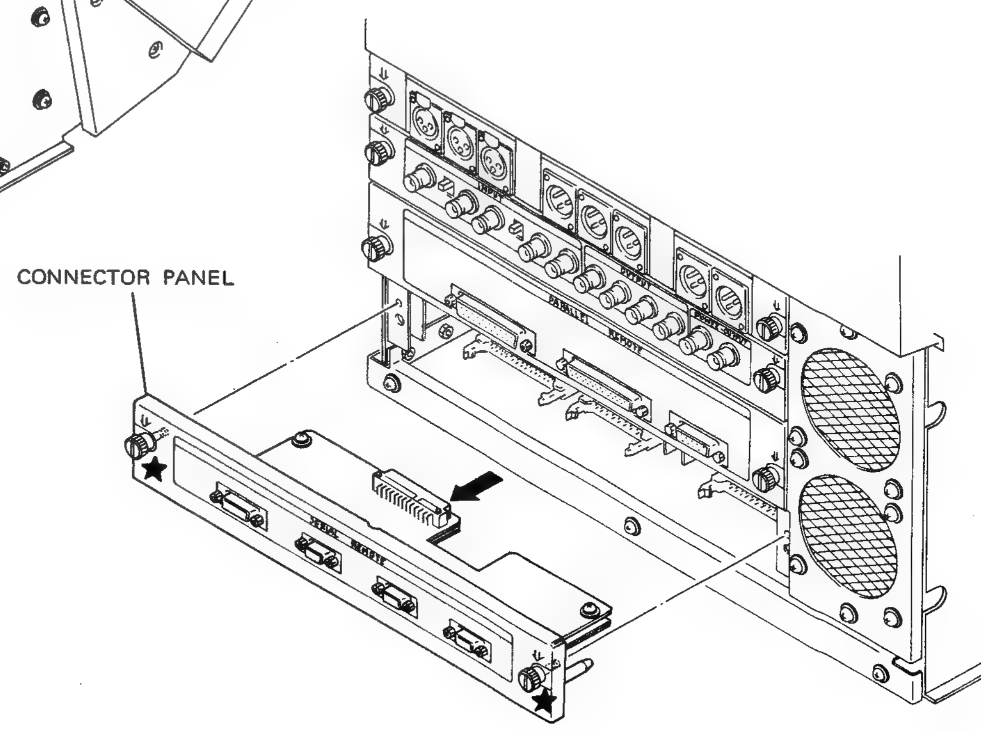
Closing the power supply unit

1. Return the power supply unit to STEP 1.
2. Close the power supply unit while pushing the lock lever in the direction of the arrow.
3. Tighten the four screws marked ⇒.

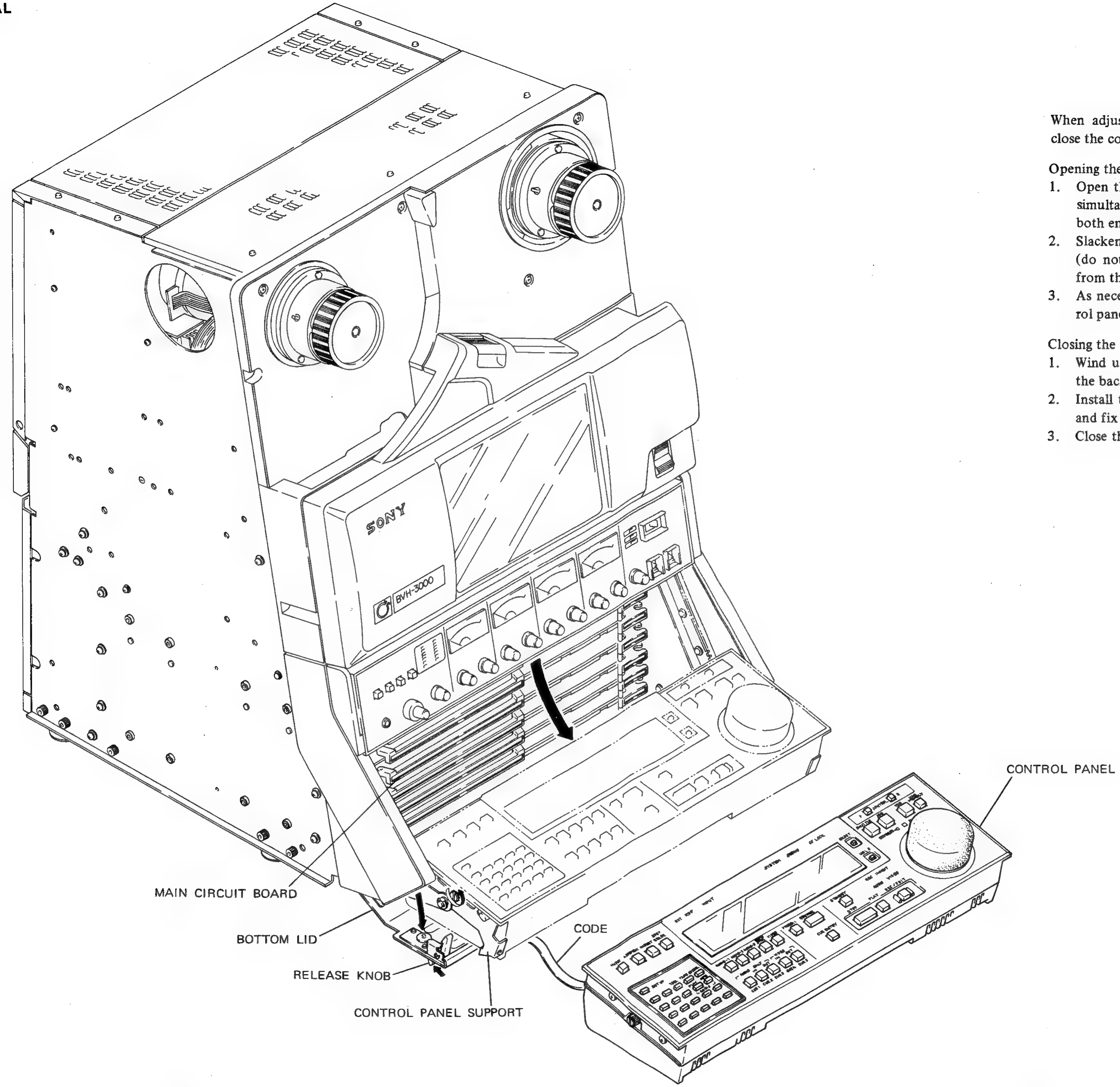
Opening the connector panel

Adequately slacken the two screws marked ⇒, then draw the connector panel forward.

NOTE: Asterisked screws have drop prevention mechanism. Do not remove forcibly.



CONTROL PANEL REMOVAL



When adjusting and checking the main board, open and close the control panel using the following procedure.

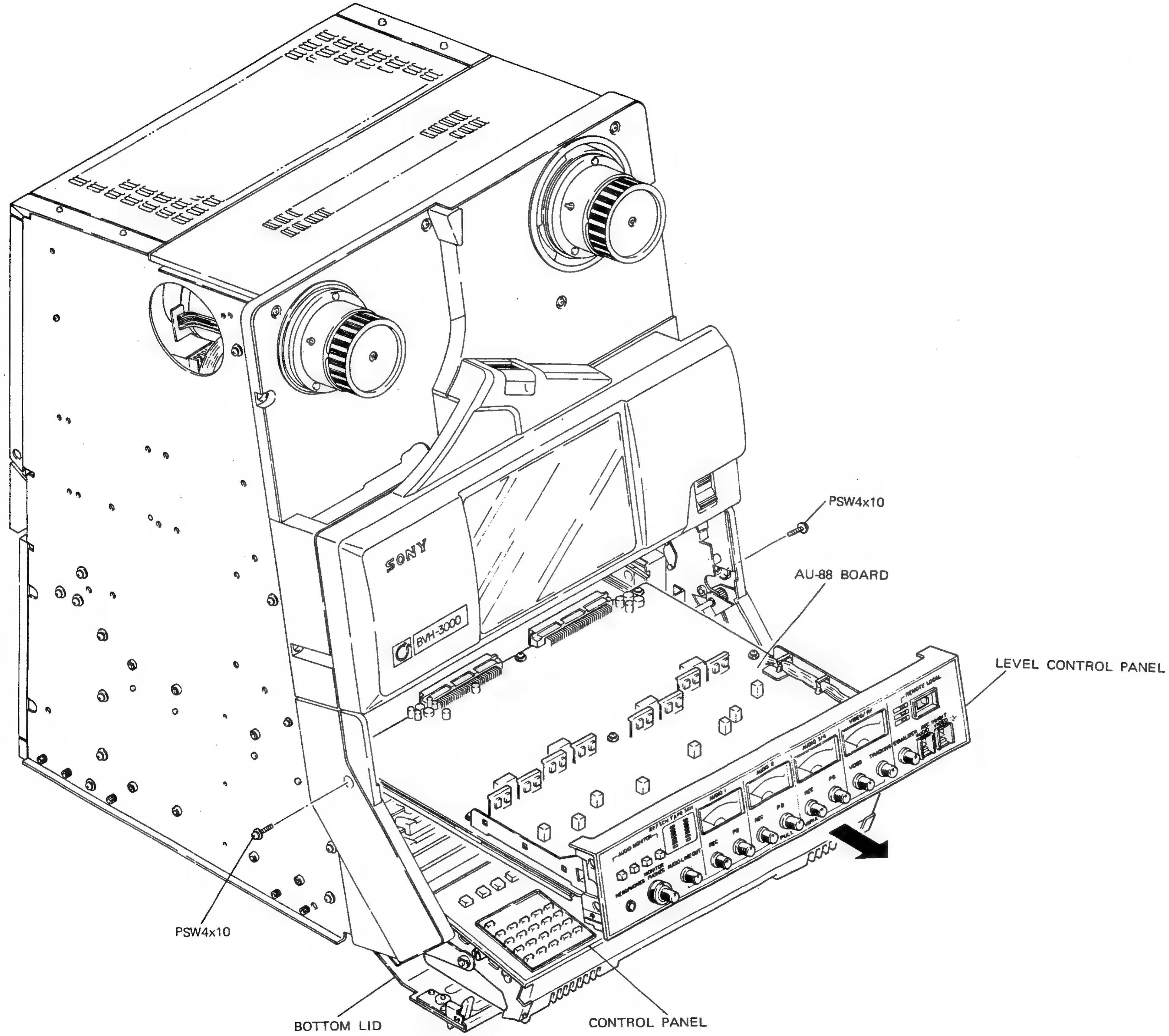
Opening the control panel

1. Open the bottom lid in the downward direction while simultaneously pushing the two lock release knobs on both ends of the bottom lid.
2. Slacken the left and right screws of the control panel (do not remove them), then remove the control panel from the left and right control panel supports.
3. As necessary, unwind the cord at the back of the control panel.

Closing the control panel

1. Wind up the cord in accordance with the the arrow on the back of the control panel.
2. Install the control panel on the control panel support, and fix it with the left and right screws.
3. Close the bottom lid.

LEVEL CONTROL PANEL REMOVAL



When checking or adjusting the AU-88 board, withdraw the level control panel using the following procedure.

1. Open the bottom lid and lower the control panel.
2. Unscrew the left and right screws fixing the level control panel.
3. Insert the hand beneath the level control panel, and draw the panel forward.

NOTE: When re-installing the level control panel, carry out the reverse procedure to steps 1 to 3.

2-3. NOTES ON POWER UNIT

2-3-1. Capacity of AC Power Source

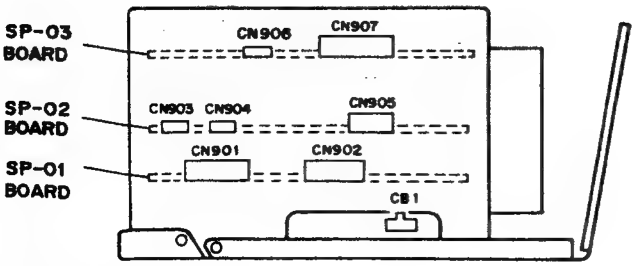
The AC (50/60 Hz) power supply voltage of the BVH-3000/3100 is 100 to 120V (100 to 240V for PS model) ±10% and the power consumption of the BVH-3000/3100 is 500W max.
However, in the worst case, an input current of about 10A for AC 100V or 6A for AC 240V plus a surge current of about 3 to 4 times this value will flow. Unless the AC supply has sufficient capacity to handle this current, the breaker on the AC supply side will operate, and also the input voltage detector inside the BVH-3000/3100 will operate, causing the VTR to go into the STOP mode.

2-3-2. Ventilation/Heat Sink

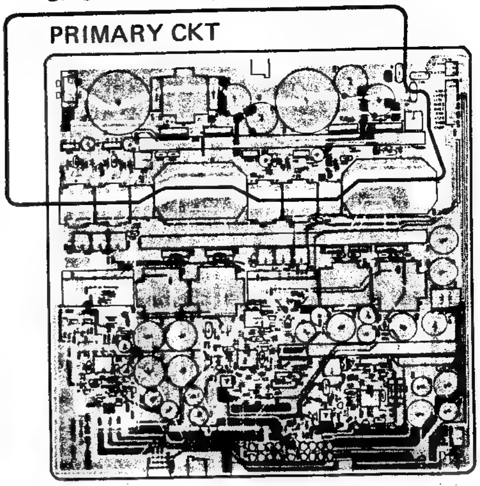
The three fans are for cooling the BVH-3000/3100. If either the intake or exhaust should become clogged or the fans stop, damage may result to the power unit etc.
The heat sinks provided on each board are rated on the assumption that cooling will be provided by the fans. Consequently, the unit should not be operated too long without fan cooling (such as when the unit is opened for checks etc.).

2-3-3. Primary Circuit & Electric Shock

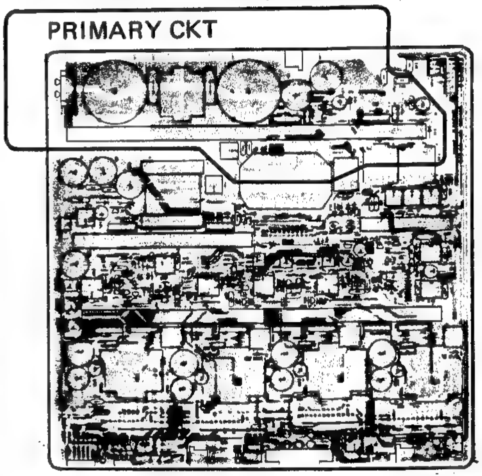
The power supply comprises the SP-01, SP-02 and SP-03 boards, and mounted on the chassis as the power unit.
Since the power supply is mainly on the primary side, it is important to beware of electric shock. The figure below shows the primary side of each board. The heat sinks on the primary zone of the SP-01, SP-02 and SP-03 are also connected to the primary.
Note that even after the power switch is turned off, a high voltage remains in the electrolytic capacitors in the power unit and it is dangerous to discharge them rapidly.
Since the DD-7 board (DT driver) outputs high voltage, beware of electric shock.
As the input, rectifier circuit and secondary circuit all have different potentials, do not use the same "cold (GND)" for all of them.



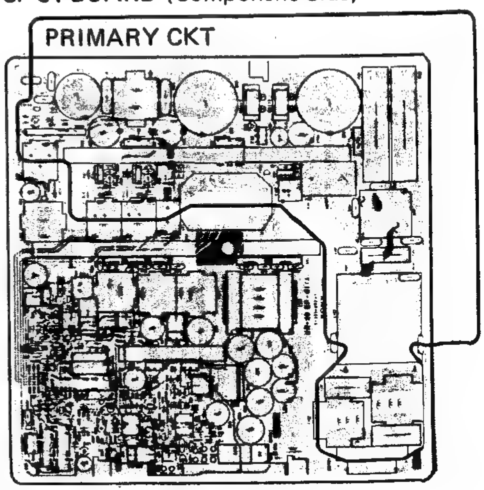
SP-03 BOARD (Component Side)



SP-02 BOARD (Component Side)



SP-01 BOARD (Component Side)



2-3-4. Output Protection Function

If the output of either the ±5V, ±12V, or ±18V preregulator of the power supply unit drops due to a short circuit or if the load across any one of them is unsuitable, all of the outputs will be interrupted. To reset the power supply, first turn the power switch to OFF, wait for about 30 seconds (or for about 2 minutes with a 220/240V AC power line voltage), and then turn it back to ON again.

2-3-5. LEDs for DC Output Check

Green LEDs are provided on the SP-01 and SP-03 boards for the following output checks :

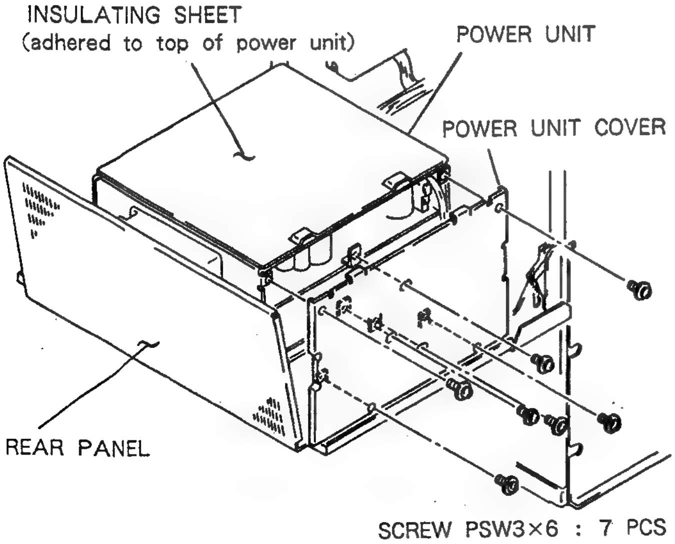
SP-01 board	SP-03 board
D210 : +5V	D204 : +12V
D217 : −5V	D222 : −12V
	D220 : +18V
	D221 : −18V

2-3-6. Power Supply Board Removal

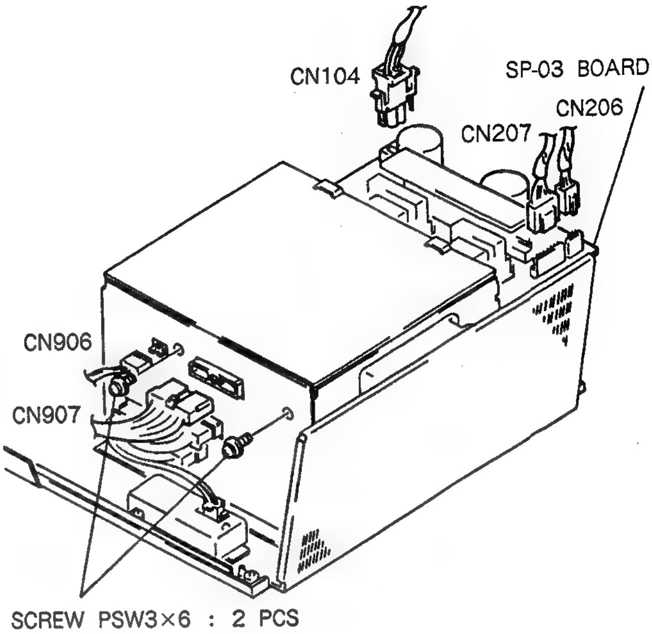
The SP-01, SP-02 and SP-03 power supply boards are located inside the power unit, and they should be removed from the unit as instructed below when they are to be inspected and adjusted.

[SP-03 board removal]

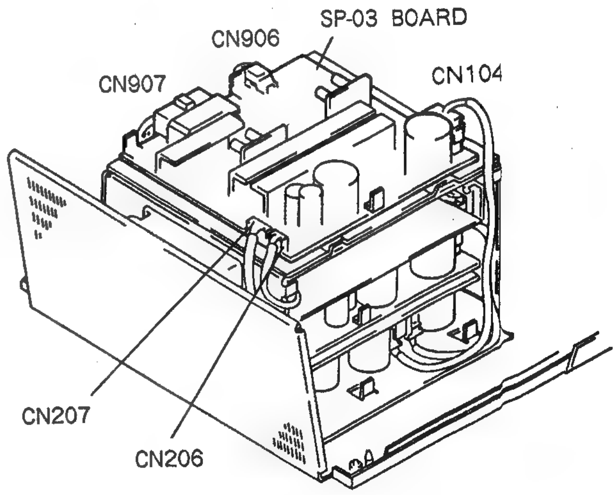
(1) Refer to page 2-11 and open the rear panel. Remove the cover of the power unit as shown in the figure below.



(2) Disconnect connectors CN906 and 907 and remove the two screws (PSW3×6). Then draw out the SP-03 board slightly and disconnect connectors CN104, 206 and 207 from the board.



(3) Place the SP-03 board on top of the power unit and connect connectors CN104, 206, 207, 906 and 907 to the SP-03 board. Now proceed to inspect and adjust the SP-03 board.

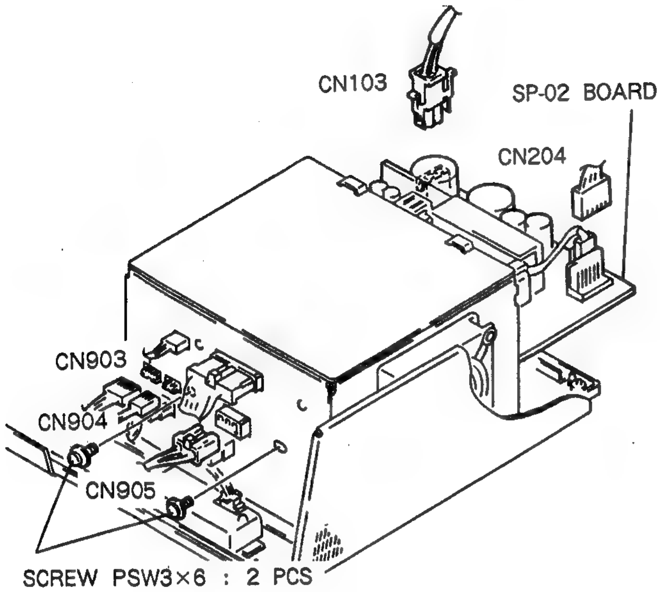


(4) Upon completion of the inspection and adjustment, return the SP-03 board to the inside of the power unit following the procedure for its removal in reverse.

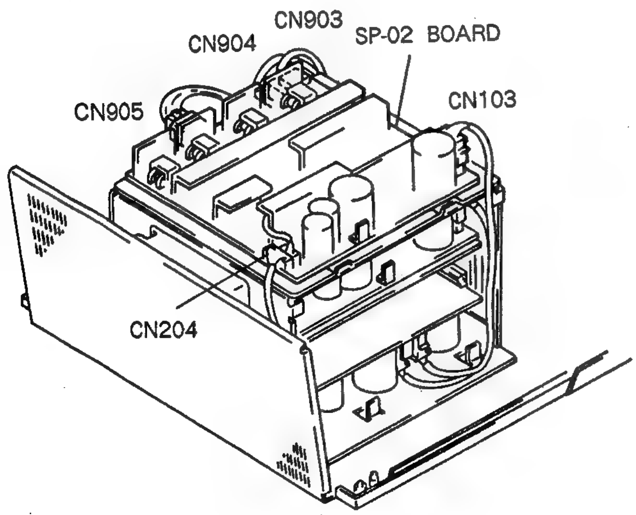
[SP-02 board removal]

(1) Remove the cover of the power unit. Refer to step (1) describing the removal of the SP-03 board.

(2) Disconnect connectors CN903, 904 and 905 and remove the two screws (PSW3×6). Then draw out the SP-02 board slightly and disconnect connectors CN103 and 204 from the board.



(3) Place the SP-02 board on top of the power unit and connect connectors CN103, 204, 903, 904 and 905 to the SP-02 board. Now proceed to inspect and adjust the SP-02 board.

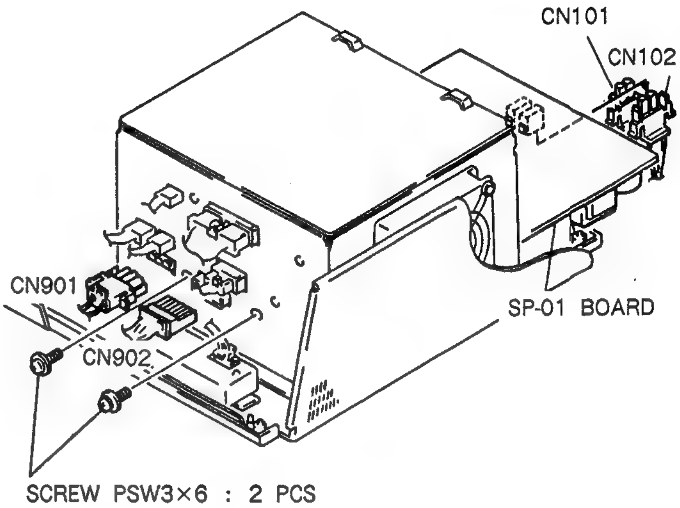


(4) Upon completion of the inspection and adjustment, return the SP-02 board to the inside of the power unit following the procedure for its removal in reverse.

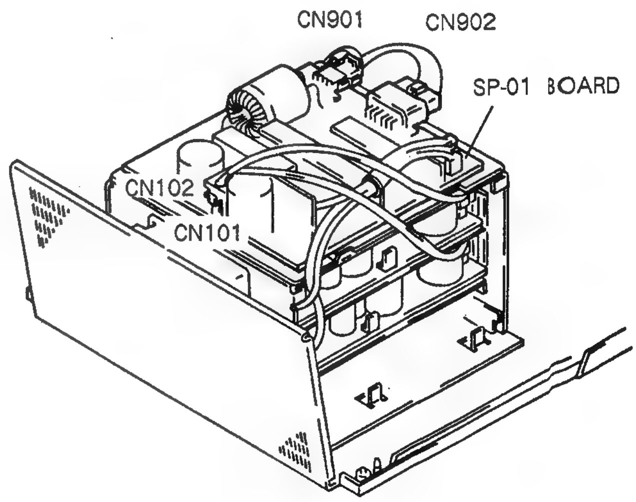
[SP-01 board removal]

(1) Remove the cover of the power unit. Refer to step (1) describing the removal of the SP-03 board.

(2) Disconnect connectors CN901 and 902 and remove the two screws (PSW3×6). Then draw out the SP-01 board slightly and disconnect connectors CN101 and 102 from the board.



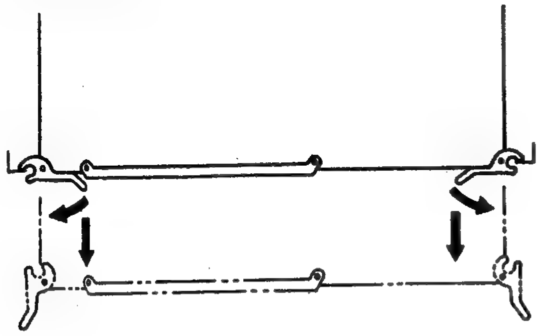
(3) Place the SP-01 board on top of the power unit and connect connectors CN101, 102, 901 and 902 to the SP-01 board. If the harnesses of the connectors CN901 and 902 are short, remove their clamping bands. Now proceed to inspect and adjust the SP-01 board.



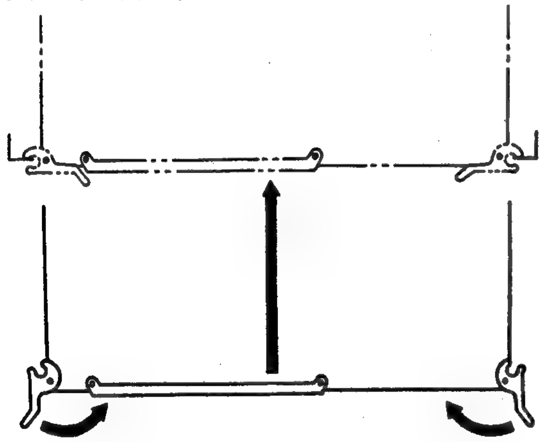
(4) Upon completion of the inspection and adjustment, return the SP-01 board to the inside of the power unit following the procedure for its removal in reverse.

2-4. EXTRACTING/INSERTING PLUG-IN BOARDS

Wait at least 2 seconds after having switched off the power before removing or inserting any of the plug-in boards.
Use the eject levers to disconnect the boards from the connectors.



Set the eject levers to the positions shown and then insert the boards.

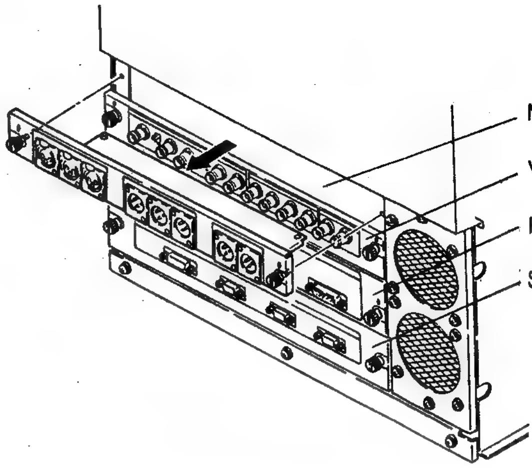


The AU-88 board is located at the rear of the level control panel. Refer to pages 2-15 and 2-16 when removing this board.

2-5. NOTES FOR CHECKING CONNECTOR PANEL

When checking the boards of the connector panels, remove the upper connector panels and open the power supply unit, then check the board of the lower panel.

MA-26 board : Open the power supply unit and check this board.
VS-30 board : Remove the MA-26 ASSY, then open the power supply unit, and check this board.
PA-56 board : Remove the MA-26 ASSY and VS-30 ASSY, then open the power supply unit and check this board.
SE-49 board : Remove the MA-26 ASSY, VS-30 ASSY, and PA-56 ASSY, then open the power supply unit and check this board.



2-6. NOTES ON REPAIR PARTS

(1) Safety Related Components Warning

Components identified by shading marked with ⚠ on the schematic diagrams, exploded views and electrical spare parts list are critical to safe operation. Replace these components with Sony parts whose part numbers appear in this manual or in service bulletins and service manual supplements published by Sony.

(2) Standardization of Parts

Repair parts supplied from Sony Parts Center may not be always identical with the parts which actually in use due to "accommodating the improved parts and/or engineering changes" or "standardization of genuine parts".
This manual's exploded views and electrical spare parts list are indicating the part numbers of "the standardized genuine parts at present".

(3) Stock of Parts

Parts marked with "o" in SP (Supply Code) column of the spare parts list are not normally required for routine service work. Orders for parts marked with "o" will be processed, but allow for additional delivery time.

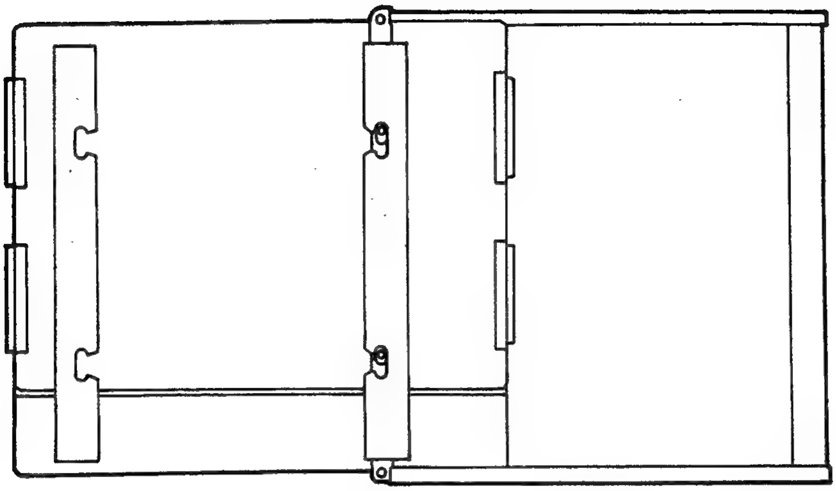
(4) Units for Capacitors, Inductors are Resistors

The following units are assumed in schematic diagrams, electrical parts list and exploded views unless otherwise specified :

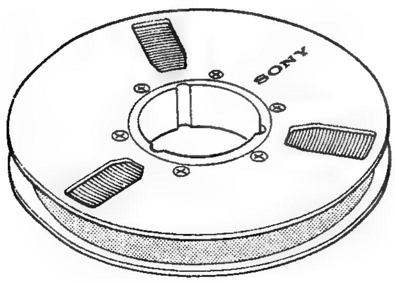
Capacitors ; μF
Inductors ; μH
Resistors ; ohm

2-7. MAINTENANCE TOOLS/FIXTURES

Extender, EX-136 Sony Part No. A-6001-007-A
Used for checking and repairing the plug-in circuit board in the card rack. The VTR has 1 pc as an accessory.



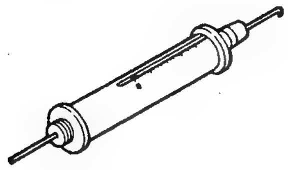
Alignment Tape
BR5-2NTSC Sony Part No. 8-944-005-03
An alignment tape for BVH series NTSC VTR. The contents are shown on the section 2-8.
BR5-2PS-A4 Sony Part No. 8-944-005-63
An alignment tape for BVH series PAL/SECAM VTR. The contents are shown on the section 2-8.



Tension Scale, 5k grams

Sony Part No. J-6041-640-A

The 5k grams tension scale is used for pinch roller pressure adjustment.



Tension Adjustment Tool

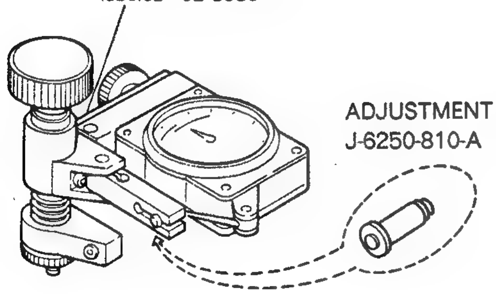
Sony Part No. J-6251-960-A

Used for tape tension adjustment.

Drum Eccentricity Adj. Gauge

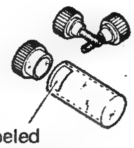
Sony Part No. J-6250-800-A

Used for drum eccentricity adjustment and for rotary head tip projection check.



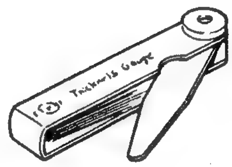
Tapered Screw Sony Part No. J-6040-460-A

Consists of two tapered screws and used for upper drum position adjustment.



Thickness Gauge Sony Part No. J-6041-670-A

Used for mechanical parts position adjustment.

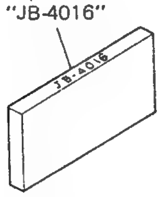


thickness (mm)

0.03	0.04	0.08
0.09	0.10	0.11
0.12	0.13	0.14
0.15	0.20	0.25
0.30	0.35	0.40
0.45	0.50	0.60
0.75	0.80	0.90
1.00		

Flat Plate Sony Part No. J-6040-160-A

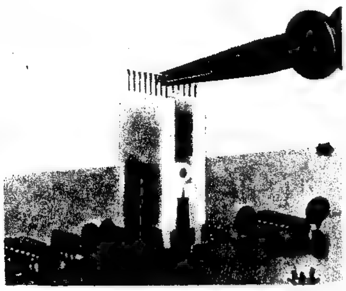
Used for stationary head zenith check and adjustment.



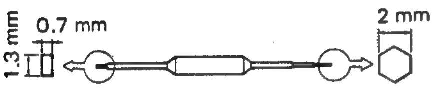
IC Test Clip, TC-16 Sony Part No. J-6041-770-A
IC Test Clip, TC-20 Sony Part No. J-6041-780-A

Manufactured by :
AP PRODUCTS INCORPORATED
P.O.Box 697, 72 Corwin Drive,
Painesville, Ohio 44077, U.S.A.
Phone : (216) 354-2101

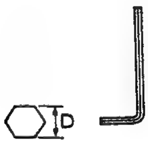
When connecting the test probe to the terminal of DIP integrated circuit, these clips are convenient. Type TC-16 is for DIP 14-pin or 16-pin IC and Type TC-20 is for 18-pin or 20-pin IC.



Alignment Screwdriver Sony Part No. 7-700-733-01
Used to adjust variable resistors and variable inductors etc.



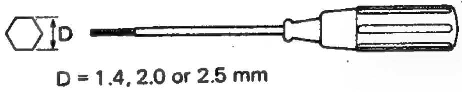
L-shaped Hexagonal Wrench Set
Sony Part No. 7-700-736-00
or J-6041-700-B



D (mm)	7-700-736-00	J-6041-700-B
1.27	○	
1.4	○	
1.5	○	○
1.58	○	
2.0	○	○
2.5	○	○
3.0	○	○
4.0	○	○
5.0	○	○
6.0	○	
8.0	○	
10	○	

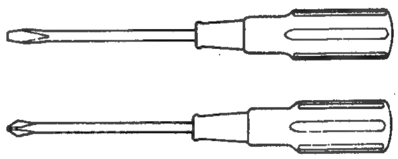
Hexagonal Screwdriver, 1.4mm
Sony Part No. 7-700-766-02
Hexagonal Screwdriver, 2mm
Sony Part No. 7-700-766-03
Hexagonal Screwdriver, 2.5mm
Sony Part No. 7-700-766-04
Hexagonal Screwdriver, 3mm
Sony Part No. 7-700-766-05

Used for stationary head replacement.



Nut Driver, 5.5mm Sony Part No. 7-700-751-02
Used to remove the power unit.

Flat Blade Screwdriver
Phillips Screwdriver
These screwdrivers are necessary for servicing.

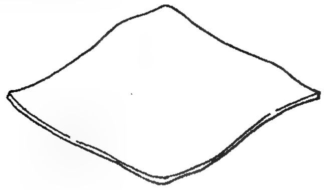


Erase Head Spacer "B" (For PS model)
Thickness 0.05mm Sony Part No. 3-651-419-01
Thickness 0.1mm Sony Part No. 3-651-419-21

These may be necessary for the height adjustment of V/S erase head when replacing it.

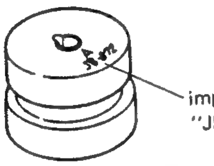
Cleaning Piece Sony Part No. 2-034-697-00

Clean the surface of parts with this cleaning piece moistened with cleaning fluid.



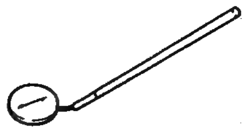
Brake Adjustment Fixture Sony Part No. J-6043-720-A

Used when replacing the reel motor, brake band or brake solenoid.



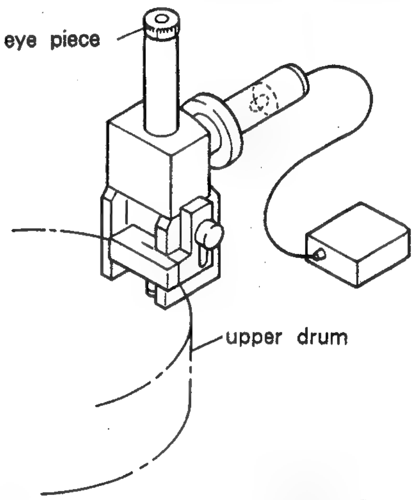
Inspection Mirror Sony Part No. 7-723-902-00

Used for observing tape path.

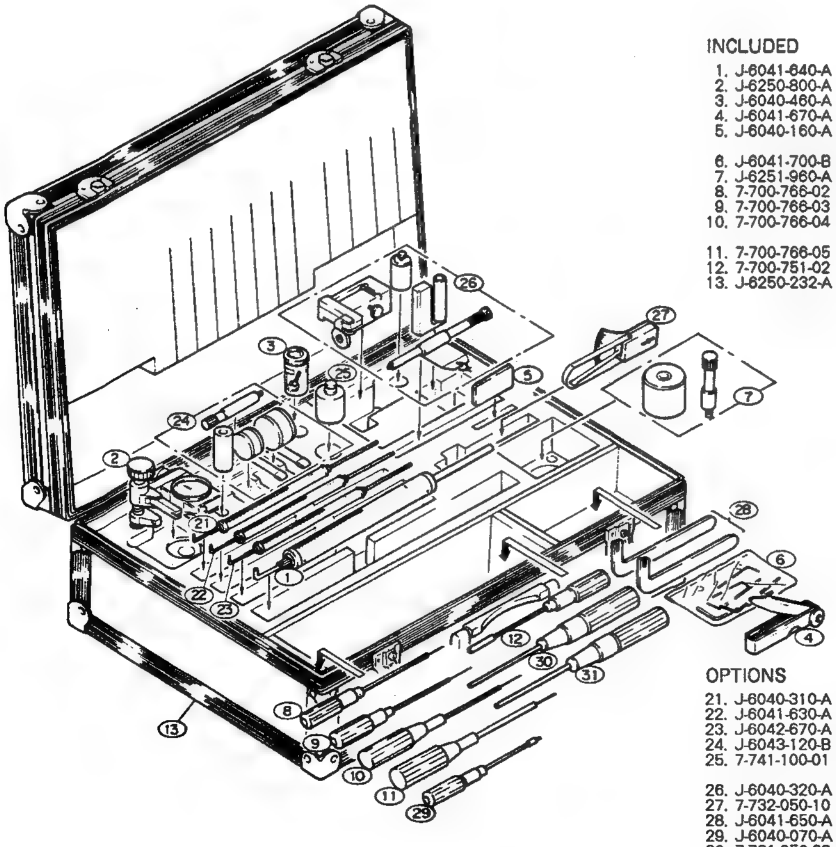


Head Tip Microscope Sony Part No. J-6252-210-A

Used for observing the surface of video heads. Please refer to the instruction sheet supplied to the microscope.



BVH-3000 Tool Kit Sony Part No. J-6252-330-A



INCLUDED	USED FOR BVH-3000 3100	BVH-2XXX series	BVH-1180 1100A	BVH-1000A 1100	HDV-1000
1. J-6041-640-A Tension Scale, 5kgrams	O	O	O	O	O
2. J-6250-800-A Drum Eccentricity Adj. Gauge	O	O	O	O	–
3. J-6040-460-A Tapered Screws	O	O	O	O	O
4. J-6041-670-A Thickness Gauge	O	O	O	O	O
5. J-6040-160-A Flat Plate	O	O	O	O	O
6. J-6041-700-B L-shaped Hex. Wrench Set	O	O	O	O	O
7. J-6251-960-A Tension Adjustment Tool	O	–	–	–	–
8. 7-700-766-02 Hex. Screw Driver, 1.4mm	O	O	–	–	O
9. 7-700-766-03 Hex. Screw Driver, 2mm	O	O	–	–	O
10. 7-700-766-04 Hex. Screw Driver, 2.5mm	O	O	–	–	O
11. 7-700-766-05 Hex. Screw Dirver, 3mm	O	–	–	–	–
12. 7-700-751-02 Nut Driver, 5.5mm	O	O	–	–	O
13. J-6250-232-A Carrying Case	O				

OPTIONS	BVH-3000 3100	BVH-2XXX series	BVH-1180 1100A	BVH-1000A 1100	HDV-1000
21. J-6040-310-A Tension Scale, 500grams	–	–	O	O	–
22. J-6041-630-A Tension Scale, 200grams	–	O	O	O	–
23. J-6042-670-A Tension Scale, 1kgrams	–	O	O	–	–
24. J-6043-120-B Tension Adjustment Tool	–	O	–	–	O
25. 7-741-100-01 Weight, 200grams	–	–	O	–	–
26. J-6040-320-A Tension Adjustment Tool	–	–	O	O	–
27. 7-732-050-10 Sector Gauge, 20grams	–	–	O	–	–
28. J-6041-650-A Tension Arm Bending Tools	–	–	O	O	–
29. J-6040-070-A Eccentric Screw Driver	–	–	O	O	–
30. 7-721-050-63 TOTSU Screw Driver, 3mm	–	O	O	O	O
31. 7-721-050-64 TOTSU Screw Driver, 4mm	–	O	O	O	O

2-8. ALIGNMENT TAPE BR5-2PS-A4

The BR5-2PS-A4 alignment tape is for Sony BVH series PAL/SECAM VTR.
The following signals are recorded on it.

TIMER min. sec	AUDIO: USE	AUDIO: CONTENTS (CH1, CH2, CH3, CH4)	SYNC	VIDEO: VIDEO CONTENTS	VIDEO: USE
0.00 – 4.00	PHASE	3kHz, +8dBm	*3	100% WHITE	TRACKING
4.00 – 8.30	PHASE	15kHz, +8dBm			
9.00 – 14.00	NIL	BLANK	*3	LINEARITY	DG, DP
14.30 – 16.30	OUTPUT LEVEL	1kHz +8dBm (, , ,)*1		MULTIBURST	FREQUENCY RESPONSE
17.00 – 18.30	FREQUENCY RESPONSE	1kHz (← REFERENCE →)		LINE 17 SIGNAL	K FACTOR etc.
19.00 – 24.00 (every 30sec.)		−2dBm: 50 Hz (, , ,)*2		100/0/75/0 PAL COLOUR BARS	GENERAL PERFORMANCE CHECK
		100 Hz (, , ,)			
		200 Hz (, , ,)			
		300 Hz (, , ,)			
		500 Hz (, , ,)			
		3 kHz (, , ,)			
		5 kHz (, , ,)			
		7.5 kHz (, , ,)			
		10 kHz (, , ,)			
		15 kHz (, , ,)			
24.30 – 26.30	NIL	BLANK	*3	100/0/100/0 PAL COLOUR BARS	GENERAL PERFORMANCE CHECK
27.00 – 29.00	NIL	BLANK	BLACK BURST	SECAM COLOUR BARS	GENERAL PERFORMANCE CHECK

*1 When playing back this tape, check/adjust the machine so that its audio output level is the normal level (+8dBm) plus the calibration level (dB) as follows.
ex. calibration level = −0.5dB
actual output level = +8−0.5 = +7.5dBm

*2 When playing back this tape, check/adjust the audio frequency response of the machine so that its output level at each frequency is the reference level at 1kHz plus the calibration level (dB).

*3 The VITS is recorded.

SYNC CHANNEL	LINE 14/327	MULTIBURST
	LINE 15/328	LINE 17 SIGNAL
VIDEO CHANNEL	LINE 19/332	LINE 17 SIGNAL
	LINE 20/333	MULTIBURST

WARNING

TAPE MUST BE STOPPED IN THE BLACK SEGMENTS ONLY. STOPPING FROM REWIND OR FAST FORWARD, AND STARTING THE REWIND OR FAST FORWARD MUST BE MADE IN THE BLACK SEGMENTS ONLY.

NEVER PUT THE MACHINE INTO JOG OR STILL MODE WHILE ALIGNMENT TAPE IS THREADED. ABOVE CONDITION MUST BE MET TO AVOID A POSSIBLE DAMAGE TO THE TAPE AND TO PROLONG THE LIFE EXPECTANCY OF THE HIGHLY CALIBRATED ALIGNMENT TAPE.

CAUTION

1. KEEP THIS TAPE AWAY FROM STRONG MAGNETIC FIELDS.

2. AVOID STORAGE AT HIGH TEMPERATURES. MAXIMUM STORAGE TEMPERATURE IS 40℃ (104℉).

2-9. FUNCTIONS OF SWITCHES AND JUMPERS ON BOARDS

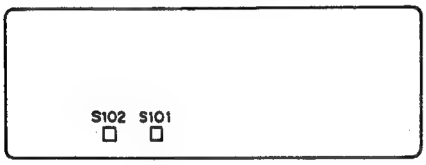
AU-88 Board

JP101, 102 : Audio-1
JP301, 302 : Audio-2
JP501, 502, 503 : Audio-3
JP701, 702 : Audio-4 (model PS-A4 only)
These are the audio input impedance changeover jumpers. Refer to section 1-7-2.

JP104, 105 : Audio-1
JP304, 305 : Audio-2
JP505, 506 : Audio-3
JP704, 705 : Audio-4 (model PS-A4 only)
These are the audio input level changeover jumpers. Refer to section 1-7-3.

KC-14 Board

KC-14 Board : component side

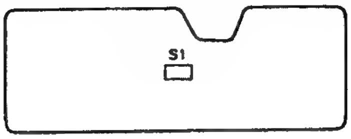


S101 : RESET switch
This is the reset switch for the function control panel. By pressing this switch, the function control panel will go into the same status as if the power had been turned OFF and then ON again.

S102 : TEST switch
By pressing this switch, the machine will go into the PANEL menu of the test menu. Refer to 3-3 "Maintenance Menu".

PA-56 Board

PA-56 Board : component side

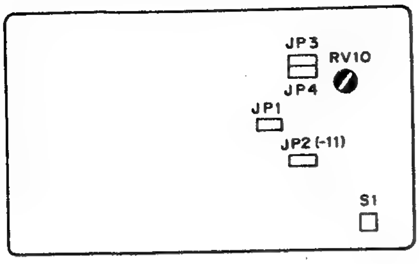


S1 : Input/output selector switches for SPARE-1, 2, 3, and 4 pins of REMOTE-3
When using the SPARE-1, 2, 3, AND 4 pins of the REMOTE-3 connector as inputs, turn the switches OFF, and when using them as outputs, turn the switches ON. All of these switches are set to OFF at the factory.
S1-1 : SPARE-2 signal (pin 22/REMOTE-3)
S1-2 : SPARE-1 signal (pin 37/REMOTE-3)
S1-3 : SPARE-4 signal (pin 40/REMOTE-3)
S1-4 : SPARE-3 signal (pin 23/REMOTE-3)

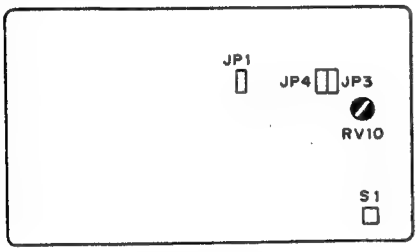
RD-6 and 7 Boards

(RD-6 is for NTSC, and RD-7 for PAL/SECAM)

RD-6 Board : component side



RD-7 Board : component side



JP1 : NM1 (NON MASKABLE INTERRUPT) ON/OFF jumper

Normally short circuited.

JP2 : EPROM OUTPUT ENABLE ON/OFF jumper (RD-6 board with suffix -11 only)

Normally short circuited.

JP3, 4 : DT DRIVE test jumper

Normally, short circuit JP3 and open circuit JP4.
As shown below, if JP4 is short circuited, the DT head can be manually operated by RV10.

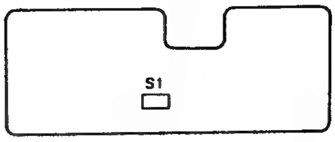
(1) Switch the VTR OFF, then remove the jumper plug from JP3 and reconnect it to JP4.
(2) Switch the VTR ON. Turn RV10 and visually confirm the motion of the DT head.
(3) Return RV10 to the mechanical center position.
(4) Turn the power OFF, then remove the jumper pin from JP4 and reconnect it to JP3.

S1 : TEST switch

Not used.

SE-49 Board

SE-49 Board : component side



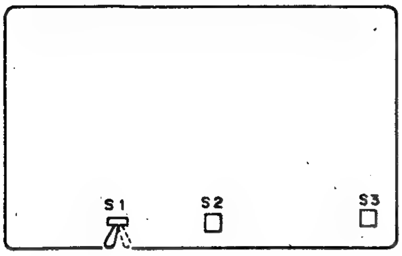
S1 : REMOTE-2A, 2B signal terminating ON/OFF switches

By turning the switches ON, the following signals will be terminated in 100 ohms. All of these switches are set to OFF at the factory.

- S1-1 : REMOTE-2A IN signal (REMOTE-2A connector)
- S1-2 : REMOTE-2A OUT signal (REMOTE-2A connector)
- S1-3 : REMOTE-2B IN signal (REMOTE-2B connector)
- S1-4 : REMOTE-2B OUT signal (REMOTE-2B connector)

SV-90 Board

SV-90 Board : component side



S1 : TAPE RUN switch (NORMAL/STOP)
Normally, leave this switch in the "NORMAL" position. If it is put in the "STOP" position, the drive amplifiers of the following motors and solenoids will go OFF, causing the motors to stop and the solenoids to be deenergized. Use this switch to check the operation of the circuits.

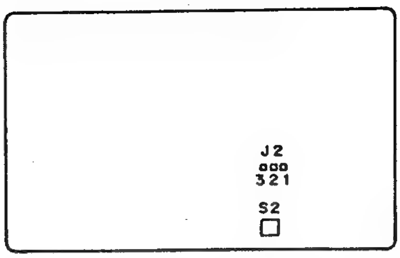
Capstan Motor
Drum Motor
Reel Motors (S and T)
IP Roller Motor
Threading Motor
Blowers (S and T)
Pinch Roller Solenoid
Reel Brake Solenoids (S and T)

S2 : NVRM (NOVRAM WRITE) switch
Turn this switch ON when writing adjustment data for the drum, capstan, reel, and servo, etc., in the NOV RAM. Refer to 3-3 "Maintenance Menu".

S3 : RESET switch
This is the system reset switch. By turning this switch ON, the VTR will go into the same status as if the power had been turned OFF and then ON again.

SY-103 Board

SY-103 Board : component side

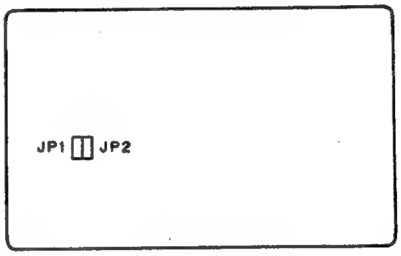


J2 : ROM (256/512) changeover jumper (2-1/2-3)
Set this jumper depending upon whether the capacity of the IC H11 EPROM is 256kbit or 512kbit.
For 256kbit, short 2-1. For 512kbit, short 2-3.
For BVH-3000/3100, a 256kbit EPROM is used.

S2 : TEST switch
By pressing the $\boxed{0}$ key on the 21-key section while pressing this switch, the TTP ADJ menu of the test menu will appear. Refer to 3-3 "Maintenance Menu".

VO-16 Board

VO-16 Board : component side



JP1, 2 : DROPOUT TEST jumpers
Normally, short circuit JP1 (for VO-16 board with suffix -11, short circuit JP2). When adjusting the dropout width sensitivity, short circuit JP2 (for VO-16 board with suffix -11, short circuit JP1).

SECTION 3
DIAGNOSIS FUNCTION

3-1. ERROR MESSAGES

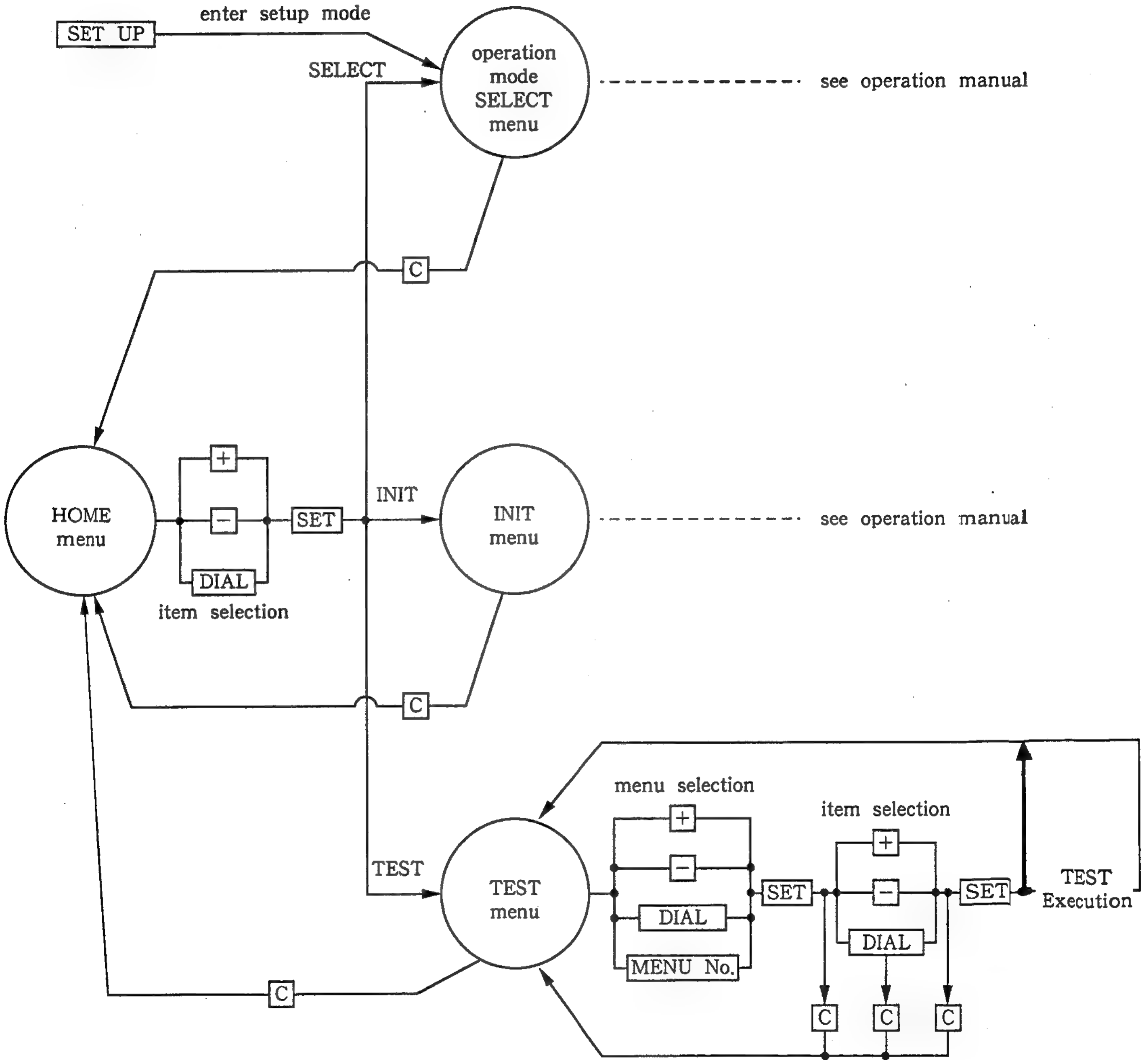
An error message will be displayed on the control panel if an error occurs after the power-on or during operation.
The meaning of the letters displayed is as follows.
The error message can be superimposed on the monitor by the menu setting.
For details, refer to the operation manual.

SYS ERR :	A system error, showing that the system control is not operating normally.
SRV ERR :	A servo error, showing that normal communication does not take place between system control circuit and servo circuit, for example, SV-90 board is not correctly installed.
OVERHEAT :	Overheating of the power supply system.
LINE ERR :	A line error, when remote control communication is not performed correctly.
ABORT :	An editing operation is not performed correctly.
LOST LCK :	Servo lock is lost during recording.
NEGATIVE :	The edit OUT point is placed before the edit IN point.
DATA ERR :	An invalid numerical value is set as time data (for example, 65 seconds 35 frames, etc.).
TAPE OUT :	The tape is not loaded correctly.
NO EOS :	When an attempt was made to perform BACK SPACE EDIT, there was no recorded part available for connection. (END OF SOURCE is not recorded.)
TBC REF :	The TBC reference signal is not received.
SV REF :	The servo reference signal is not received.
SV90 SW :	The NOR/STOP select switch on the SV-90 board is set to STOP.
RD BATT :	The voltage of the battery on the RD-6/7 board has lowered below the limit. If this message is displayed, replace the battery BT1 on the RD-6/7 board with new one and perform "Section 13-12. Auto Jump Adjustment".
AU BOARD :	The AU-88 board is not properly installed, or an error has occurred in the bus interface.
VO BOARD :	The VO-16 board is not properly installed, or an error has occurred in the bus interface.
PR BOARD :	The PR-91/92/96/98 board is not properly installed, or an error has occurred in the bus interface.
PA BOARD :	The PA-56 board is not properly installed, or an error has occurred in the bus interface.
NO RF :	An RF signal is not obtained when the TAPE/EE select switch is set to TAPE and the STANDBY status is OFF, or when a non-recorded part is played.
TEST MOD :	After the VTR was operated in the TEST mode with some Test Mode Menu items changed, the SET UP lamp has been turned off without resetting those items to the default ones.

3-2. TEST FUNCTIONS (TEST MENU)

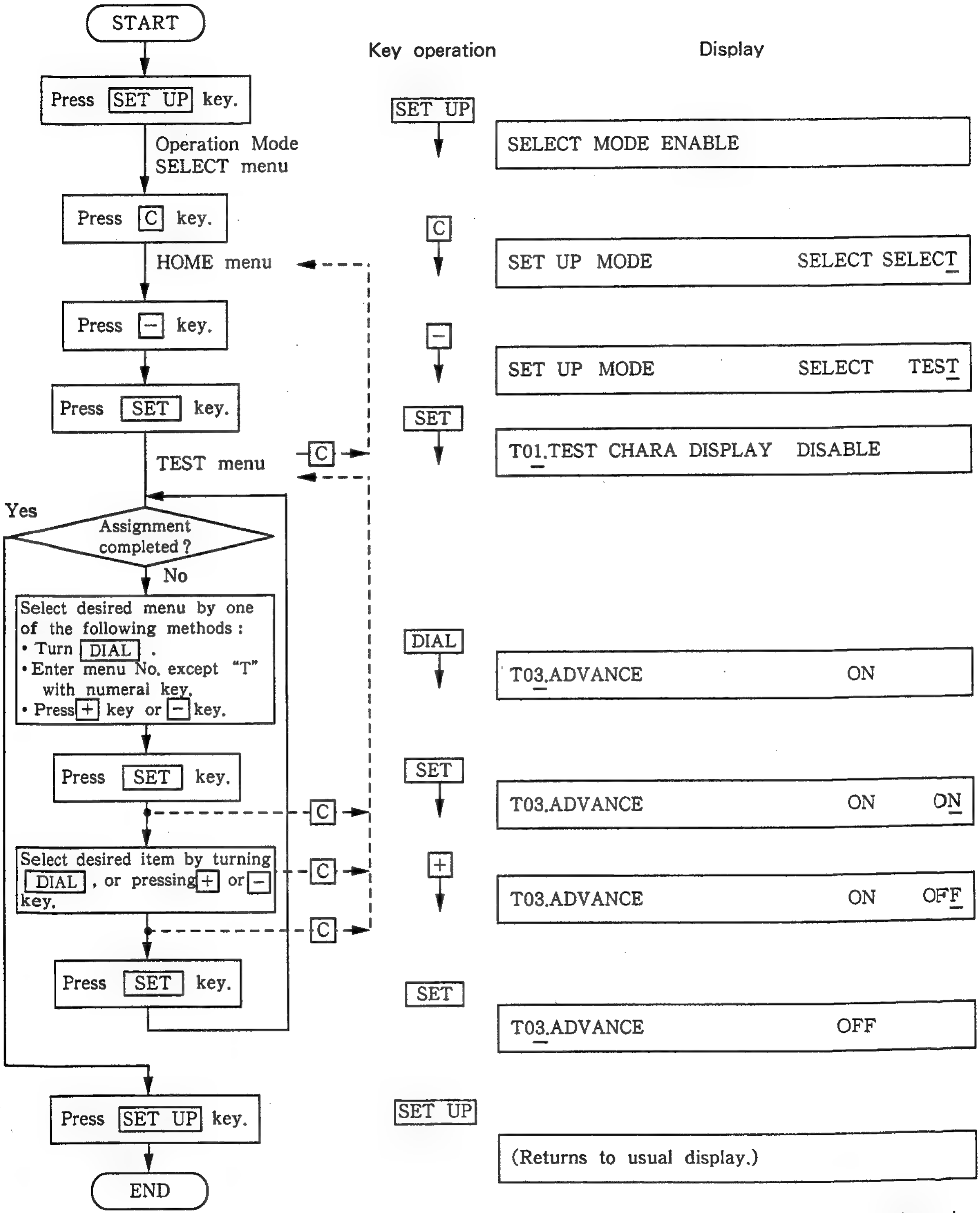
This unit is provided with test functions for performing various tests.

When performing a test, operate the 21-key on the control panel and select a test menu, as shown below. An operation example is shown on the following page.



1) □ shows key or dial operations.
2) Press SET UP key to exit from setup mode.
3) Press C Key to return to the previous step.

Operation flow of TEST menu or example of operation



*1. As shown by broken lines, you can return to the previous step by pressing [C] key. However, the selection finalized by pressing [SET] key cannot be canceled by this means.

The contents of the test menus are shown below.

Note 1 : The □ indication of each item indicates the normal setting.

Note 2 : Upon completion of testing, return each menu to the normal setting before canceling the TEST mode. If the TEST mode is canceled while an individual menu remains activated (when an item not displayed in □ of the mode is selected), TEST MOD will be displayed on BLOCK 6 of the control panel.

Note 3 : If the power switch is turned OFF while the test mode of an individual menu remains activated, theTEST mode will be automatically canceled.

MENU No.	MENU	ITEMS	DESCRIPTION
T01	TEST CHARA DISPLAY	ON [OFF]	Used to specify whether or not to superimpose characters on the picture monitor. When this menu is selected, all types of characters will be displayed, enabling the character generator to be checked. ON : Characters are superimposed. OFF : Characters are not superimposed.
T02	DOC	[ON] OFF	Used to turn the Dropout Compensator ON or OFF. Set to OFF when checking the operation of the Dropout detector. ON : DOC operates. OFF : DOC is turned OFF.
T03	ADVANCE	[ON] OFF	Used to specify whether or not to advance the rotating phase of the drum. ON : Drum is advanced by 8H for BKH-3010, 10H for BKH-3050 (12H for BKH-3020, 14H for BKH-3060). OFF : Drum is not advanced.
T04	AUTO PG	[ON] OFF	Used to stop the AUTO PG function. Use this function when adjusting the drum servo after replacing the drum, and so on. ON : AUTO PG functions. OFF : AUTO PG does not function.
T05	PR TEST 1	[OFF] 0 IRE 100 IRE −10 IRE	Used to turn the adjustment Digital Data on the PR board ON or OFF. OFF : Test signal is turned OFF. 0 IRE : 0 IRE test data is generated. This data is used to generate the set up level (black level). 100 IRE : 100 IRE test data is generated. This data is used to adjust the video level. −10 IRE : −10 IRE test data is generated. This data is used to adjust the dark clip level.
T06	PR TEST 2	ON [OFF]	Used to forcibly set the video level, chroma level, and set up level (black level) on the PR board to the preset values. ON : The video level, chroma level, and set up level (black level) are set to the preset values. OFF : The video level, chroma level, set up level (black level) are set using the controls on the front of the board or the remote controller.

MENU No.	MENU	ITEMS	DESCRIPTION
T07	RD TEST 1	ON $\boxed{\text{OFF}}$	Used to forcibly set the hue (burst-chroma) value on the RD board to the preset value. ON : The hue (burst-chroma) value is set to the preset value. OFF : The hue (burst-chroma) value is set using the control on the front of the board or the TBC remote controller.
T08	RD TEST 2	ON $\boxed{\text{OFF}}$	Used to forcibly set the SC phase on the RD board to the preset value. ON : The SC phase is set to the preset value. OFF : The SC phase is set using the control on the front of the board or the TBC remote controller.
T09	DT TEST	ON $\boxed{\text{OFF}}$	This mode is used to forcibly turn the DT operation OFF. ON : The DT operation is forcibly turned OFF. OFF : The DT operation is turned ON or OFF by commands from the system contol circuit.
T10	AUTO JUMP	$\boxed{\text{ON}}$ OFF	This mode is used to turn the auto jump of the DT head ON or OFF. ON : The auto jump is turned OFF. OFF : The auto jump stops, and the DT jump data is replaced by the initial data.
T11	DP VIDEO	ON $\boxed{\text{OFF}}$	Used to specify whether or not to activate the DP control on the PR board in the EE mode. ON : In the EE mode, the DP control on the PR board is deactivated. OFF : In the EE mode, the DP control on the PR board is activated, enabling the set value to be checked.
T12	NORMAL FWD TEST	ON $\boxed{\text{OFF}}$	This test function enables the NORM FWD + EE signals to be activated in the STOP mode. It is used for checking or adjusting the video circuits. ON : The NORM FWD + EE signals are activated. OFF : Normal operation takes place.
T13	OSC CONT TEST	ON $\boxed{\text{OFF}}$	This test function enables the operation of the audio bias/erase oscillator to be controlled. It is used for checking the recording section of the audio system without using a tape. ON : The audio bias oscillator operates. OFF : Normal operation takes place.
T14	VIDEO REC OFF TEST	ON $\boxed{\text{OFF}}$	Used to operate the VIDEO/SYNC rotary erase alone in the STOP mode. ON : The VIDEO/SYNC erase head operates in the STOP mode. OFF : Normal operation takes place.
T15	CONFI TEST	ON $\boxed{\text{OFF}}$	This test function is used to check the audio monitor head. It enables the playback signals from the audio monitor head to be output from the MONITOR OUTPUT R/L connectors in the PLAY mode. ON : By entering the PLAY mode when the TAPE lamp on the 21-key is lit, the playback signals from the audio monitor head will be output to the MONITOR OUTPUT R/L connectors. OFF : The playback signals from the audio monitor head will be output to the MONITOR OUTPUT R/L connectors only in the REC and EDIT mode.
T16	VIDEO TEST	ON $\boxed{\text{OFF}}$	This test function enables the video recording system to be operated in the STANDBY OFF and STOP modes. It is used to check the recording circuits. ON : The recording system can be operated even when the drum is stationary. OFF : Normal operation takes place.

<table>
<tr><th>MENU No.</th><th>MENU</th><th>ITEMS</th><th>DESCRIPTION</th></tr>
<tr><td>T17</td><td>MAINTENANCE</td><td>OFF (boxed)
TTP ADJ
PANEL
VERSION
EXTEND</td><td>Enables the control panel and also the servo system to be checked. For details, refer to Sec. 3-3.
OFF : Testing does not take place.
TTP ADJ : The tape transport system can be checked or adjusted.
PANEL : The control panel can be checked. Use this function to check the indicator lamps and keys, and also to check the version of the software used in the control panel.
VERSION : The software version of the SY, SV and RD boards are displayed on the control panel.
EXTEND : The extension menu mode is selected.</td></tr>
<tr><td>T18</td><td>SPECIAL REEL MODE</td><td>ON
OFF (boxed)</td><td>Used to wind tape onto a spot reel in order to make a spot reel tape. (NOTE : When a spot reel is played back, it is unnecessary to select this menu.)
ON : Enables tape to be wound onto a spot reel. The tape speed is limited to 20 times speed.
1. Wind tape on to a take-up reel.
2. Set this menu (T18) to ON. 1)
3. Replace the S-reel with a spot reel.
4. Thread the tape to the S-reel from the T-reel.
5. Set the VTR to the REWIND mode to take up the tape onto the spot reel.
6. Set the VTR to the STOP mode, then cut the tape nearby the spot reel.
7. Remove the spot reel.
8. Repeatedly perform step 3 to 7 to make the desired number of spot reel tapes.
9. Set this menu (T18) to OFF. 2)
OFF : Normal operation takes place.

1) The followings are two methods for set the menu (T18) to ON.
1. According to operating flow (Sec. 3-3) of test menu, set this T18 to ON.
2. Push the SHUTTLE button while push on the STOP button. In this case, it will be set to the SETUP mode automatically, and indicate "T18. SPECIAL REEL MODE" "ON" on menu display. This indication is the same display when compare the item 1 and this item 2.

2) When set to off the menu (T18), according to operating flow of the test menu.
It has no special process when set to ON the T18.</td></tr>
</table>

3-3. MAINTENANCE MENU (T17. MAINTENANCE)

The T17. MAINTENANCE menu among the test menus is used for the tape transport and servo system adjustments and for the function control panel checks. One of the following three items is selected in accordance with the objective at hand.

T17. MAINTENANCE menu

OFF : No testing

TTP ADJ : This item is selected when checking and/or adjusting the tape transport and servo systems. See section 3-3-1.
Note : When the $\boxed{0}$ key in the 21-key section is pressed while the TEST switch S2 on the SY-103 board is kept depressed, direct entry is made into the TTP ADJ menu.

PANEL : This item is selected when conducting checks on the function control panel. See section 3-3-2.
Note : When the TEST switch S102 on the KC-14 board is pressed, direct entry is made into the PANEL menu.

VERSION : This menu is selected when checking the software version of the SY, SV and RD boards. See section 3-3-3.

EXTEND : This menu is selected to extend the menu. See section 3-3-4.

3-3-1. TTP ADJ Menu

The TTP ADJ menu under the T17. MAINTENANCE menu includes all the menus listed below.

Group C	C0.	TEST MODE OFF
	C5.	DAC ADJUST
	C68.	REF SCH GAIN
	C69.	REF SCH DATA
	C6A.	TAPE SCH DATA
	C70.	TEN SNS OFFSET
	C71.	TEN SNS GAIN
	C80.	TRACKING ADJ
	C81.	CTL ADJ
	C82.	OVERLAP CHECK
	C90.	PG ADJ
	CC0.	CAP SPEED ADJ
	CD.	DRUM SPEED ADJ
Group T	T0.	T0 0 START
	T1.	T1 ADJ&START
	T2.	T2 FULL CHECK
	T3.	T3 BRK CHECK
	T4.	T4 CCW BK ADJ
	T5.	T5 CW BK ADJ
	T8.	T8 0 START
	T9.	T9 ADJ&START
	TA.	TA FULL CHECK
	TB.	TB BRK CHECK
	TC.	TC CCW BK ADJ
	TD.	TD CW BK ADJ
Group F	F0.	F0 PINCH
	F1.	F1 GUIDE
	F2.	F2 MECHA
	F3.	F3 -----
	F4.	F4 DRUM
	F5.	F5 CAPSTAN
	F6.	F6 S-REEL
	F7.	F7 T-REEL
	F8.	F8 CFG ADJ
	F9.	F9 SFG ADJ
	FA.	FA TFG ADJ

<u>**Group C**</u>

The Group C menus are used for checking and adjusting the tape transport system while the tape is running. The settings required for the checks/ adjustments are performed automatically.

Menu C0. TEST MODE OFF
This is used to cancel the Group C menus. Refer to step ⑯ in the "Operation Sequence for the TTP ADJ Menu".

Menu C5. DAC ADJUST
This is used for section 10-3 servo D/A converter adjustment.

Menu C68. REF SCH GAIN
Menu C69. REF SCH DATA
These are used for section 13-14 reference SC-H adjustment.

Menu C6A. TAPE SCH DATA
This is used for section 14-15 (14-18 for PS) tape SC-H adjustment.

Menu C70. TEN SNS OFFSET
Menu C71. TEN SNS GAIN
These are used to calibrate the tape tension sensor. Refer to Section 9-2.

Menu C80. TRACKING ADJ
This is used for the tracking checks and adjustments. Refer to Sections 5-3 and 9-5. The settings are made as follows.

VIDEO HEAD :	R/P HEAD
ADVANCE :	OFF
AUTO PG :	OFF
WFM OUTPUT :	RF ENVELOPE
VIDEO MONITOR OUTPUT :	DEMOD OUT
FR PLS OUTPUT :	REF 2
PLAY MODE :	1.5 HEAD

Menu C81. CTL ADJ
This is used to adjust the CTL head position. Refer to Section 9-6. The settings are made as follows.

VIDEO HEAD :	R/P HEAD
ADVANCE :	OFF
AUTO PG :	ON
WFM OUTPUT :	RF ENVELOPE
VIDEO MONITOR OUTPUT :	DEMOD OUT
FR PLS OUTPUT :	REF 2
PLAY MODE :	1.5 HEAD

Menu C82. OVERLAP CHECK
This is used to check and adjust the overlap of the RF waveforms. Refer to Section 9-8. The settings are made as follows.

VIDEO HEAD :	R/P HEAD
ADVANCE :	OFF
AUTO PG :	ON
WFM OUTPUT :	SELECT
VIDEO MONITOR OUTPUT :	DEMOD OUT
FR PLS OUTPUT :	REF 2
PLAY MODE :	1.5 HEAD

Menu C90. PG ADJ
This is used to adjust the PG phase. Refer to Section 9-7. The settings are made as follows.

VIDEO HEAD :	R/P HEAD → PLAY HEAD
ADVANCE :	OFF
AUTO PG :	OFF
WFM OUTPUT :	SELECT
VIDEO MONITOR OUTPUT :	DEMOD OUT
FR PLS OUTPUT :	REF 2
PLAY MODE :	1.5 HEAD

Menu CC0. CAP SPEED ADJ
This is used to adjust the tape speed. Refer to Sections 6-9 and 9-4. The settings are made as follows.

VIDEO HEAD :	R/P HEAD
ADVANCE :	ON
AUTO PG :	ON
WFM OUTPUT :	CTL
VIDEO MONITOR OUTPUT :	DEMOD OUT
FR PLS OUTPUT :	REF 2
PLAY MODE :	1.5 HEAD

Menu CD. DRUM SPEED ADJ
This is used to adjust the drum speed. Refer to Section 6-2-1. The settings are made as follows.

VIDEO HEAD :	R/P HEAD
ADVANCE :	ON
AUTO PG :	ON
WFM OUTPUT :	SELECT
VIDEO MONITOR OUTPUT :	DEMOD OUT
FR PLS OUTPUT :	REF 2
PLAY MODE :	1.5 HEAD

Group T
The Group T menus are used to adjust the torques of the reel motors and reel brakes without a tape having been threaded.
The test mode is canceled by pressing the S3 RESET switch on the SV-90 board or setting the power switch to OFF and then back to ON again.

Menu T0. T0 0 START
Menu T1. T1 ADJ&START
Menu T8. T8 0 START
Menu T9. T9 ADJ&START
These are used to measure and adjust automatically the reel motor torque. At menu T0, a voltage is supplied to the supply reel motor for generating a torque of 2 kg-cm, and the actual torque generated by this motor is measured. Upon completion of the measurement the motor stops. At menu T1, the drive voltage of the supply reel motor is adjusted based on the data measured with T0 and the torque is measured again. Upon completion of the measurement the motor stops. Menus T0 and T1 are for the supply reel motor. Refer to Section 6-5-1.
Menus T8 and T9 are for the take-up reel motor. Refer to Section 6-5-2.

Menu T2. T2 FULL CHECK
Menu TA. TA FULL CHECK
Voltages are supplied to the reel motor for generating torques of 1, 2, 4 and 8 kg-cm, and the torques which are actually generated by the reel motor are automatically measured. Upon completion of the measurement the motor stops automatically. Menu T2 is for the supply reel motor and menu TA for the take-up reel motor.

Menu T3. T3 BRK CHECK
Menu TB. TB BRK CHECK
The mechanical brake torque of the reel tables is automatically measured in both the clockwise and counterclockwise directions. Upon completion of the measurement the motor stops automatically. Menu T3 is for the supply reel table and menu TB for the take-up reel table. Refer to Section 6-5-2.

Menu T4. T4 CCW BK ADJ
Menu T5. T5 CW BK ADJ
Menu TC. TC CCW BK ADJ
Menu TD. TD CW BK ADJ
The mechanical brake torque of the reel tables is automatically measured. Menus T4 and TC are for counterclockwise rotation and menus T5 and TD are for clockwise rotation. Even when the measurement is completed, the reel motors will still continue to turn. Menus T4 and T5 are for the supply reel table and menus TC and TD for the take-up reel table. Refer to Section 6-5-1.

Group F

The Group F menus are used to check and adjust the tape transport without a tape having been threaded.
The test mode is canceled by pressing the S3 RESET switch on the SV-90 board or setting the power switch to OFF and then back to ON again.
Note : The functions of the [F0], [F1], [F2] and [F3] keys are based on the following key operations.
- [F0] key : Press the [7] key with the blue [OUT] key kept depressed.
- [F1] key : Press the [8] key with the blue [OUT] key kept depressed.
- [F2] key : Press the [9] key with the blue [OUT] key kept depressed.
- [F3] key : Press the [TAPE/IN] key with the blue [OUT] key kept depressed.

Menu F0. F0 PINCH
When this menu is entered, the capstan rotates and the pinch roller will be pressed against the capstan as below, depending on the operation of the following keys.
When the [F0] key is pressed, the pinch roller is pressed against the capstan.
When the [F1] key is pressed, the pinch roller moves away from the capstan.
When the [F2] key is pressed, the pinch roller will be pressed against the capstan for as long as the key is kept depressed.
This menu is used to adjust the pinch roller pressure. Refer to Sections 6-9, 6-10 and 6-11.

Menu F1. F1 GUIDE
When this menu is entered, the moving guide opens and closes as indicated below.
When the [F0] key is pressed, the moving guide opens fully.
When the [F1] key is pressed, the moving guide closes fully.
When the [F2] key is pressed, the moving guide opens halfway.
While the [F3] key is kept depressed, the threading motor is made operational and the moving guide repeatedly opens and closes.

Menu F2. F2 MECHA
This menu enables the operation of the S/T blowers, S/T reel brake solenoids and IP roller motor to be checked.
When the [F0] key is pressed, the S blower will operate for as long as the key is kept depressed.
When the [F1] key is pressed, the T blower will operate for as long as the key is kept depressed.
When the [F2] key is pressed, the S and T reel brake solenoids will be energized (the reel brakes will be released) for as long as the key is kept depressed.
When the [F3] key is pressed, the IP roller motor will operate for as long as the key is kept depressed.

Menu F3. F3 -----
This stops the motors which are operating and releases the solenoids. When adjustments have been made using the F8, F9 and FA menus, the motors will be stopped by menu F3. Refer to step ⑫ in the "Operation Sequence for the TTP ADJ Menu".

Menu F4. F4 DRUM
Menu F5. F5 CAPSTAN
Menu F6. F6 S-REEL
Menu F7. F7 T-REEL

At these menus, the drum motor, capstan motor, supply reel motor and take-up reel motor can be operated at high or low speed and in the clockwise or counterclockwise direction.

The speed and direction of the rotation are as below:

While the [F0] key is kept depressed:
High speed, CCW rotation

While the [F1] key is kept depressed:
Low speed, CCW rotation

While the [F2] key is kept depressed:
Low speed, CW rotation

While the [F3] key is kept depressed:
High speed, CW rotation

Menu F8. F8 CFG ADJ
Menu F9. F9 SFG ADJ
Menu FA. FA TFG ADJ

At these menus, the FG duty cycles of the capstan motor, supply reel motor and take-up reel motor are adjusted.

When the [F3] key is pressed, adjustment is conducted automatically for as long as the key is kept depressed. Upon completion of the adjustments, the motors are stopped by menu F3. Refer to Sections 6-9 and 9-4 for menu F8, Section 6-5-1 for menu F9 and Section 6-5-2 for menu FA.

Operation Sequence for the TTP ADJ Menu

Steps ① through ④ below allow entry into the test menus and the subsequent steps up to ⑨ allow entry into the TTP ADJ menu. Instead of proceeding with steps ① through ⑨, the TTP ADJ menu can also be entered by pressing the [0] key in the 21-key section while TEST switch S2 on the SY-103 board is kept depressed.

①Press the [SET UP] key. The OPERATION MODE SELECT menu is automatically selected.

②Push the [C] key to select the HOME menu.

③Press the [–] key to select TEST.

④Press the [SET] key to establish the test menu.
(Note) The last selected menu is displayed.

Display

SELECT MODE ENABLE	

SET UP MODE	SELECT SELECT

	SELECT TEST

T01. TEST CHARA DISPLAY OFF

Note: The shaded area of the display is not related to the menu selection. The contents of this display are determined by the VTR operation.

⑤The number of the desired menu is assigned using the [0] through [9], [+] and [−] keys or Search Dial. For instance, T17 is selected by keying in [1] and [7].

T17. MAINTENANCE	OFF

⑥Press the [SET] key to establish the menu number selection.

T17. MAINTENANCE	OFF	OFF

⑦Select TTP ADJ using the [+] and [−] keys or Search Dial. (Select PANEL if the PANEL menu is to be entered.)

T17. MAINTENANCE	OFF TTP ADJ

⑧Press the [SET] key.

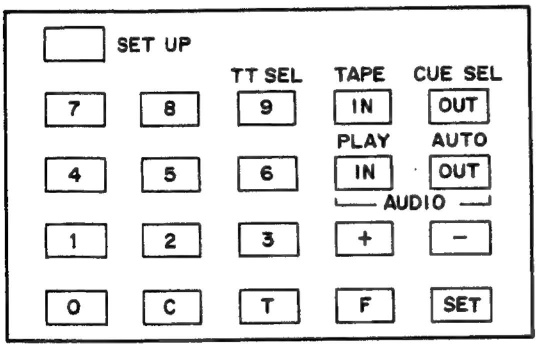
	>_

⑨Press the [SET] key again to establish the TTP ADJ selection.
The TTP ADJ menu is now entered.

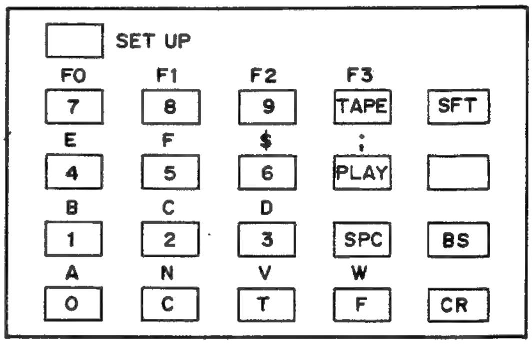
	>?_
	>_

Entry into the TTP ADJ menu causes the functions of the keys in the 21-key section to be changed, as indicated below.

Normal mode



TTP ADJ mode



[SFT] is the shift key. When, for instance, the [T] key is pressed with the [SFT] key already depressed, the result is the same as if the [V] key had been pressed.
[CR] is the carriage return key.

The adjustments and checks are now conducted.
The description below uses [C90. PG ADJ] as an example.

⑩Key in [C], [9] and [0], and press the [CR] (SET) key.
C90. PG ADJ is now selected.

>C90	>PG ADJ
XXXX XXXX XXXX	

⑪Proceed with the adjustment. Depending on the item, adjustment is made automatically.

⑫When [F8. CFG ADJ], [F9. SFG ADJ] or [FA. TFG ADJ] has been selected, key in [F] and [3] and press [CR] (SET). The motor which was operating now stops.

	>F8 CFG ADJ
	>_

>F8 CFG ADJ	>F3 STOP
	>_

Now continue with steps ⑬, ⑭ and ⑮ in order **to write the results of the adjustments into the NOVRAM** (non-volatile random access memory).
Skip these steps and proceed straight to step ⑯ if there is no need to write the results into the NOVRAM.

⑬Press [C], [T] and [F] in sequence while keeping the [SFT] (OUT) key depressed. This has the same result as if [N], [V] and [W] had been keyed in. Now press the [CR] (SET) key.

	>NVW

	>NVW
	>XXXX XX-XX_

⑭Keep the [+] key depressed. The display will appear as shown in the figure on the right.

	>PUSH NVWR SW

⑮Press the NVWR switch S2 on the SV-90 board.

>XXXX-XX	>READY_
	>_

These operations save the adjustment data into the NOVRAM. Next, proceed with the operation **to cancel the test mode.** To cancel a Group C menu, proceed to step ⑯. To cancel a Group F menu, proceed to step ⑲.

⑯Press [C], [0] and [CR] (SET) in sequence. In this state, it is now also possible to proceed to step ⑩ again.

>C0	>TEST MODE OFF
	>_

⑰Press the [SET] key while keeping the blue [OUT] key depressed. In this state, it is now also possible to proceed to step ⑤ again.

⑱Press the [SET UP] key or perform any operation of step ⑲. This operation causes a return to the normal operating mode.
If the [C] key is pressed instead of the [SET UP] key, it causes a return to the state after operating step ②.

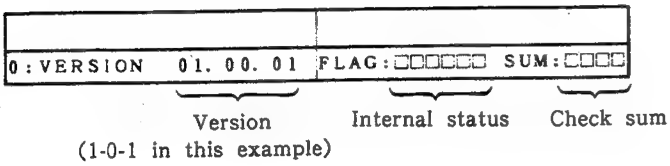
⑲The operation is completed by any of the following.
- Press the S3 RESET switch on the SV-90 board.
- Set the power switch to OFF and then back to ON again.

This operation causes a return to the normal operating mode. It is possible in any mode to perform this operation.

3-3-2. PANEL Menu

The following menus are included in the PANEL menus of the T17. MAINTENANCE menu. These enable tests on the function control panel to be conducted.

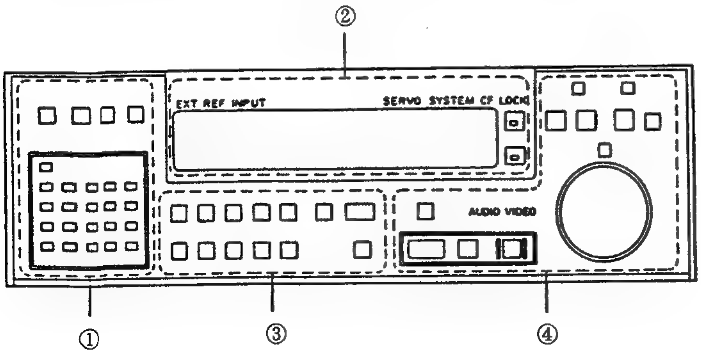
Menu 0: VERSION
The software version of the function control panel and check sum, etc., will be displayed as follows.

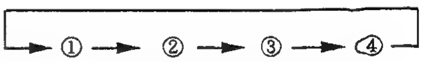


Menu 1: ALL DOT
All dots on the display will light.

Menu 2: ALL CHR
All characters on the character generator will appear on the display as shown below.

Menu 3: LMP TST
The lamps on the function control panel will be checked. Blocks of lamps light successively at intervals of about 2 seconds, as follows. When the [+] key is pressed, the unit will go into the mode whereby the lit blocks shift each time the [+] key is pressed.

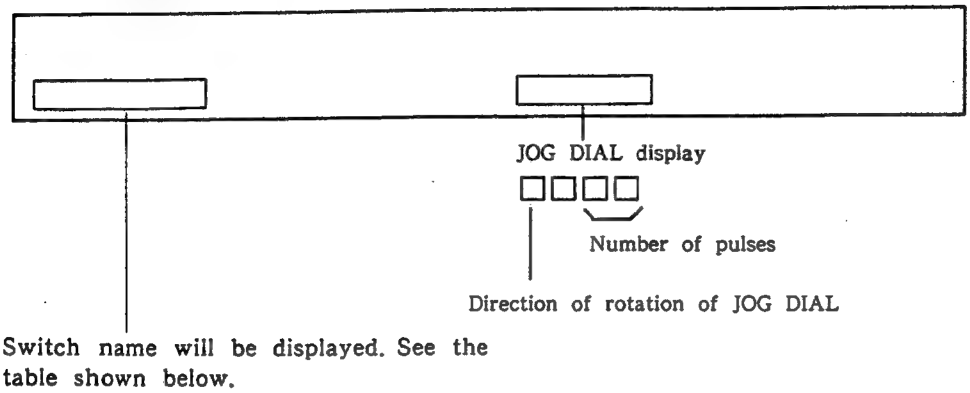




Lamps light successively.

Menu 4 : KEY

When a switch on the control panel is pressed, the name corresponding to that switch will be displayed. Simultaneously, the number of pulses and direction data will be displayed in accordance with the rotation of the JOG DIAL.



No.	Switch name	Display	No.	Switch name	Display
1	STOP	STOP	26	SPOT ERASE	SPOT ERS
2	PLAY	PLAY	27	INPUT	INPUT
3	REC/EDIT	REC	28	0 (21key)	0
4	VAR	VARIABLE	29	1 (21key)	1
5	VAR MEMORY	VR MMRY	30	2 (21key)	2
6	JOG	JOG	31	3 (21key)	3
7	SHUTTLE	SHUTTLE	32	4 (21key)	4
8	STANDBY	STANDBY	33	5 (21key)	5
9	PREROLL/SEARCH	PREROLL	34	6 (21key)	6
10	PREVIEW/REVIEW	PREVIEW	35	7 (21key)	7
11	CUE ENTRY	CUE ENT	36	8 (21key)	8
12	RESET	RESET	37	9 (21key)	9
13	DISPLAY HOLD	HOLD	38	C (21key)	C
14	VIDEO IN	VIDEO IN	39	T (21key)	T
15	VIDEO OUT	VD OUT	40	F (21key)	F
16	AUDIO SPLIT IN	AD SPL I	41	+ (21key)	+
17	AUDIO SPLIT OUT	AD SPL O	42	− (21key)	−
18	AUDIO SPLIT	AD SPL	43	SET (21key)	SET
19	AUDIO 1	AUDIO 1	44	IN (21key)	VIDEO IN
20	AUDIO 2	AUDIO 2	45	AUDIO IN (21key)	AUDIO IN
21	AUDIO 3	AUDIO 3	46	OUT (21key)	VIDEO O
22	AUDIO 4/SYNC	AUDIO 4	47	AUDIO OUT (21key)	AUDIO O
23	VIDEO	VIDEO	48	SET UP (21key)	SET UP
24	ASSEMBLE	ASSEMBLE	49	CONTROL P	CTRL-P
25	INSERT	INSERT	50	CONTROL R	CTRL-R

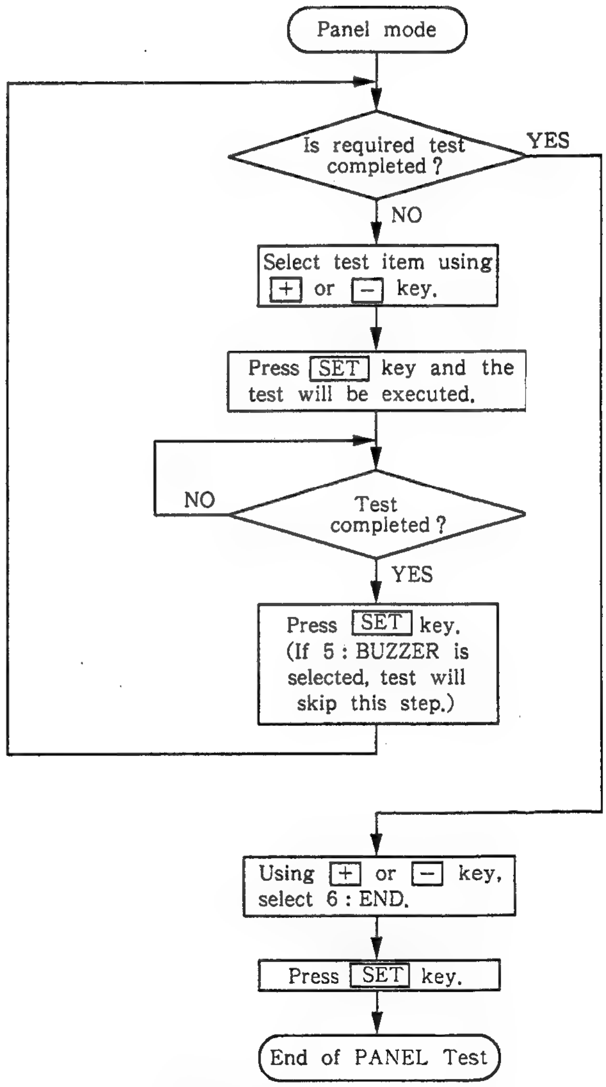
Menu 5 : BUZZER
A beep tone will be emitted 8 times. By pressing the [SET] key, the test can be performed again.

Menu 6 : END
The PANEL mode will end.

Menu 7 : MONITOR
Used to check the memories of the control panel and so on. Not normally used.
When the menu has been selected, cancel it by the following key operations.
[SET] → [9] → [SET]
After the operations, [7 : MONITOR] will be displayed on the control panel.

Operation Sequence for the PANEL Menu

The test menu and then also the PANEL menu can be entered using the same key operations as for entry into the TTP ADJ menu. Simply select [PANEL] instead of [TTP ADJ] in step ⑦ of the above-mentioned "Operation Sequence for the TTP ADJ Menu", and the PANEL menu will be entered when steps ① through ⑨ are carried out.
Direct entry into the PANEL menu is made by pressing the TEST switch S102 on the KC-14 board.



By pressing [SETUP] key, unit will return to normal operating mode.

3-3-3. VERSION Menu

The software version of the SY, SV and RD boards is displayed on the control panel by the VERSION menu under the T17. MAINTENANCE menu.

Ex.

```
SY=2-0-0  SV=2-0-0  SB=2-0-0  RD=2-0-0
```

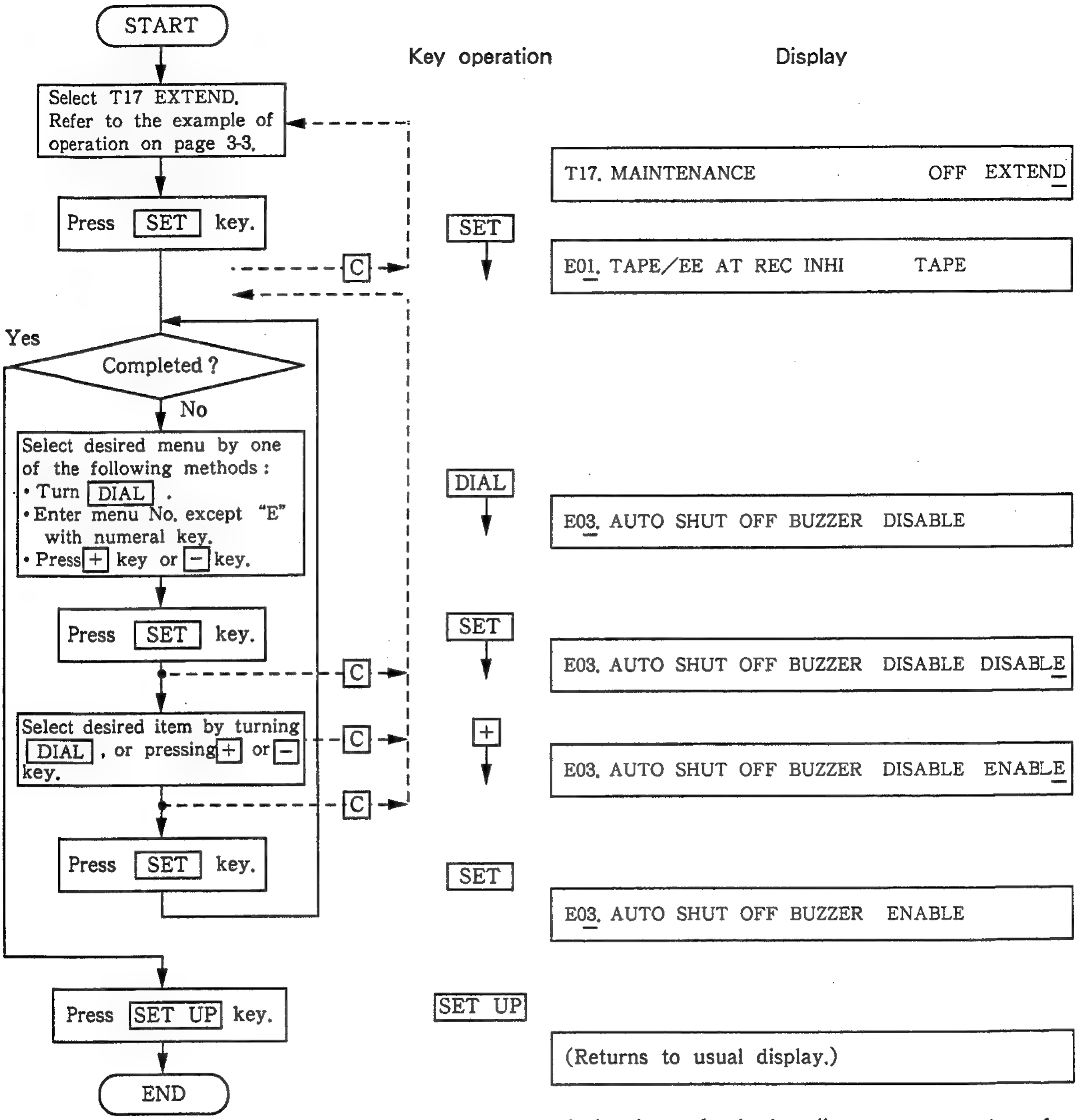
[SY=2-0-0] shows that the version 2-0-0 program is written onto ICH12 and H11 on the SY-103 board.
[SV=2-0-0] shows that the version 2-0-0 main program is written onto ICN5 and N3 on the SV-90 board.
[SB=2-0-0] shows that the version 2-0-0 sub program is written onto ICE15 on the SV-90 board.
[RD=2-0-0] shows that the version 2-0-0 program is written onto ICL15 on the RD-6 board (ICM14 on the RD-7 board for the PS model).

Press the $\boxed{C}$ key under the VERSION menu to return to the state in which the T17. MAINTENANCE menu is set to OFF.

3-3-4. EXTEND Menu

The items shown below are selectable in the EXTEND menu under the T17. MAINTENANCE menu. After the test menu is canceled, the each menu keeps the item selected in the EXTEND menu.

MENU No.	MENU	ITEMS
E01	TAPE/EE AT REC INHI	$\boxed{\text{TAPE}}$ EE
E02	CF LOCK ERROR DISP	$\boxed{\text{DISABLE}}$ ENABLE
E03	AUTO SHUT OFF BUZZER	$\boxed{\text{DISABLE}}$ ENABLE
E04 (NTSC only)	C-ADD	$\boxed{\text{ON}}$ OFF
E05	BINARY GROUP FLAG	ISO $\boxed{\text{BINARY}}$
E06	TC COLOR FRAME CONT	$\boxed{\text{VTR}}$ ON OFF
E07	REC INHI STATUS	OR $\boxed{\text{AND}}$
E08 (NTSC only)	CONFI SYNC DELAY	DISABLE $\boxed{\text{ENABLE}}$
E09 (PS only)	SECAM ID	$\boxed{\text{ON}}$ OFF
E10	HOLD UB SENSE RETURN	$\boxed{\text{DISABLE}}$ ENABLE
E11	REM2A/REM3 PARA MODE	$\boxed{\text{DISABLE}}$ ENABLE
E12	CF DETECT WINDOW	$\boxed{\text{+- 70}}$ +- 40 +- 20



*1. As shown by broken lines, you can return to the previous step by pressing [C] key. However, the selection finalized by pressing [SET] key cannot be canceled by this means.

SONY

VIDEOCORDER

BVH-3000PS
BVH-3100PS

SUPPLEMENT-4

SUBJECT

Addition and Replacement of Documents

APPLICABLE MANUALS/SERIAL NUMBERS

BVH-3000PS/3100PS MAINTENANCE MANUAL
Volume-1 1st Edition
1st Edition (Revised 1 thru Revised 4)
Above manuals are packed with the following machines.
BVH-3000PS # 10001 thru 10999
BVH-3100PS # 10001 thru 11799

MAINTENANCE MANUAL

BVH-3000PS (EK)
BVH-3100PS (EK)
9-966-968-10

Sony Corporation

Printed in Japan
1988 08 09

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5. PERIODIC CHECK AND MAINTENANCE

6. PARTS REPLACEMENT

SECTION 4
THEORY OF OPERATION

4-1. OUTLINE

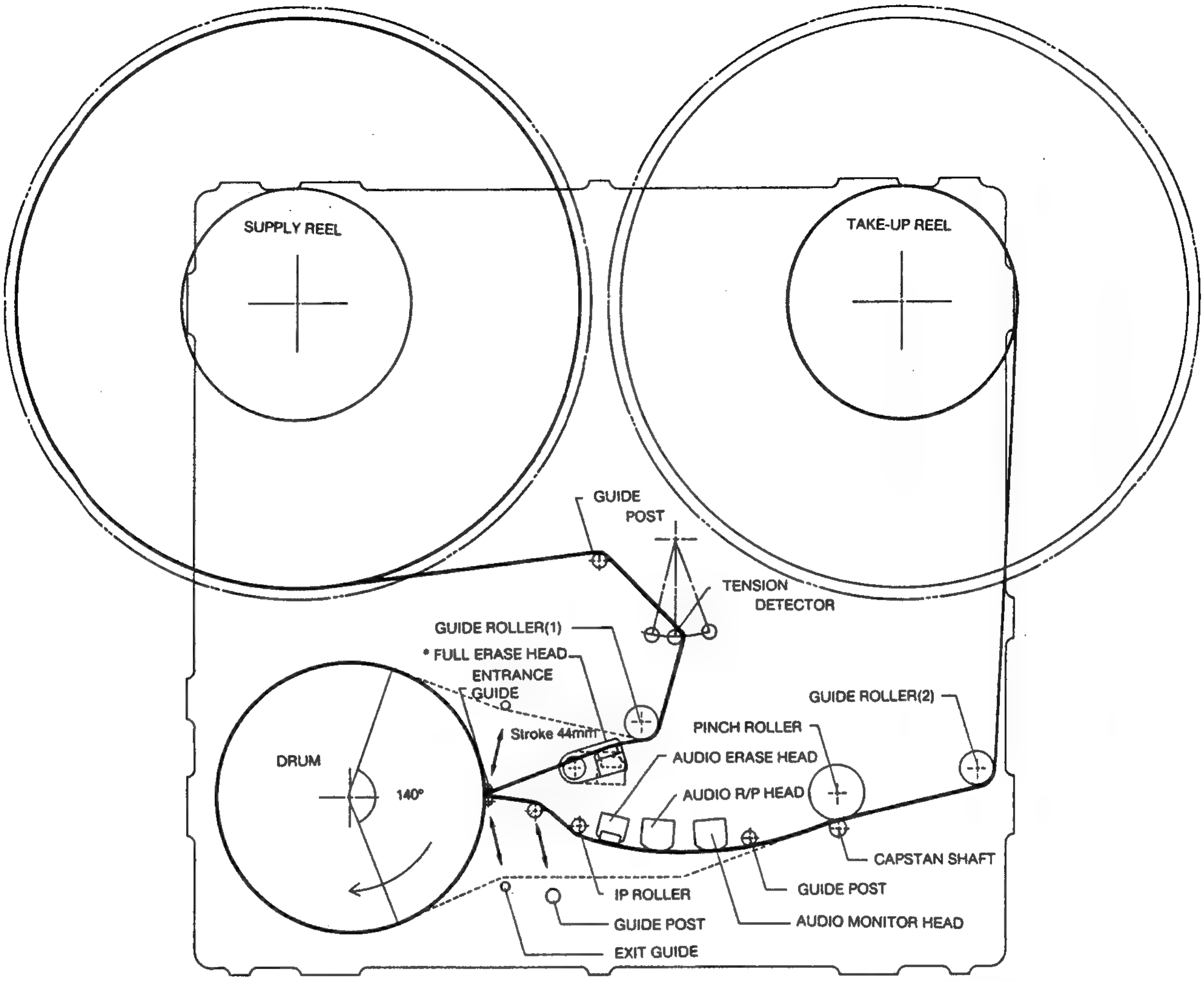
The BVH-3000/3100 is a direct high band FM recording 1-inch helical scan VTR based on the SMPTE type C format (or the EBU type C format in the case of a PAL/SECAM model). The only difference between the BVH-3000 and the BVH-3100 is that the former has a sync head whereas the latter does not.
The PAL/SECAM model is also available with 4-channel audio tracks.

		Sync head	Audio channels
NTSC	BVH-3000	Yes	3
	BVH-3100	No	3
P/S	BVH-3000PS	Yes	3
	BVH-3100PS	No	3
	BVH-3000PS-A4	Yes	4
	BVH-3100PS-A4	No	4

An air threading system employing moving guides, blowers, and a dedicated reel is used, greatly simplifying tape threading.
The timer roller and the take-up side tension arm have been removed from the tape transport system for ease of maintenance. Refer to Fig. 4-1-1.
Figure 4-1-2 shows the tape pattern for the NTSC model, and Fig. 4-1-3 shows the tape pattern for the PAL/SECAM model.

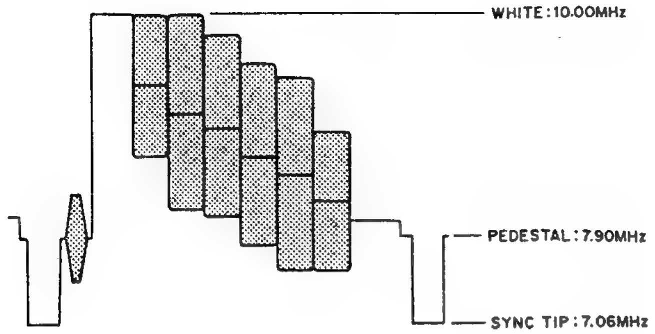
The BVH-3000/3100 system is controlled by the CPU. The entire setup procedure from setting the system conditions to setting the test mode can be done by making menu selections using the keys on the control panel. The CPU controls communication with the control panel and external devices, controls the system control circuit, and servo circuits (S reel, T reel, capstan, and drum), and also controls the audio, video, and TBC circuit mode according to the system control circuit, servo circuit, and menu settings. An RS-422 serial interface is provided for communication between the system and external control equipment. By using an optional BKH-3002, serial communication can also be done with an RS-232C interface.

The BHV-3000/3100 is provided with a simultaneous playback function and a DT (dynamic tracking) function. The video PLAY head is a DT head. The DT head uses an auto jump control function, permitting stable and noiseless playback between −1 and +3 times normal speed.
The SC-H phase of the tape signal and reference signal is displayed on the front panel. This enables the continuity of the video signal at the editing point to be checked prior to editing. (In the case of an NTSC model, the BHV-3000/3100 outputs the video signal at an SC-H phase which matches the RS-170A. Also, if the SC-H phase of the input signal matches the RS-170A, color framing adjustment is unnecessary.)
The TBC processor can select either a standard processor BKH-3010/PR-91 board or a higher performance BKH-3050/PR-96 board (in the case of a PAL/SECAM model, the BKH-3020/PR-92 board or the BKH-3060/PR-98 board). The BKH-3050 (BKH-3060) uses a new Y addition method to improve the up and down motion of the screen and also flicker, during DT playback.
The TBC circuit has a field freeze function for preventing tape damage during still playback.
By adding a BKH-3080 (NR-26 board), audio channels 1 and 2 will become Dolby A or Dolby SR noise reduction systems.
The generator/reader of the time codes (LTC and VITC) is built into the unit.



*FULL ERASE HEAD FOR NTSC MODEL
V/S ERASE HEAD FOR PS MODEL

Fig. 4-1-1. Tape Transport



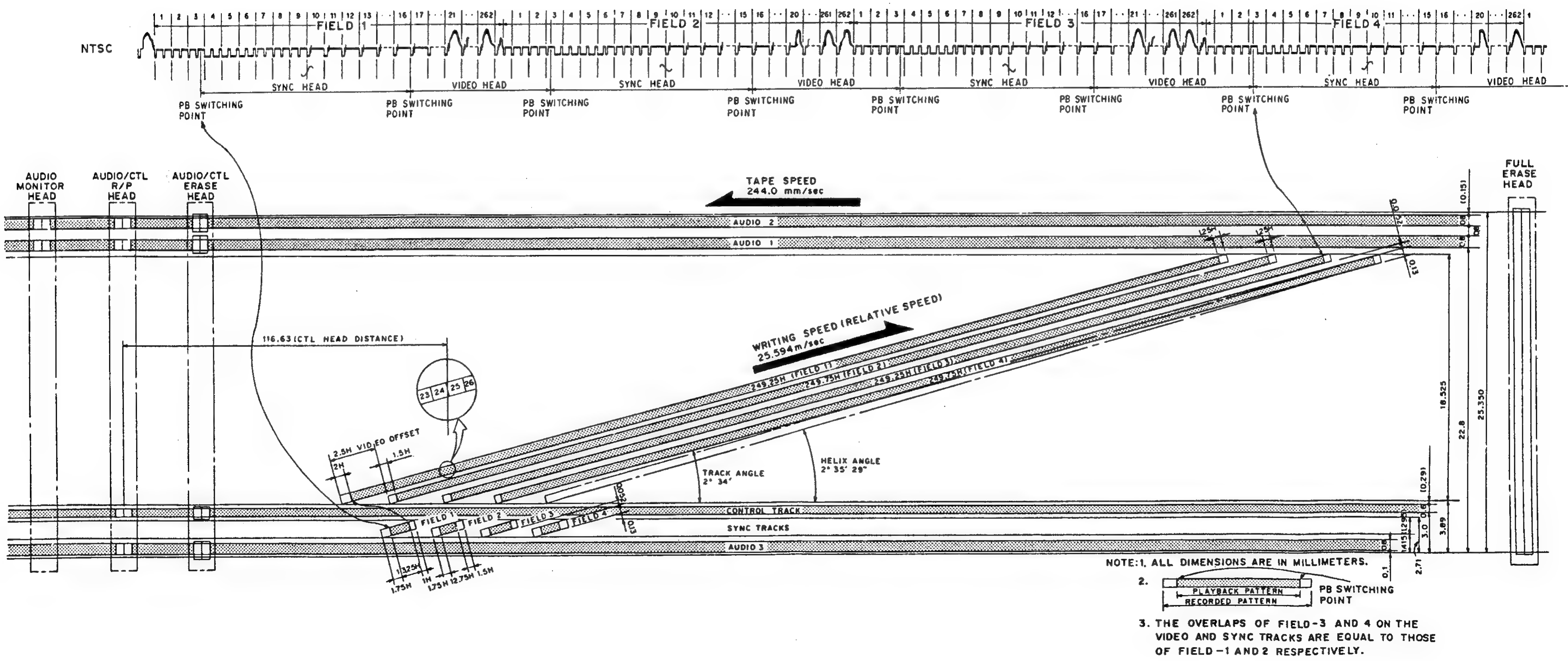


Fig. 4-1-2. NTSC Tape Pattern

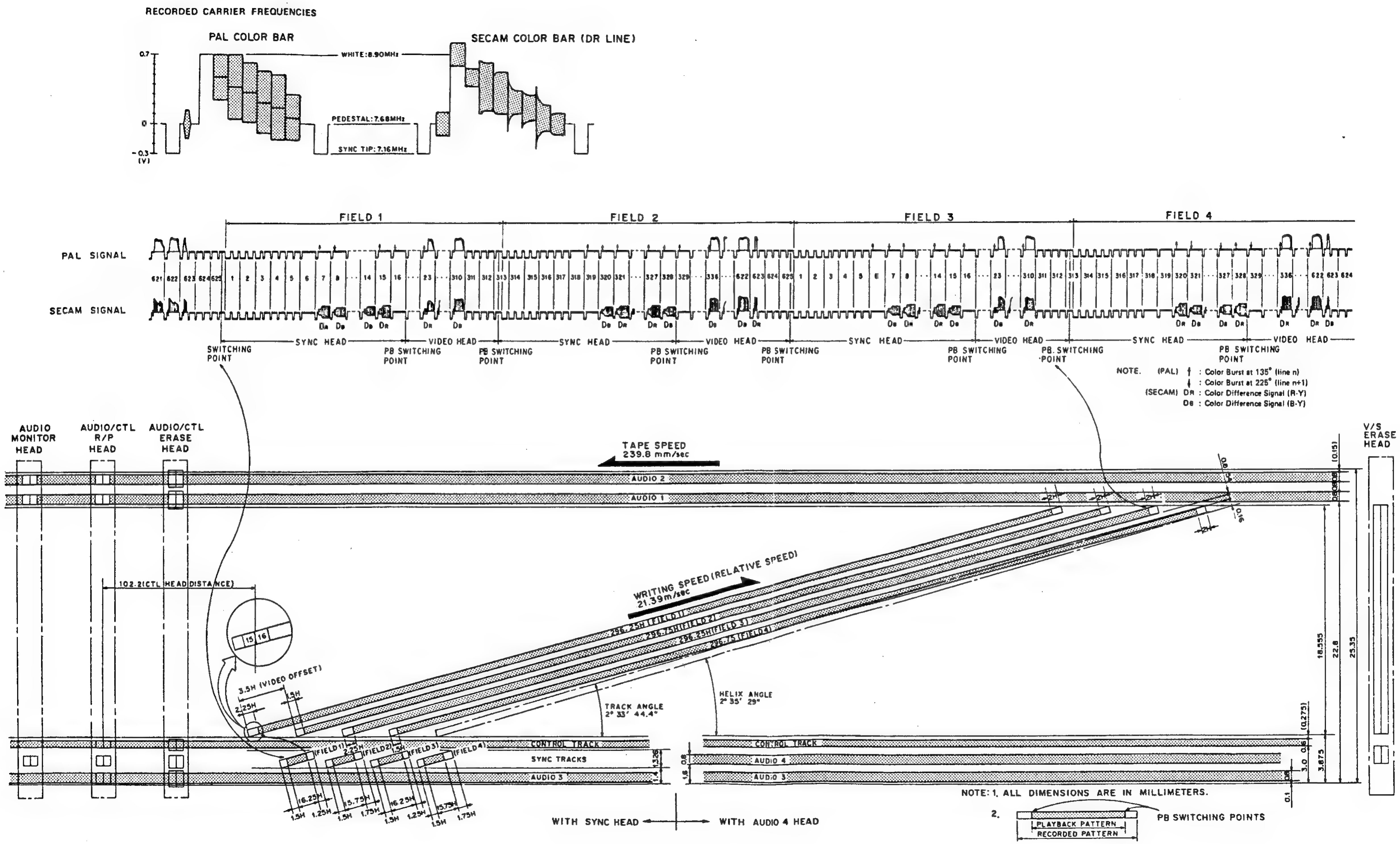


Fig. 4-1-3. PAL/SECAM Tape Pattern

4-2. AUDIO SIGNAL SYSTEM

4-2-1. Outline of Audio Signal System

The BVH-3000/3100 audio system has the following circuit configurations as described below.
The numbers of the audio channel are three channels of audio-1, 2 and 3 in the NTSC/PS model and are four channels of audio-1, 2, 3 and 4 in the PS A4 model.
The audio signal system consists of the record/playback circuit of each channel and the CONFI signal playback monitor circuit. But the CONFI playback is possible only in the two channels of audio-1 and 2 in the NTSC/PS model and in the three channels of audio-1, 2 and 4 in the PS A4 model. The bias and erase circuits which reqires during record mode are also included in this circuit.
The audio-3 channel has the LTC processing circuit that enables the time code signal's record/playback, in addition to the normal audio signal's record/playback circuit like other channels.
The BVH-3000/3100 audio circuit has the following features.

- The transformerless balanced input/output circuits are employed that realize the good low frequency response characteristics.
- The record and playback mode switching for the audio R/P head, is done by means of an electronic switch using FET, thus reliability of this circuit is improved and the on/off timing characteristics is also improved.
- The audio phase adjustment for the audio channel-1 versus channel-2 during record mode, is made possible that provides the high quality stereophonic recording.
- When the audio-1 and 2 mix mode is used, the phase difference between the both channels in the stereophonic mode can be easily confirmed.

The audio system of this equipment consists of the following five circuit boards. But the audio-4 is available exclusively only in the PS-A4 model.

(1) AU-88 board
The AU-88 board comprises the input amplifiers, output line amplifiers, record/playback equalizer circuits and also the input/output circuits that interface the various control signals, for all the audio-1, 2, 3 and 4 channels.
(2) AP-15 board
The AP-15 board comprises the record/playback amplifiers for the audio-1, 2, 3 and 4, the CONFI playback amplifiers for the audio-1, 2 and 4, the CTL record/playback amplifier and the bias/erase amplifiers for all channels.
(3) MA-26 board
The MA-26 board comprises the monitor-L and -R channel output amplifiers.
(4) VR-51 board
The VR-51 board comprises the record level adjustment circuit and the playback level adjustment circuit for all channels.
(5) BC-12 board
The BC-12 board has the bias level adjustment controls that are connected to the AP-15 board.

The record/playback circuits of the audio signals are mainly located in the AU-88 board that is housed in the amplifier chassis. The meter panel is including the VR-51 board, MS-21 board, SW-195 board and LP-34 board and is joined to the AU-88 board with screws. The AU-88 board, MA-26 board and AP-15 board are plugged into the mother board MB-140 for connections.

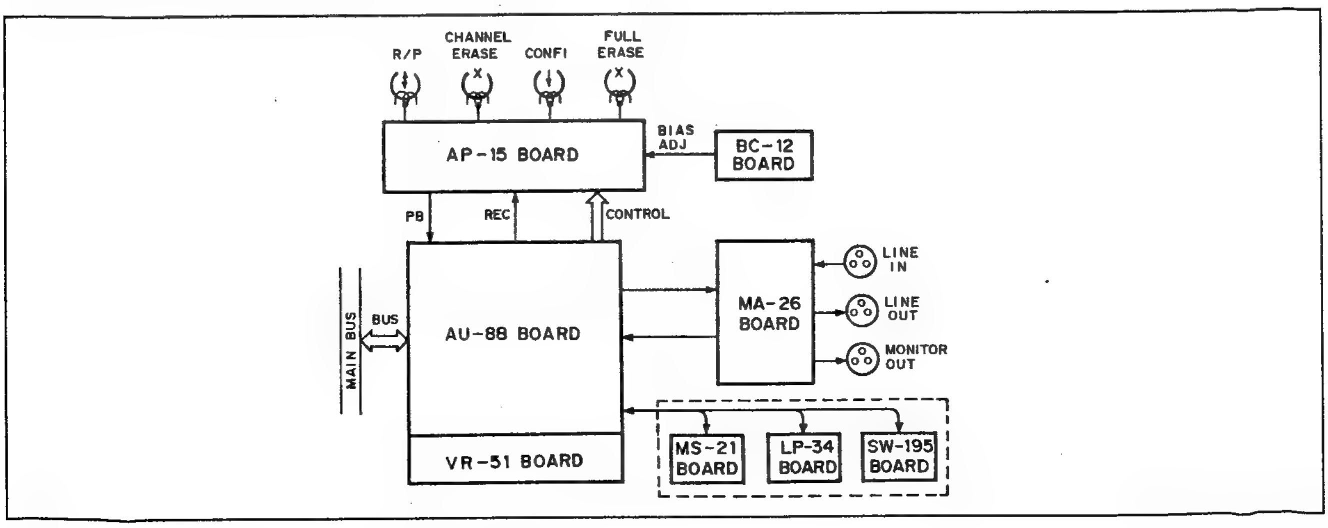


Fig. 4-2-1. Audio Signal System Configuration

The audio system has the following eight major circuit blocks. The circuit description is provided for each block by block.

(1) Audio signal record system
(2) Audio signal playback system
(3) Crosstalk canceller
(4) Audio monitor system
(5) Audio bias system
(6) Erase system
(7) Audio control signal system
(8) Time code system

4-2-2. Audio Signal Record System (AU-88, AP-15 Boards)

The signal flow of the audio signal record system, is shown in the Fig. 4-2-2.
The audio input signal that is fed to the LINE INPUT connector, passes through the MA-26 board and the MB-140 board, and is then sent to the AU-88 board where proper input level and input impedance are selected and the balanced input is converted to the unbalanced input. The input signal is then sent to the Input Level Control circuit (VR-51 board). The signal passes through the TAPE/EE switch, receives the record level adjustment and the equalizer adjustment, passes through the crosstalk canceller, and is then sent to the AP-15 board's record amplifier.
The audio record signal input at the AP-15 board, passing through the record amplifier and bias trap. The audio signal and the recording bias are added together and are then sent to the audio R/P head.

(1) Input circuit (AU-88 board)

Because the audio-1, 2, 3 and 4 have all the same circuit configurations, the audio-1 only is described. The circuit is shown in Fig. 4-2-3.
The signal is input to IC103 as the balanced signal that is converted to the unbalanced signal by IC104. C177 and C178 are the capacitors that reject the dc offset component in the input signal.
Resistors R101 through R104 and R231 through R233, are prepared in order to match the input impedance of 10k Ω, 600 Ω and 150 Ω. The desired input impedance can be selected by the combinations of the soldering jumpers in this circuit and by combination of JP101 and JP102. Only the channel-3 can select the input impedance of 47k Ω.
Resistors R105 and R106, and diodes D101 through D104 are used for input protection of IC103. Resistors R109 and R110 are used to determine the amplification gain.
Fig. 4-2-4 shows the channel-3 circuit. Unlike the other channels, the channel-3 accepts the MIC input as well as LINE input so that an exclusive gain-up amplifier is added in channel-3 circuit that amplifies the MIC input signal.
When a MIC is selected by menu, IC505 is turned off so that IC504 becomes a high gain amplifier, enabling the use of microphone.

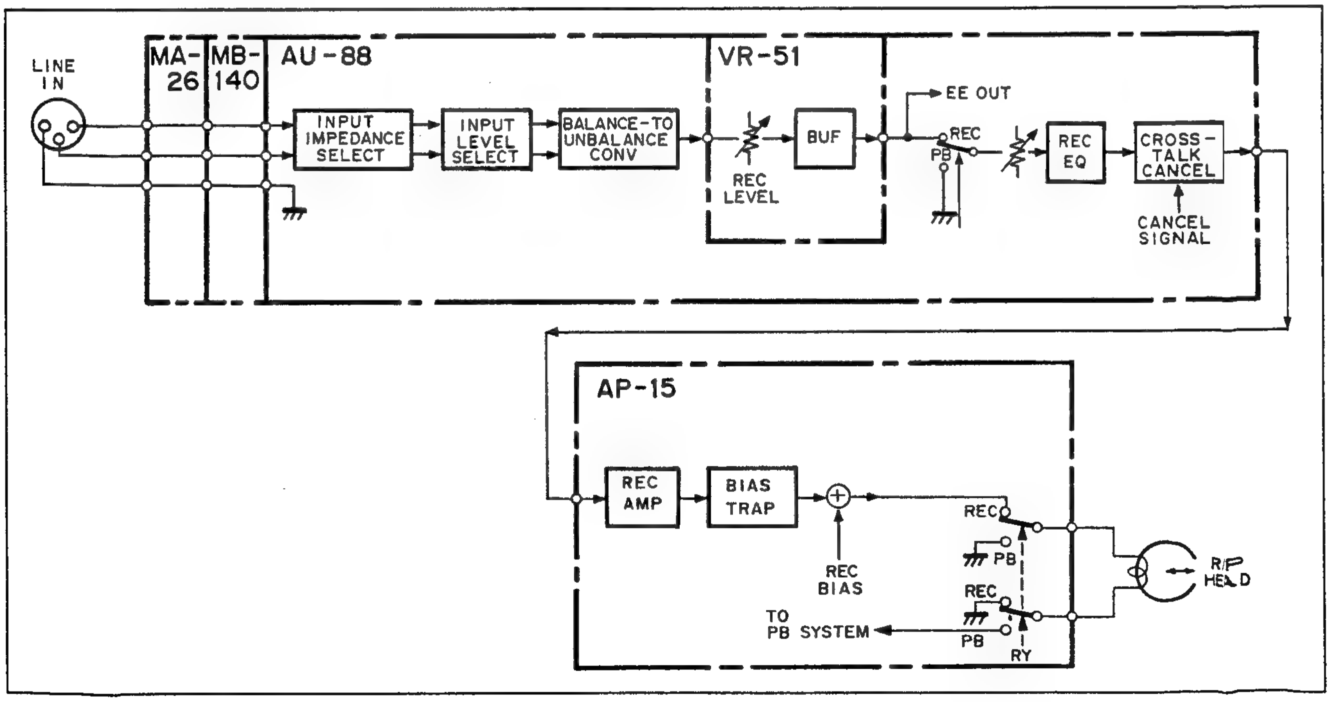


Fig. 4-2-2. Audio Signal Record System

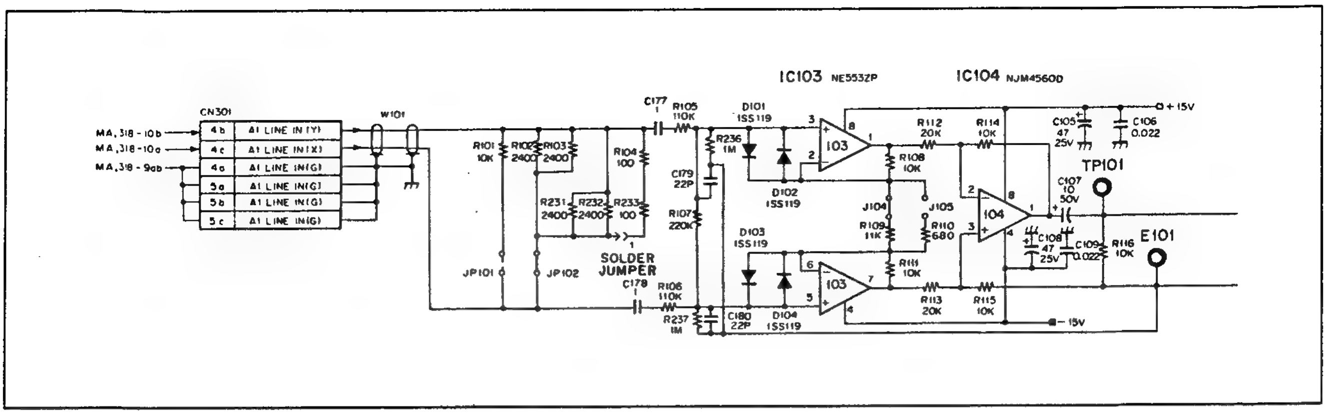


Fig. 4-2-3. Audio-1 Input Circuit (AU-88)

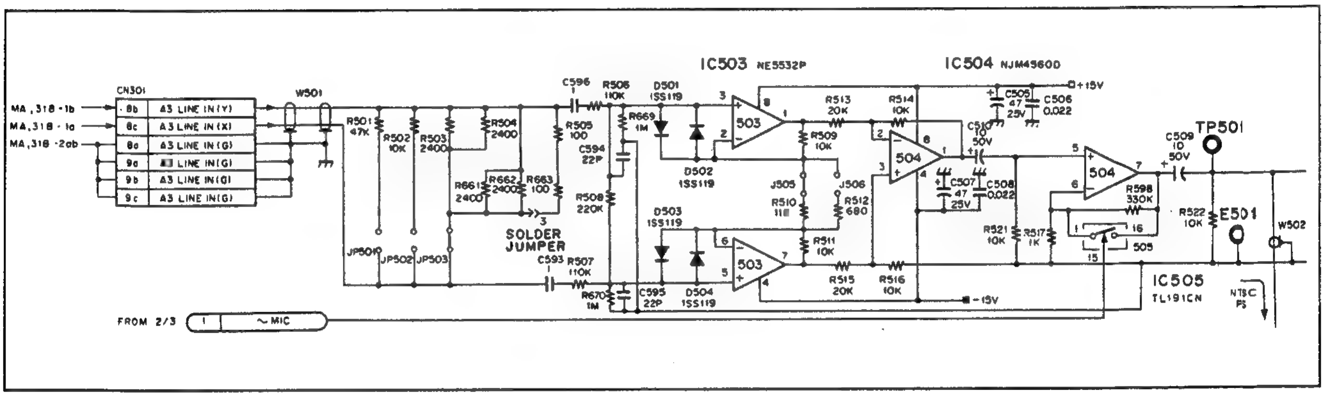


Fig. 4-2-4. Audio-3 Input Circuit (AU-88)

(2) Record/playback selector (AP-15 board)

The record/playback selection of the R/P head is accomplished by FET. Fig. 4-2-5 shows the fundamental circuit.
When the REC/PB signal is "L" level, meaning that the mode is record mode, Q1 is turned off while Q2 is turned on. So, the record amplifier's output signal is sent to the R/P head through the dc-cut capacitor, the constant current resistor and the bias trap circuit.

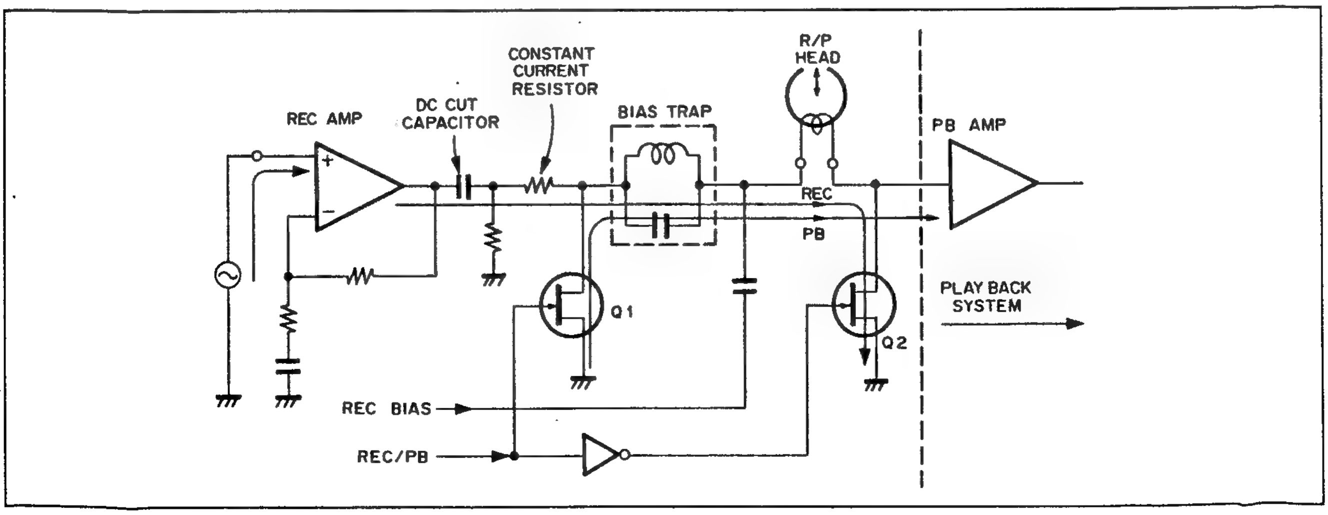


Fig. 4-2-5. Record/Playback Selector Fundamental Circuit (AP-15)

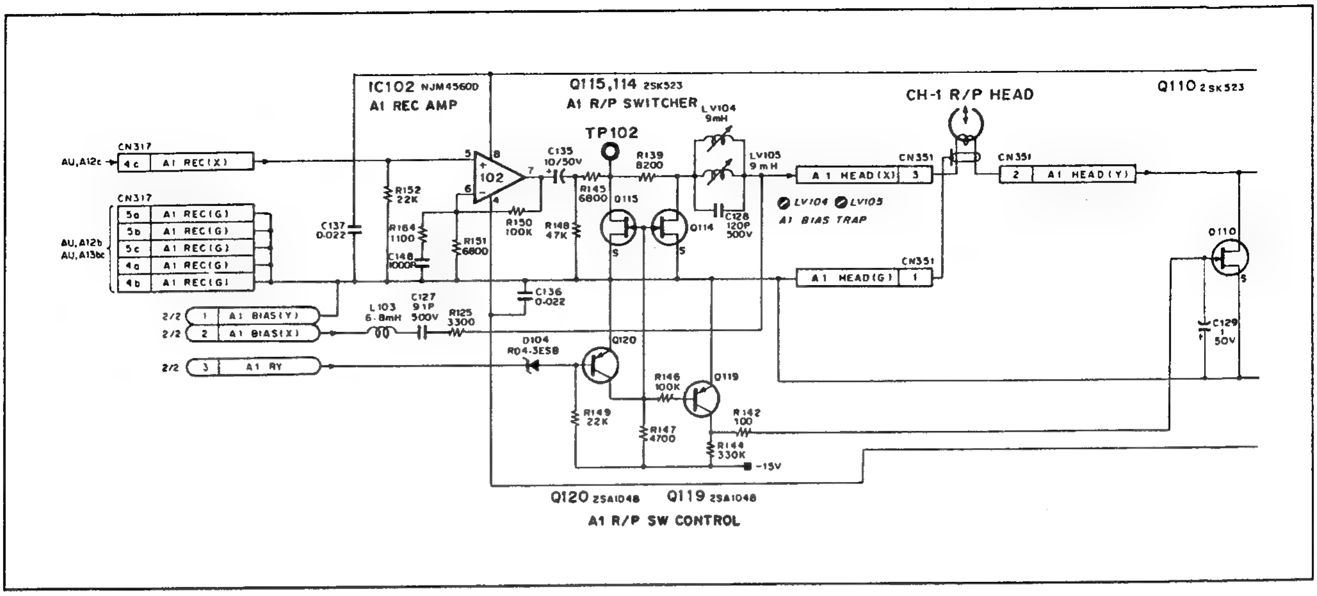


Fig. 4-2-6. Audio-1 Record/Playback Selector (AP-15)

The actual circuit is shown in Fig. 4-2-6. Because all the audio-1, 2, 3 and 4 channels have the same circuit configurations, only the audio-1 channel is described. C135 is the dc-cut capacitor that prevents the dc-current from flowing through the R/P head so that the R/P head should not get magnetized by the dc-current. Transistors Q114 and Q110 are the record/playback switching FETs. Q115 forms the record muting circuit with R145, that prevents the record circuit's noise from leaking into the playback circuit. Inductors LV104 and LV105 and capacitor C128 are the bias trap forming the parallel resonant circuits. Here, LV104 and LV105 are connected in opposite polarities each other so that external noise like hum is cancelled even though it leaks into LV104 and LV105, and the noise will not be recorded on tape.

(3) Record phase adjustment circuit (AU-88 board)

This circuit shifts the signal phase alone, while the original record signal amplitude is maintained. The audio-1 circuit does not have the phase adjusting circuit but the audio-2 has the phase adjusting circuit so that the correct phase relationship between the CH-1 signal and the CH-2 signal is maintained by adjusting the audio-2 signal phase. By using this adjustment, the phase difference between the audio-1 signal and the audio-2 signal can be minimized.

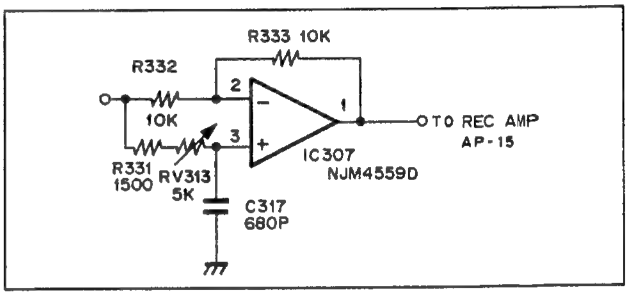


Fig. 4-2-7. Audio-2 Record Phase Adjustment Circuit (AU-88)

(4) Record system frequency response

The record system frequency response is shown in Fig. 4-2-8. Various losses incurred in the record system are compensated with this characteristics curve. Because the NTSC model and the PS model have the different time constant for playback equalizer's low frequency range, the record systems also have different low frequency response.

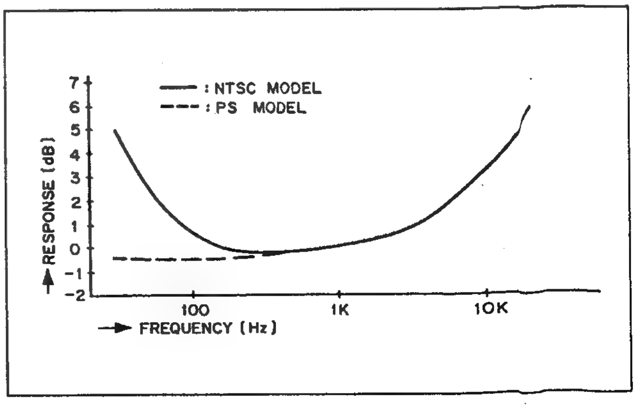


Fig. 4-2-8. Record Equalizer Frequency Response (AU-88)

4-2-3. Audio Signal Playback System (AU-88, AP-15 Boards)

The playback system amplifies the R／P head's playback signal and provides the various signal processing for the playback signal until the playback signal is fed to the LINE OUT connector for output. The playback system's signal flow is shown in Fig. 4-2-9.
The playback signal that is picked up by the R／P head is amplified by the AP-15 board's playback amplifiers and then sent to the AU-88 board.
The playback signal passes through the crosstalk canceller, the bias trap, the playback equalizer, the muting, and the attenuator circuits located in the AU-88 board and then sent to the VR-51 board for playback level adjustment.
After playback signal level is adjusted, the signal is sent from the VR-51 board back to the AU-88 board where it is passed through the TAPE／EE selector, and is then distributed to the monitor circuit and to the output amplifier circuit. The output signal is converted from the unbalanced type to the balanced type signal in the output amplifier circuit. The signal is power-amplified at the next stage, being routed through the power on／off muting relay, and is output the LINE OUTPUT connector on the MA-26 board.

The playback equalizer frequency response is shown in Fig. 4-2-10.

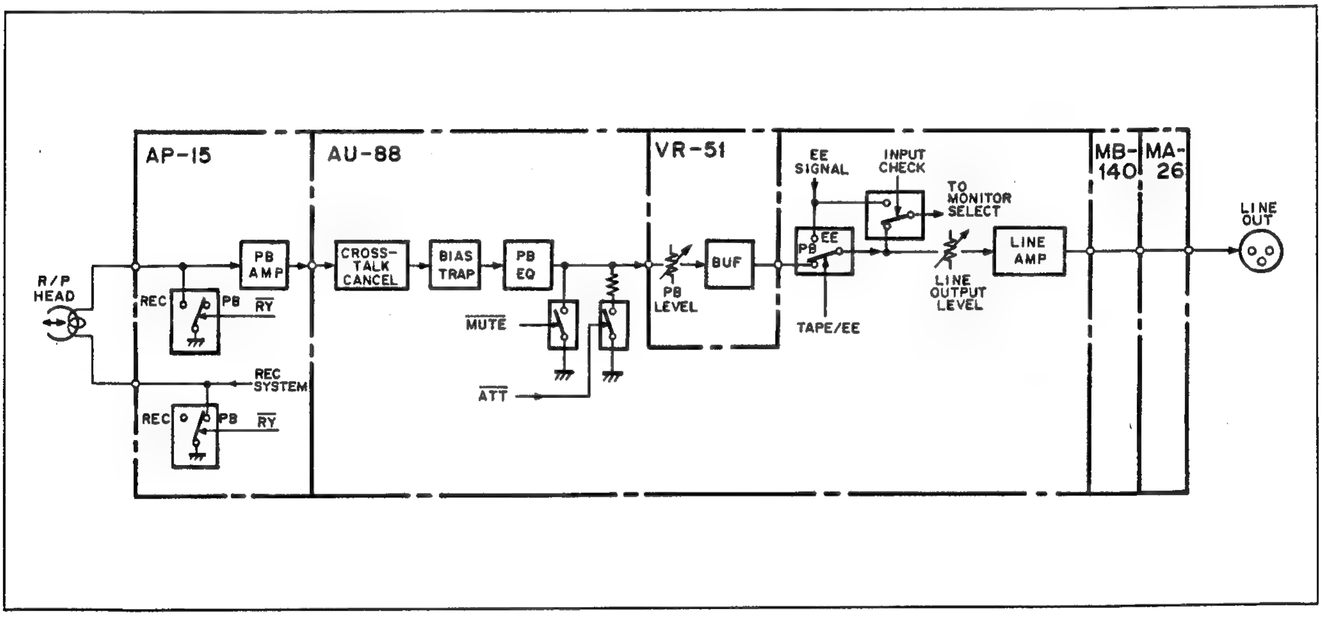


Fig. 4-2-9. Audio Signal Playback System

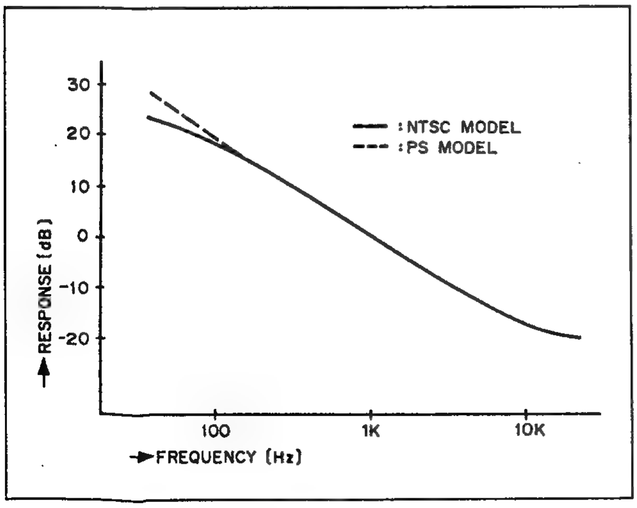


Fig. 4-2-10. Playback Equalizer Frequency Response

The audio line amplifier of BVH-3000/3100 employs the BTL (Balanced Transformer-Less) type amplifiers using no transformer, having the ±18V power supplies. The non-distorted output of this circuit is +28dBm with 1kHz/600 Ω load, having approx. 34dB (1kHz) amplification gain. This circuit can be muted perfectly using relay.
The line amplifier of the audio-1 is shown in Fig. 4-2-11. The audio-2, 3 and 4 channels have the same circuit configurations as audio-1 channel.
The IC118 line amplifier has the two built-in amplifiers where one amplifier is the inverting amplifier and the other is the non-inverting amplifier. The buffer connected after each amplifier functions as the the power amplifier. The line amplifier has the amplification·gain of approx. 33.6dB.
Diodes D109 through D112 function to protect the output transistors. Transistors Q718 through Q720 constitute the muting control circuit of the Schmitt type that controls muting at power on/off timings. The muting time is approx. 6 seconds when the power is turned on, that is determined by the time constant of R824 and C781.

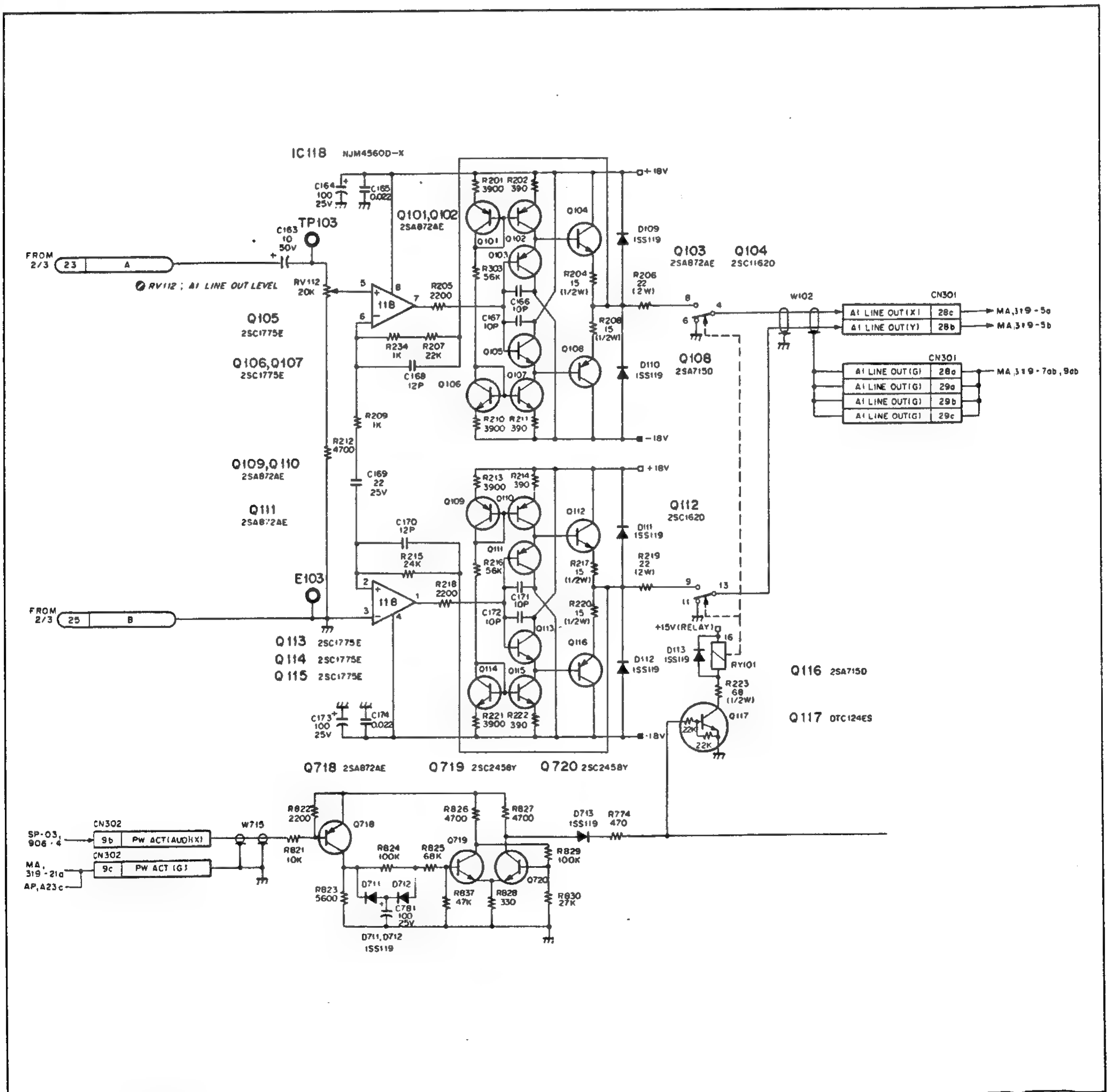


Fig. 4-2-11. Audio-1 Line Amplifier (AU-88)

4-2-4. Crosstalk Canceller (AU-88 Board)

(1) Outline

The crosstalk canceller circuit has the following three kinds in this machine.

a. PB-PB crosstalk canceller
When both of the two channels are put into playback mode simultaneously, a crosstalk will occur. This PB-PB crosstalk between the two channels can be cancelled by this crosstalk canceller. This crosstalk can be cancelled by connecting the playback signals from the two channels in opposite phase each other.

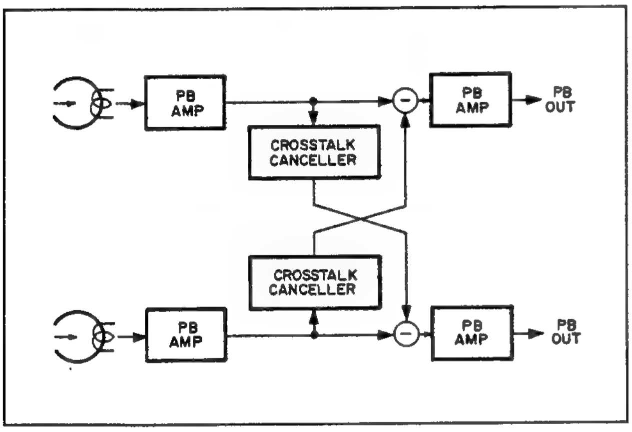


Fig. 4-2-12. PB-PB Crosstalk Canceller

b. REC-REC crosstalk canceller
When both of the two channels are put into record mode simultaneously, a crosstalk will occur between the two channels. This REC-REC crosstalk can be cancelled by this REC-REC crosstalk canceller. This crosstalk can be cancelled by connecting the recording signals of both channels in opposite phase each other.

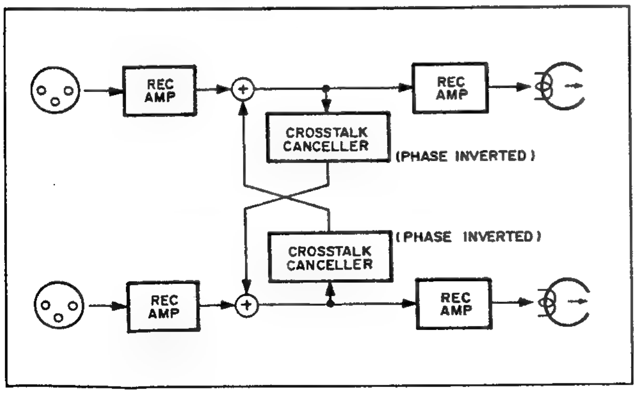


Fig. 4-2-13. REC-REC Crosstalk Canceller

c. REC-PB crosstalk canceller
When one channel is in record mode while the other channel is in playback mode, the recording channel signal can leak into the playback channel, causing crosstalk. This REC-PB crosstalk can be cancelled by REC-PB crosstalk canceller. This crosstalk can be decreased by adding the recording channel component into the playback channel in opposite phase.

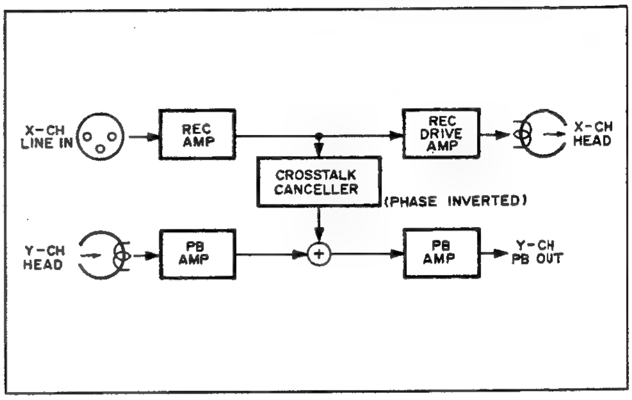


Fig. 4-2-14. REC-PB Crosstalk Canceller

These crosstalk canceller are classified into the following categories in respective channels.

a. Between the channels of audio-1 and audio-2
Between the channels of audio-3 and audio-4 (only in PS-A4 model)
- PB ↔ PB crosstalk canceller
- REC ↔ REC crosstalk canceller
- REC → PB crosstalk canceller

b. Between the channels of audio-3 and CTL (NTSC model)
- PB CTL → PB A3 crosstalk canceller
- REC A3 → PB CTL crosstalk canceller

c. Between the channels of audio-3 and CTL (PS-A3 model)
- PB CTL → PB A3 crosstalk canceller
- REC A3 → PB CTL crosstalk canceller
- REC CTL → PB A3 crosstalk canceller (in the video assemble mode)

d. Between the channels of audio-4 and CTL (PS-A4 model)
- PB CTL → PB A4 crosstalk canceller
- REC A4 → PB CTL crosstalk canceller
- REC CTL → PB A4 crosstalk canceller

(2) PB-PB crosstalk canceller (AU-88 board)

The PB-PB crosstalk canceller between the audio-1 and audio-2 channels, is shown in Fig. 4-2-15.
The cancel signal from the audio-1 to the audio-2, is generated by the circuit of R145 through R148, C126, C127 and RV105, is input to pin 6 (−terminal) of IC309 to be added to the audio-2 channel in opposite phase.
The cancel signal from the audio-2 to the audio-1 is generated by R345 through R348, C326, C327 and RV305.

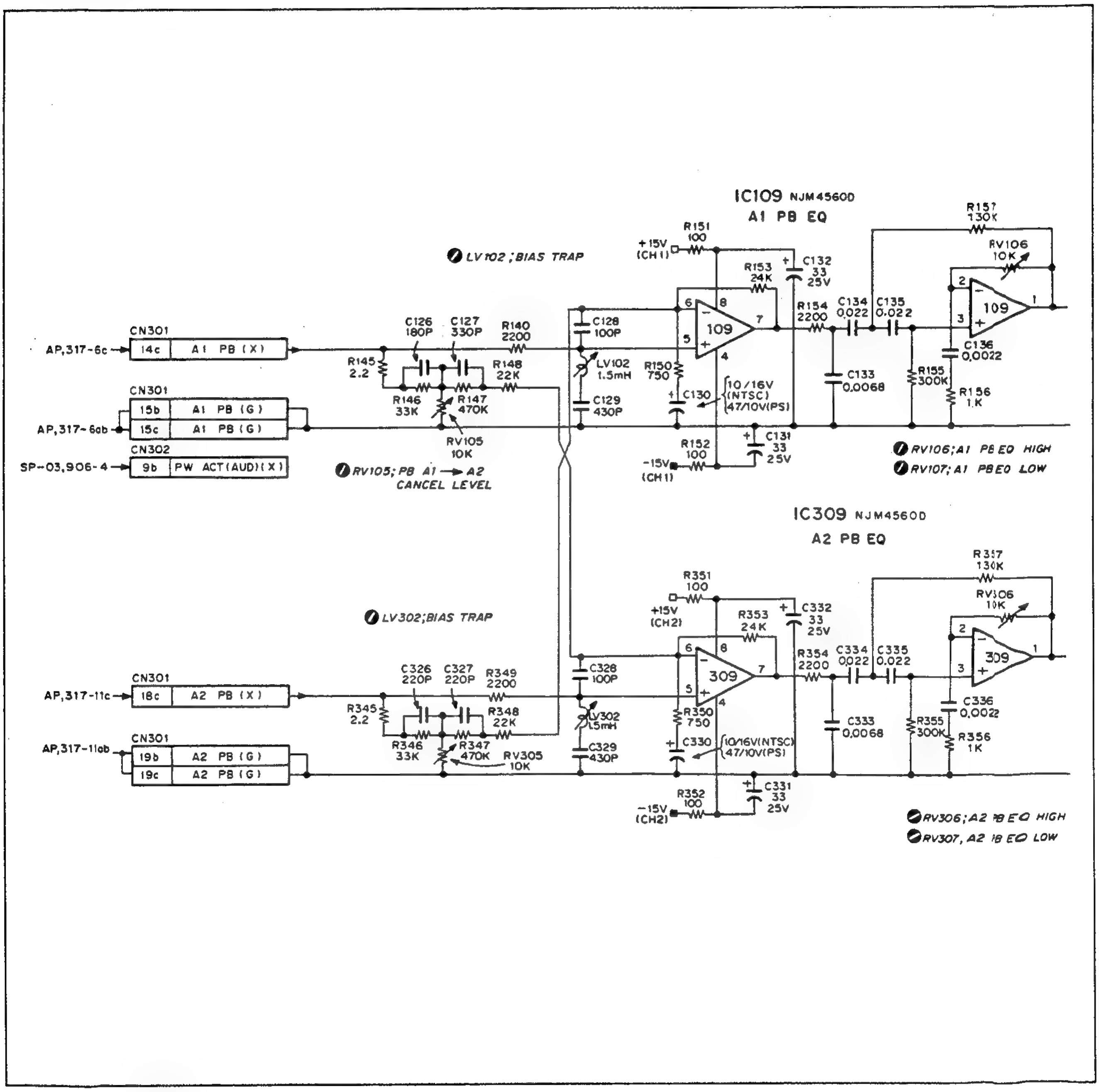


Fig. 4-2-15. PB-PB Crosstalk Canceller (AU-88 board)

(3) REC-REC crosstalk canceller (AU-88 board)

The audio-1 recording equalizer amplifier output is inverted/amplified by IC107 (pin 7), and is added to the audio-2 recording equalizer amplifier output. Thus the crosstalk from the audio-1 to the audio-2 in the record mode is cancelled.

(4) REC-PB crosstalk canceller (AU-88 board)

The pin 7 of IC107 output that is the REC-REC crosstalk canceller circuit's output is added to the audio-2 playback equalizer amplifier circuit through analog switch IC108. This is how the crosstalk is cancelled when the audio-1 is in the insert record mode while the audio-2 is in the playback mode. The IC108 analog switch is kept on in all modes other than record mode of audio-1 channel that prohibits the cancel signal from being sent to the audio-2 channel.
The crosstalk level in the high frequency area during insert mode can be adjusted by adjustment controls RV104 and LV101.

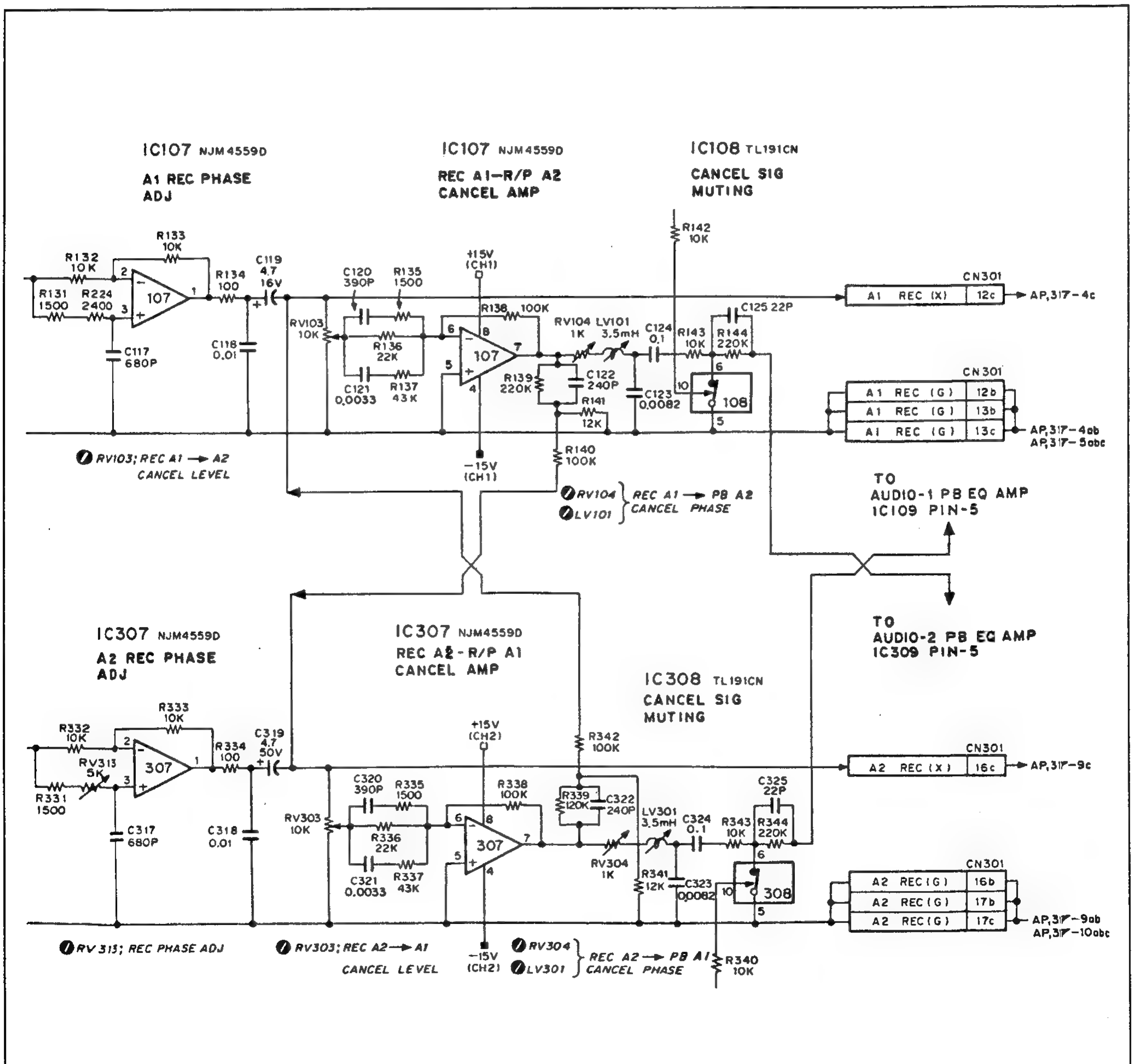


Fig. 4-2-16. REC-REC and REC-PB Crosstalk Canceller (AU-88)

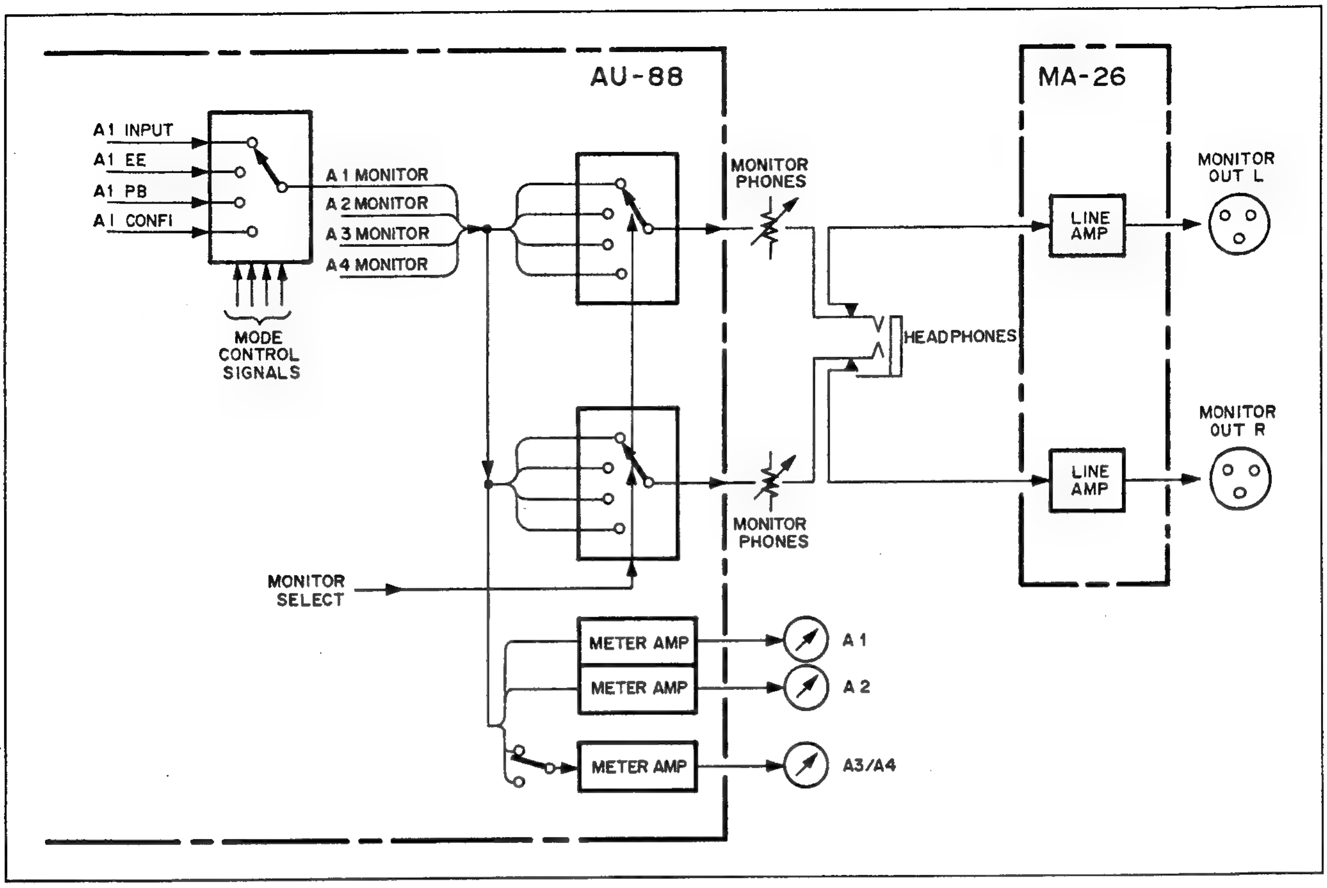


Fig. 4-2-17. Audio Monitor Selector System

4-2-5. Monitor System (AU-88, MA-26 Boards)

The monitor system circuit provides the output signal to the headphone jack on the level control panel, and to the MONITOR OUTPUT L/R connectors located on the connector panel.
The MONITOR SELECT switch on the level control panel can specify which of the A1, A2, A3 and A4 channels is to be selected as the monitor output. Which output of INPUT, EE, PB and CONFI PB signals, should be selected as the monitor signal, is automatically determined depending upon the operating mode of the VTR.
The audio meter is driven by the output signal from the monitor system circuit.

(1) Audio-1/Audio-2 mixing circuit (AU-88 board)

This circuit is to generate the mixtures signal of the audio-1 signal and the audio-2 signal without changing their signal phases. This function can be effectively used in order to confirm the phase difference between the two channel signals during the stereophonic operation very easily.
The audio-1 monitor signal and the audio-2 monitor signal are added and amplified by IC315/IC316 and are fed to the monitor select circuit.
When both signals of the audio-1 and the audio-2 are in phase, the IC316 output signal will obtain the doubled amplitude against the audio-1 or the audio-2 signal.

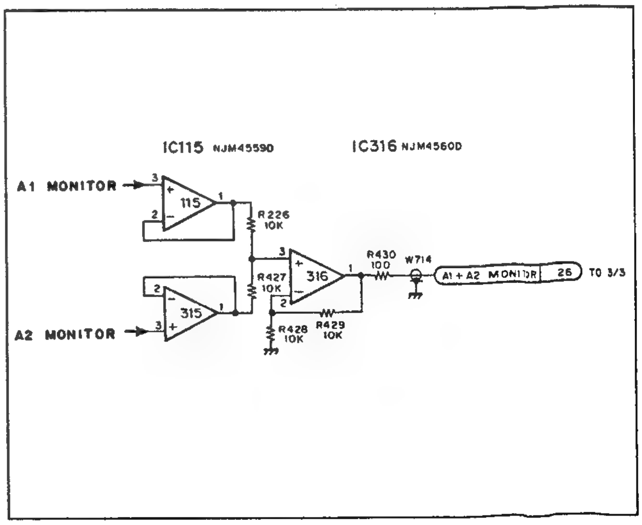


Fig. 4-2-18. Audio-1/2 Mixing Circuit (AU88)

(2) Audio monitor (CONFI) playback circuit (AU-88 board)

In order to confirm whether the audio signal is surely recorded on tape or not in the record mode or in the edit mode, the monitor heads for the audio-1 and for the audio-2 (in the audio-4 too in the PS A4 model), are equipped.
The playback signal that is picked up by the monitor head is amplified by the playback amplifiers on the AP-15 board and then sent to the AU-88 board.
The CONFI playback signal that is sent to the AU-88 board, is supplied to the equalizer and then to the monitor select switch.

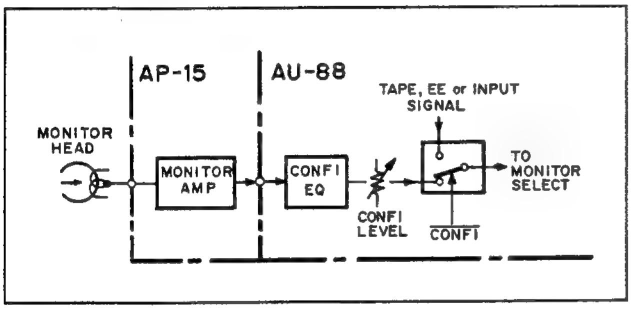


Fig. 4-2-19. Audio Monitor (CONFI) Playback System

4-2-6. Audio Record Bias System (AP-15 Board)

(1) Bias/erase oscillator (AP-15 board)

This circuit is the Colpitts oscillator consisting of the IC1 inverter and the X1 ceramic oscillator. Oscillating frequency of this circuit is 800kHz. The frequency is divided by four to make 200kHz that is sent to the IC4 resonant amplifier. The bias signal input at IC4 is wave-shaped into sine wave and sent to pins 3 and 6 of IC5. The two kinds of signal having 180° out of phase each other, are sent out from pins 1 and 7 of IC5 to the bias drive circuits.

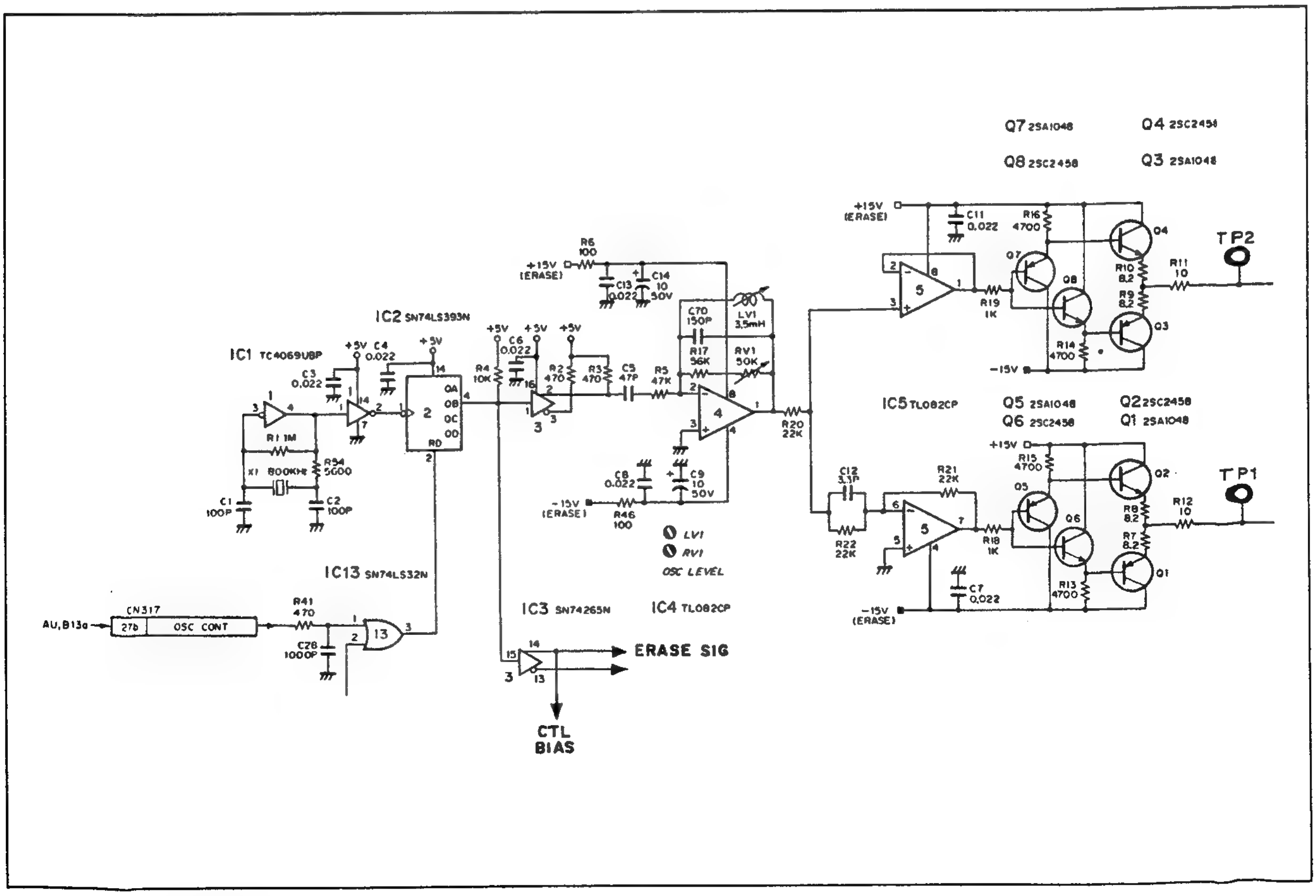


Fig. 4-2-20. Bias/Erase Oscillator (AP-15)

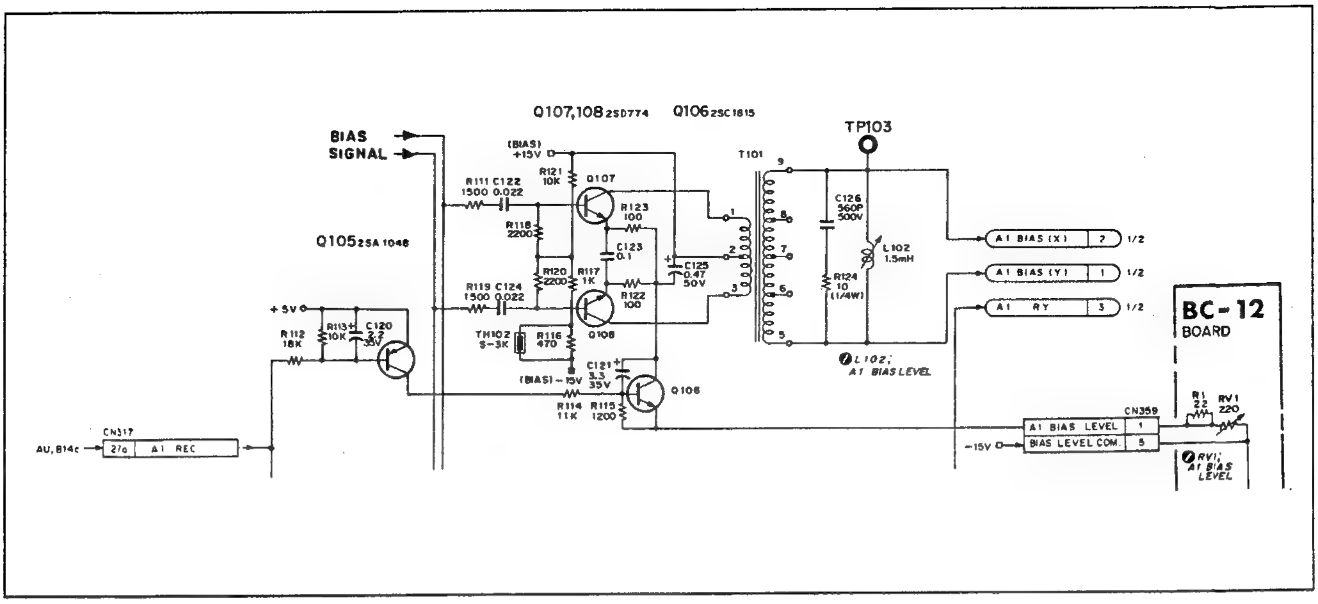


Fig. 4-2-21. Bias Driver (AP-15)

(2) Bias driver (AP-15 board)

The bias drive circuits for the audio-1, 2, 3 and 4 have the same circuit configurations so that only audio-1 channel circuit is described as follows. The audio-4 is installed only in the PS A4 model.
The audio record bias system consists of the bias timing control circuit and the bias drive circuit. The bias drive circuit is constituted by the push-pull type drive circuit using the Q107/Q108 transistors and the T101 transformer.
Q105/Q106 are the bias timing control circuit using an integrator that controls the bias signal on/off timing so that the audio signal should not be made non-continuous at the editing point. The bias level can be adjusted by the RV1 variable resistor located on the BC-12 board that controls the operating current of bias drive circuit.

4-2-7. Erase System (AP-15 Board)

The erase circuits for the audio-1, 2, 3 and 4 channels have the same circuit configuration so that only the audio-1 and 2 channels are described as follows. The audio-4 is installed in the PS A4 model only.
The erase driver circuit in the audio-1 and 2 channels have the same circuit configurations but the signals in both channels have the different phase in 180° apart in order not to leak the erase signals into the opposite channels.
This leak of erase signal into opposite channels is caused by the transformer-coupling between the coil windings inside the erase head, and is cancelled by inserting the inductors and resistors.

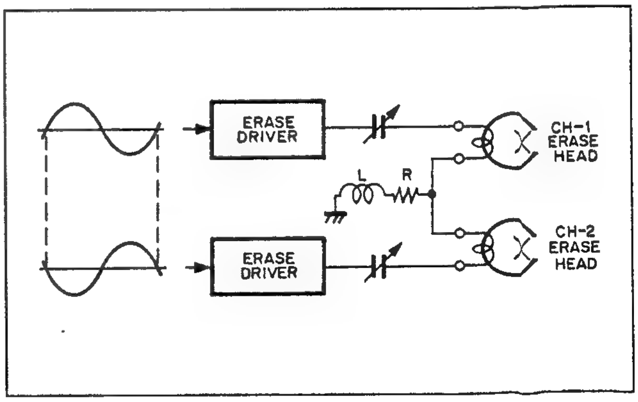


Fig. 4-2-22. Erase System (AP-15)

The 200kHz erase signals having 180° phase difference, is supplied from the bias/erase oscillator to pins 13 and 11 of IC12. IC101 and IC201 are forming the integrator that controls the erase signal's rise-up timing and fall-down timing. The resonant circuits of LV101/C112 and LV201/C212 decrease the waveform distortion.

The IC11 analog switch is the circuit that the erasure should not take place at the power on/off timings. The leakage of the erase signal between two channels are be cancelled by L206 and RV202.

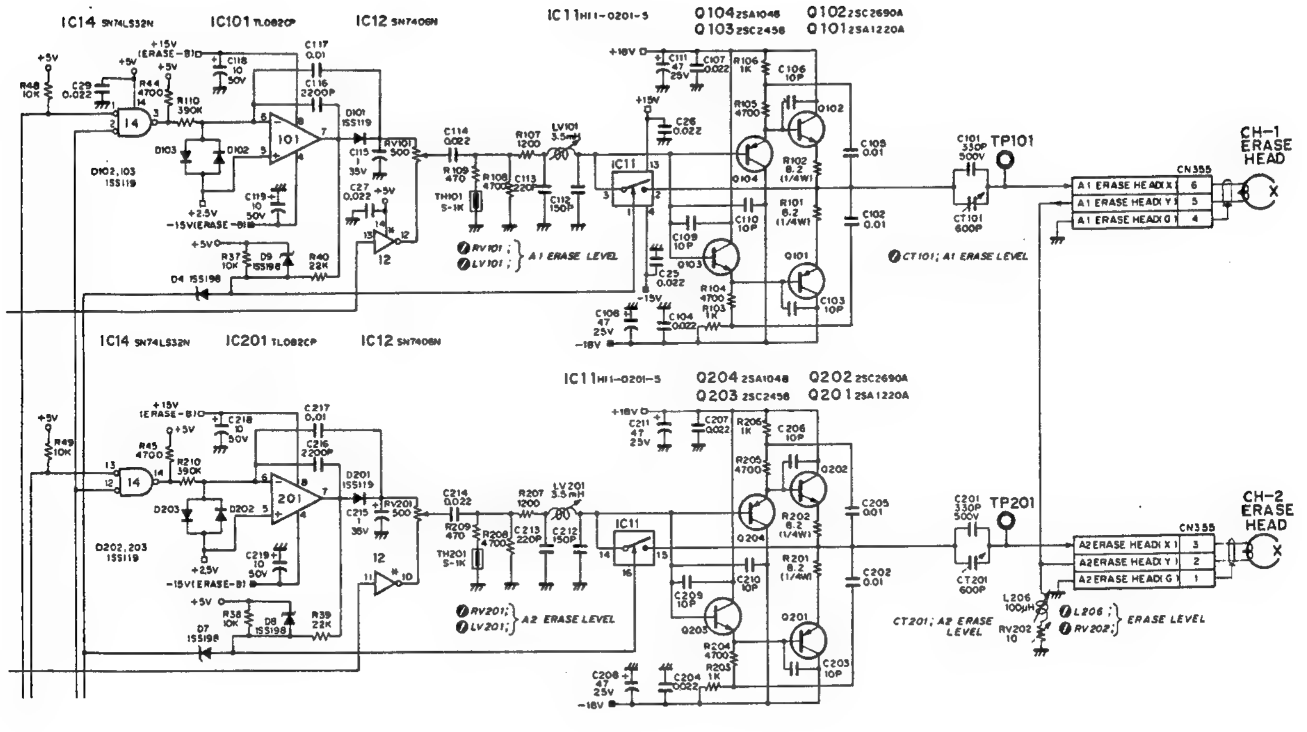


Fig. 4-2-23. Channel Erase Circuit (AP-15)

4-2-8. Audio Control Signal System (AU-88 Board)

The control signals for the audio signal system, are sent from the SV-90 board in the form of 8-bit serial data.
The serial data are converted into parallel data and then used for each control. The serial-to-parallel conversion is done by I/O expander IC4 and IC5 (CXD1095Q) on the AU-88 board.

The control signal for the bias erase system is supplied from IC4 to the AP-15 board in the form of parallel signal. The control signal for the LED display of the monitor select system is sent out from IC5.
The REC inhibit command or the monitor select command that are set-up depending upon the switch settings on the level control panel, are converted from parallel to serial by the same I/O expander, and are sent to the main CPU on the SV-90 board.

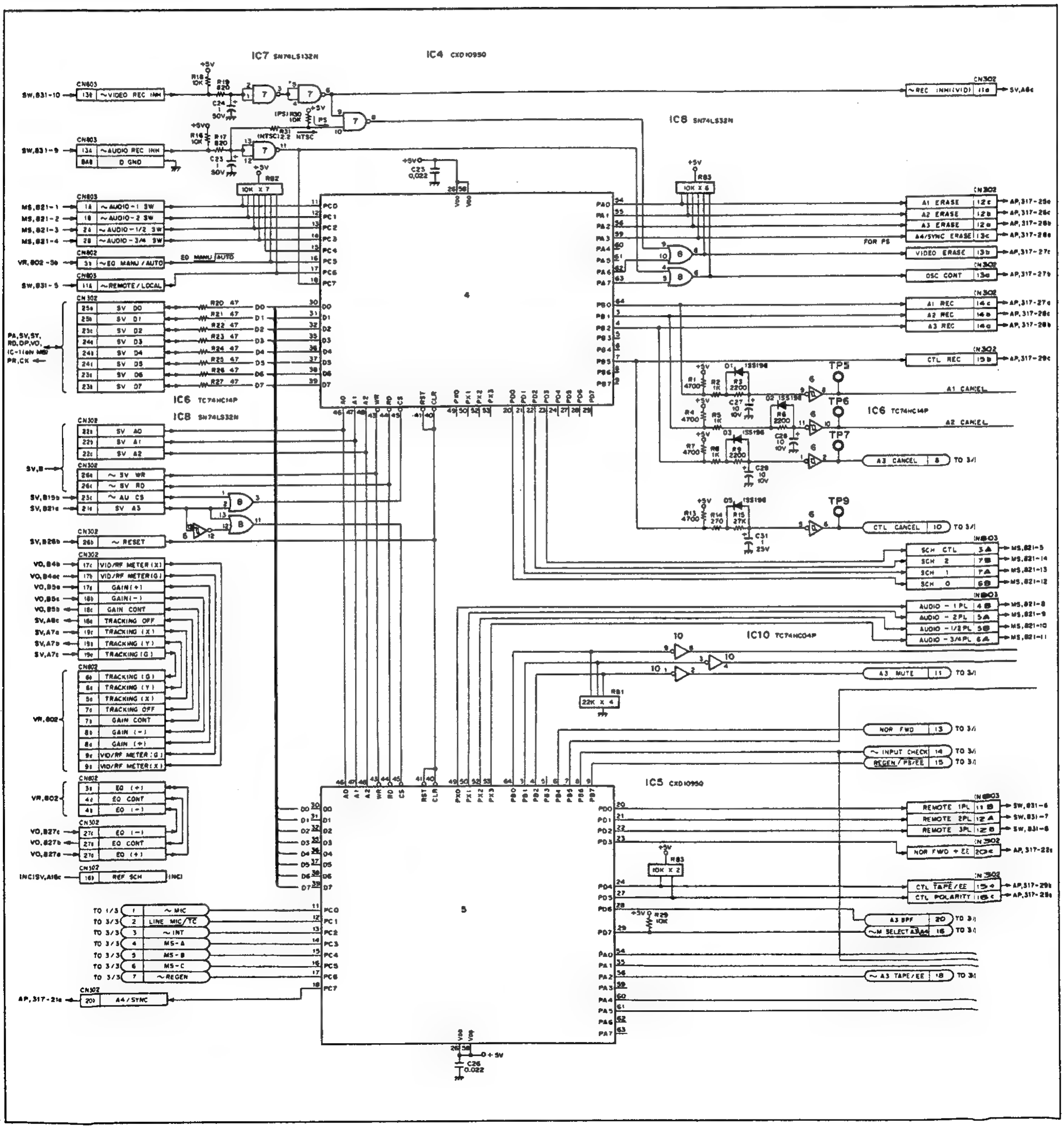


Fig. 4-2-24. Audio Control Signal System (AU-88)

4-2-9. Time Code System (AU-88 Board)

The time code signal is recorded on the audio-3 track. The necessary circuit for time code signal processing is located in the audio-3 circuit block.

(1) Time code record system (AU-88 board)

The two kinds of time code signals can be recorded. One signal is the TC GEN signal that is generated by the SY-103 board's time code generator while the other is the time code signal being supplied from the A3 LINE IN connector. Either one of these two time code input signals, is selected by the IC520. The time code signal selected by IC520, is wave-shaped by the comparator IC521 and then sent to IC519 through IC522 and IC525 where the signal is again wave-shaped. The wave-shaped time code signal is sent to the record equalizer through the IC506 analog switch. The rest of the signal processing is the same as the normal audio-3 signal processing.

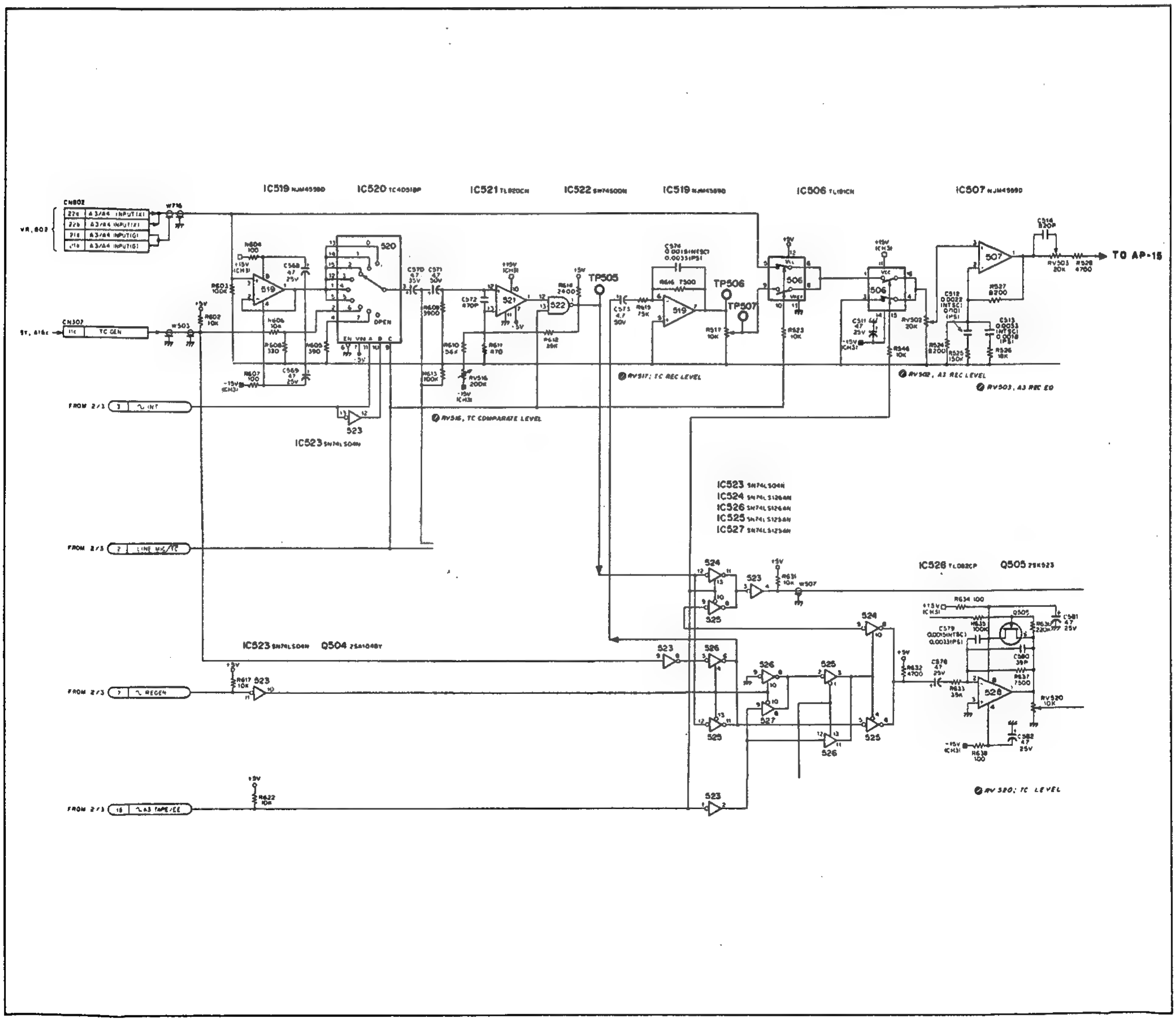


Fig. 4-2-25. Time Code Record System (AU-88)

(2) Time code playback system (AU-88 board)

The playback time code signal is input to the AU-88 board as an ordinary audio signal, amplified by IC510 and IC513, and is then sent to the playback level control circuit as the audio signal, and also sent to the wave-shape circuit of IC521 and IC522 as the time code signal. The wave-shaped time code signal is sent to the time code reader circuit of the SY-103 board through IC525 and IC523. The time code signal is shaped into the specified wave-shape by IC524 and IC528, and is then sent to the audio-3 line amplifier.

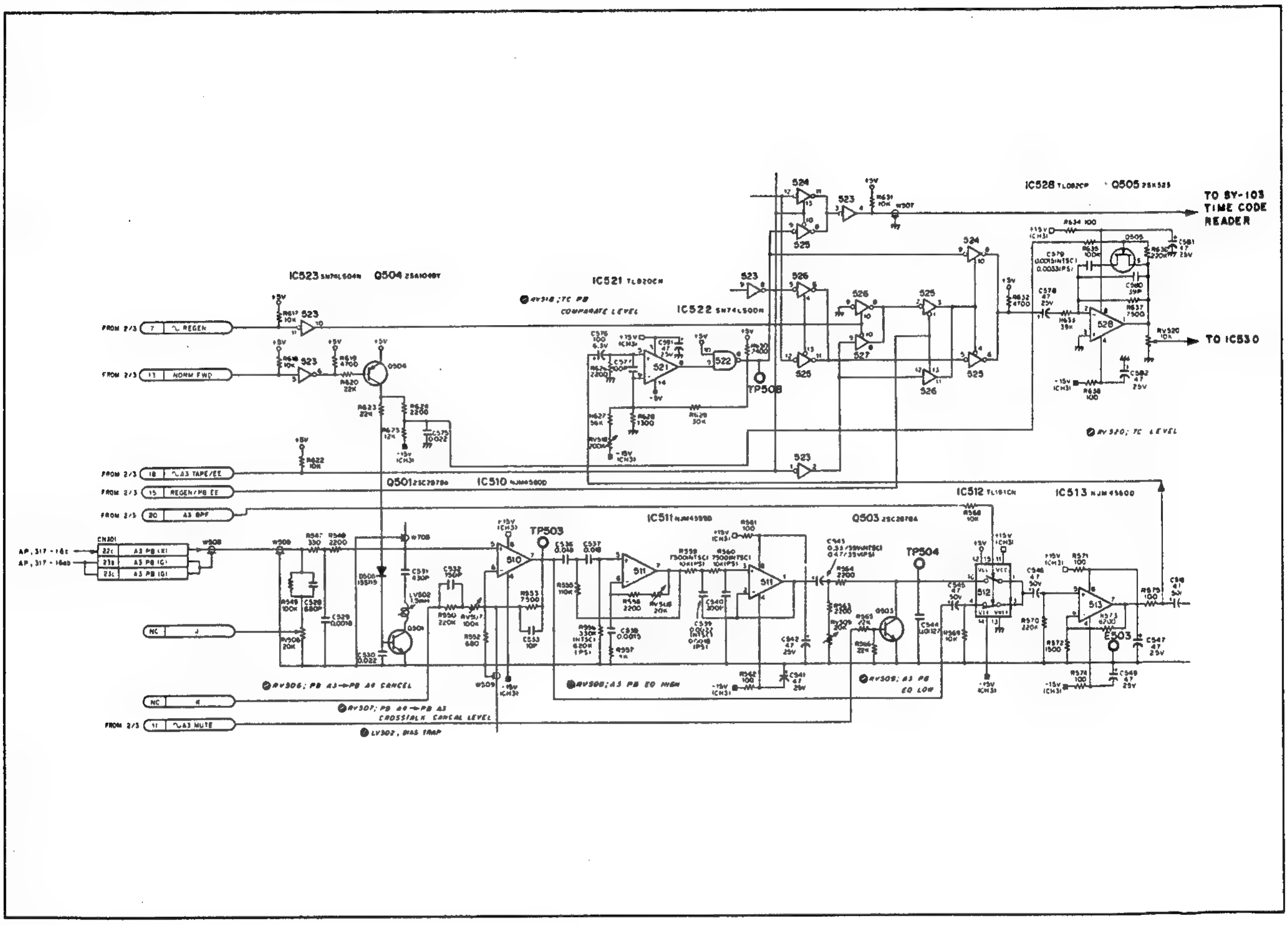


Fig. 4-2-26. Time Code Playback System (AU-88)

4-3. VIDEO SIGNAL SYSTEM

Note 1 : Any references to the sync channel in the description below apply only to the model BVH-3000 and not to the model BVH-3100.

Note 2 : Reference should be made to Section 4-4 for details on the TBC section.

4-3-1. Outline of Video Signal System

The video signal system circuitry is composed of five circuit boards whose names and functions are listed below

1. VO-16 board : Modulator, RF equalizer, demodulator
2. RP-32 board : REC/PB amplifier (for R/P head)
3. VS-30 board : I/O buffer/monitor output amplifiers
4. VR-51 board : REC level/PB equalizer control
5. DR-13 board : PB amplifier/strain gauge amplifier (for PLAY head)

The video signal input to the VIDEO INPUT terminal is supplied to the VO-16 board via the buffer amplifier on the VS-30 board. On the VO-16 board, the level of the video signal is first adjusted by the DC voltage from the REC level control on the front panel and then it is frequency-modulated. The frequency-modulated RF signal is amplified by the RP-32 board, supplied to the R/P head and then recorded onto the tape.

During playback, the signal recorded on the tape is played back by the R/P head or PLAY head. The RF signal from the R/P head is supplied to the VO-16 board via the RP-32 board, and the RF signal from the PLAY head is supplied to the VO-16 board via the DR-13 board inside the upper drum. The VO-16 board is responsible for the differential gain, differential phase and frequency response compensation and other such equalizer processing and also for the demodulation of the RF signal.
The demodulated video signal passes through the noise suppressor which serves to suppress the switching noise which is generated with video/sync channel switching, it then goes through the TBC section and is output from the VIDEO OUTPUT terminal via the buffer on the VS-30 board.

4-3-2. Video Signal Recording System (VO-16, RP-32 Boards)

The video signal which is input to the VIDEO INPUT terminal is supplied to the VO-16 board through the buffer on the VS-30 board, and its level is adjusted by the DC voltage from the VIDEO level control on the front panel. The adjusted signal is supplied via the pedestal clamp, burst doubler, VITC insertion and pre-emphasis circuits to the modulator where it is frequency-modulated.
The modulator output is supplied to the demodulator as the EE signal, and it is also supplied to the R/P head through the recording amplifier on the RP-32 board and recorded onto the tape.

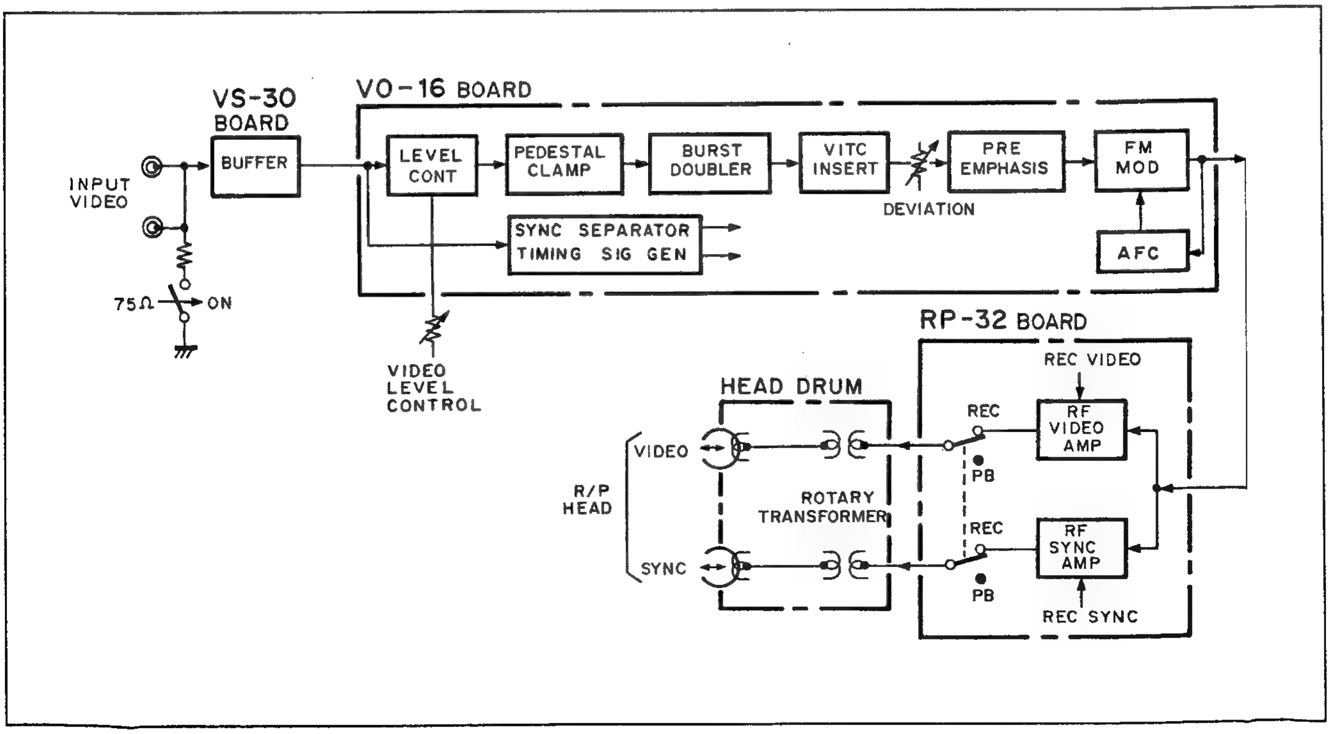


Fig. 4-3-1. Video Signal Recording System

(1) Input level controller (VO-16 board)

The input video signal which has been sent from the VS-30 board to the VO-16 board passes through buffer amplifier IC1 and its level is controlled by IC2. The control signal controls the inverted input (−input) impedance of video amplifier IC2 by the DC voltage (TP4) which has been sent from the VR-51 board.
The control range is from −6dB to 3.5dB. In other words, the signal can be controlled to the same level as that of the normal input video signal in the event of no termination or double termination. The video signal whose level has been controlled is sent to the pedestal clamper circuit.

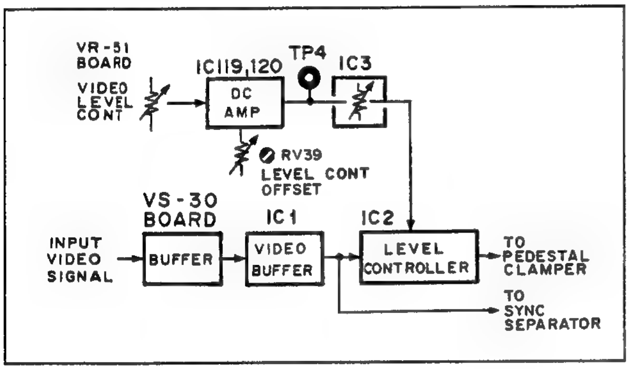


Fig. 4-3-2. Input Level Controller (VO-16)

(2) Sync separator/timing signal generator (VO-16 board)

One of the input buffer outputs passes through the low-pass filter composed of R98 and C146, it is amplified 2-fold by IC42 and it enters sync separator IC43.
The sync separation output is produced from pin 4 of IC43 and the TTL level is provided by R104 and R105. The signal is then supplied to the IC44 and 45 monostable multivibrators to produce the timing signals with the required phase and pulse width.
The TP2 output pulse is sent to the pedestal clamper, burst doubler and AFC circuit while the TP3 output pulse is sent to the AFC circuit.

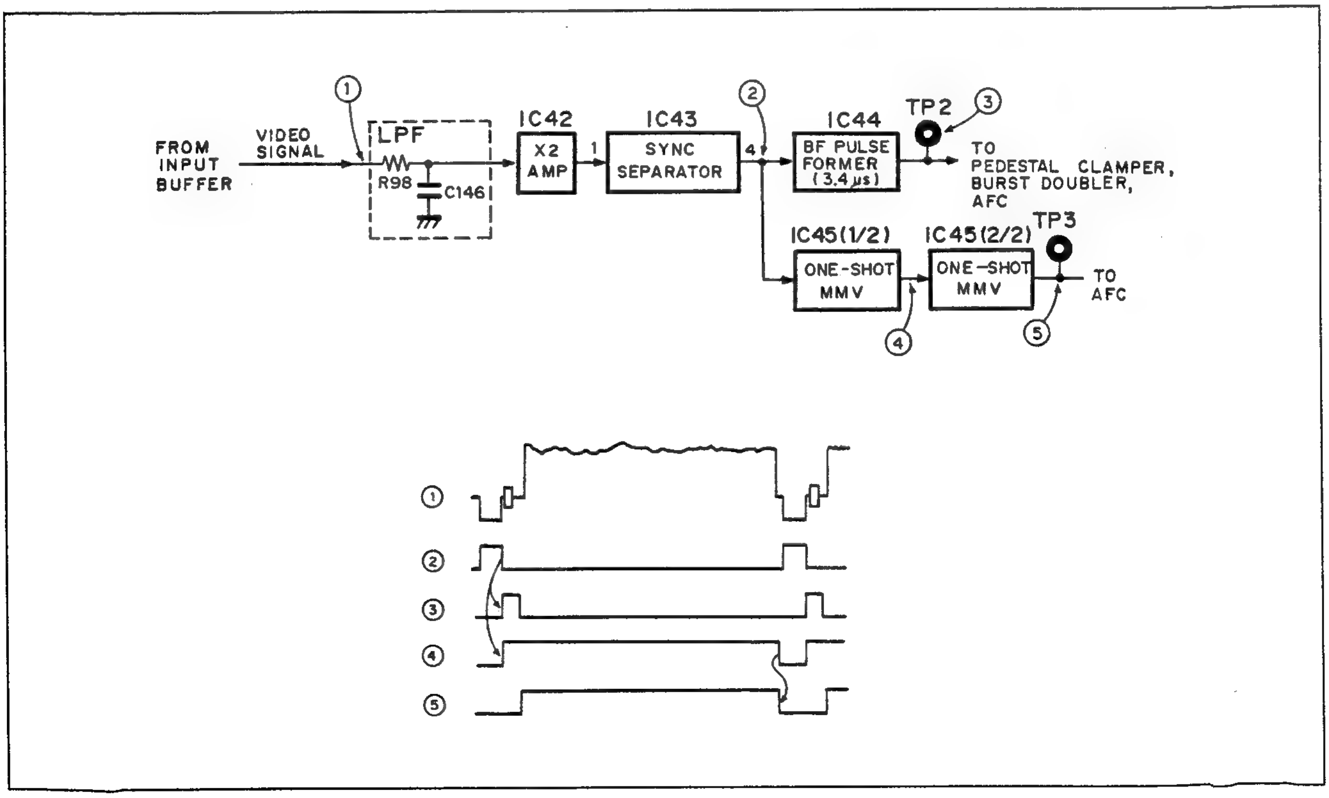


Fig. 4-3-3. Sync Separator/Timing Signal Generator (VO-16)

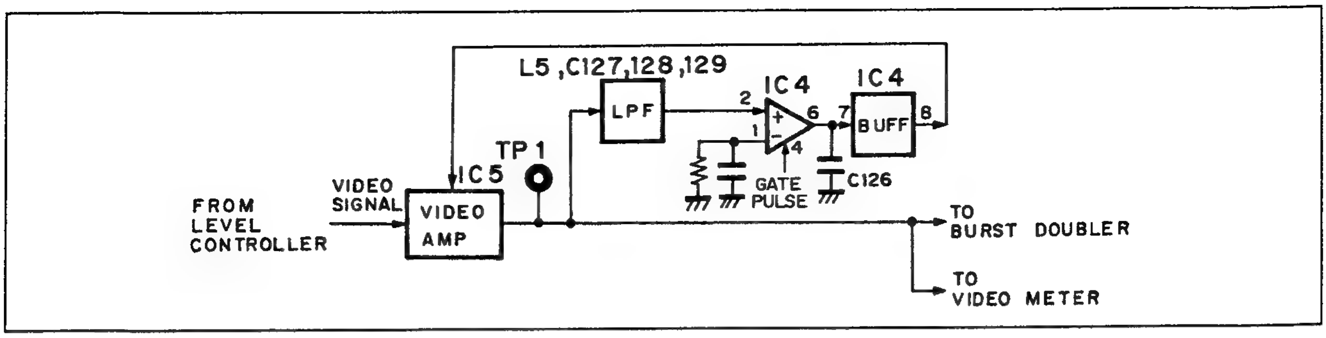


Fig. 4-3-4. Pedestal Clamper (VO-16)

(3) Pedestal clamper (VO-16 board)

The input video signal whose level has been controlled by IC2 is supplied to the pedestal clamper which is configured by IC4 and IC5. This circuit fixes the back porch portion of the video signal at DC 0V in order to stabilize the operation of the later stage circuitry when video signals with a fluctuating APL are supplied.
The video amplifier IC5 output (TP1) passes through the low-pass filter composed of C127, 128, 129 and L5, and it is supplied to pin 2 of IC4.
IC4, which is configured as shown in the figure, is a sample and hold circuit which charges the difference in level between pins 1 and 2 into C126 when the gate pulse is supplied to pin 4 and which outputs the signal as a DC voltage from pin 8 through the buffer amplifier. The video signal (TP1) whose pedestal level has been clamped is now supplied to the burst doubler and video level meter circuit.

(4) Burst doubler (VO-16 board)

The recording level of the burst signal is amplified 2-fold by the burst doubler in order to improve the signal-to-noise ratio of the burst signal during playback. The pedestal-clamped input video signal is amplified 2-fold by video amplifier IC6 and it is split into two. One signal is supplied to pin 6 of analog switch IC8 after its level is divided down to one-half by resistors; the other signal is supplied directly to pin 8 of analog switcher IC8. A video signal whose burst level is amplified 2-fold can be produced by switching the switcher using the TP2 burst gate pulse.

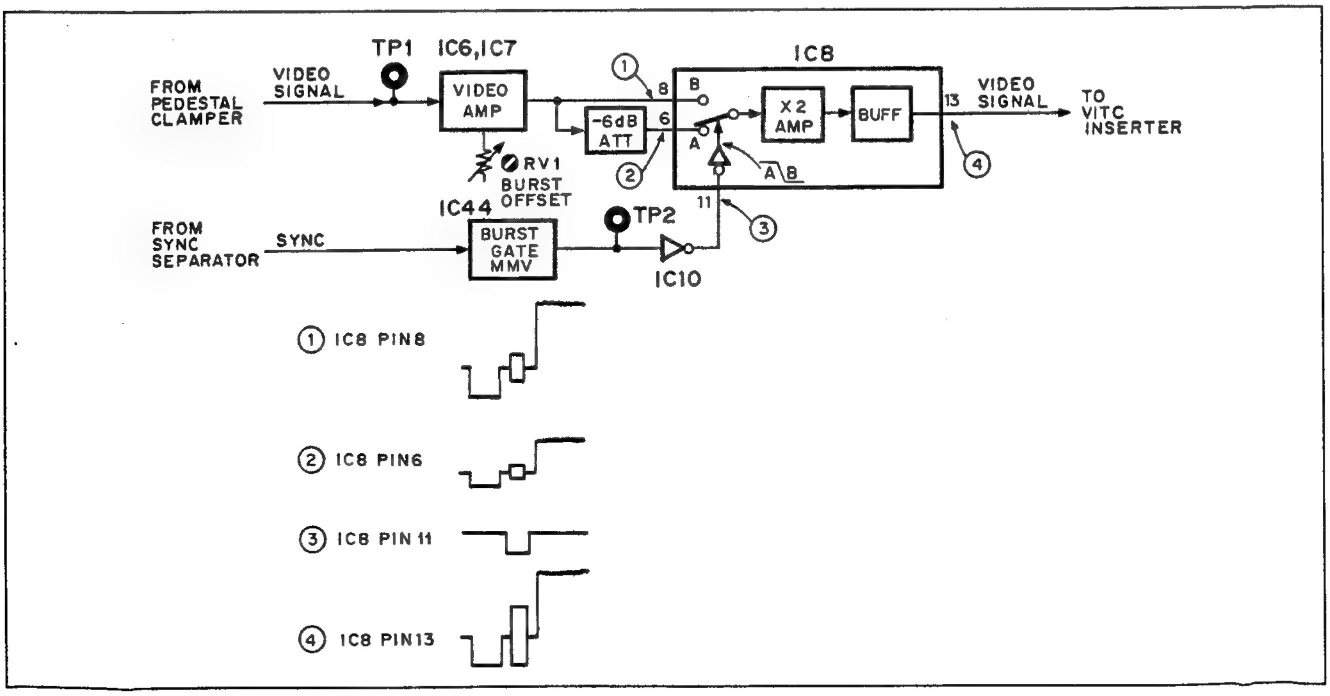


Fig. 4-3-5. Burst Doubler (VO-16)

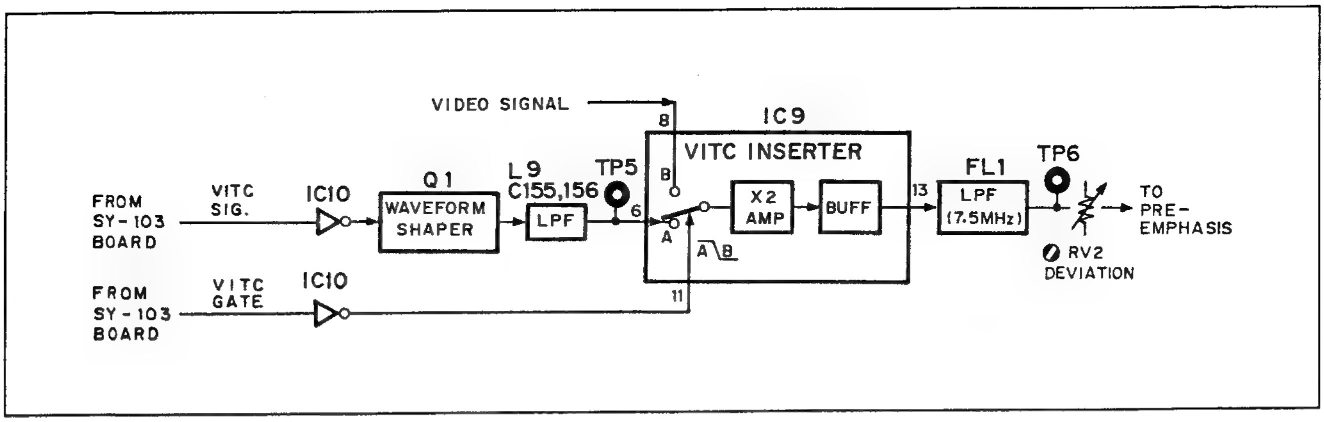


Fig. 4-3-6. VITC Inserter (VO-16)

(5) VITC inserter (VO-16 board)

This circuit serves to insert the VITC signal, which is supplied from the SY-103 circuit, into the input video signal.
The VITC signal (TP5), which has been waveform-shaped by Q1, is inserted into the video signal line by the VITC gate signal. The VITC gate signal is also sent from the SY-103 circuit. The VITC inserter circuit also functions as a circuit for inserting the time code characters into the video signal to be recorded and it does this for off-line editing purposes. Initial setup menu [I60. CHARACTER RECORD] is usedto select the character recording mode. The next-stage low-pass filter has characteristics of 7.5MHz/−3dB and it has been inserted in order to improve the signal-to-noise ratio and reduce the amount of switching noise during operations involving the burst doubler and VITC inserter. The low-pass filter output is sent to the pre-emphasis circuit through the variable resistor (RV2) used to adjust the deviation.

(6) Pre-emphasis and FM modulator (VO-16 board)

R37-40, C131 and C132 represent the emphasis constants. Based on these constants, the emphasis is 8dB (or 10.6dB for the PAL/SECAM system) and the center frequency is 420kHz (or 480kHz for the PAL/SECAM system). The output (TP7) of the pre-emphasis circuit provides the multivibrator with current drive and generates frequency modulated waves.
When there is any deterioration in the symmetry of the output waveforms of the multivibrator, this is accompanied by an even-numbered order of higher harmonics, and beat interference known as moire is generated. The balance of the modulator is adjusted by RV3 in order to improve the symmetry of the output waveforms. A balanced output type of oscillator is used in order to improve the symmetry of the output waveforms and to cancel out leakage into the RF signals from the video signal.

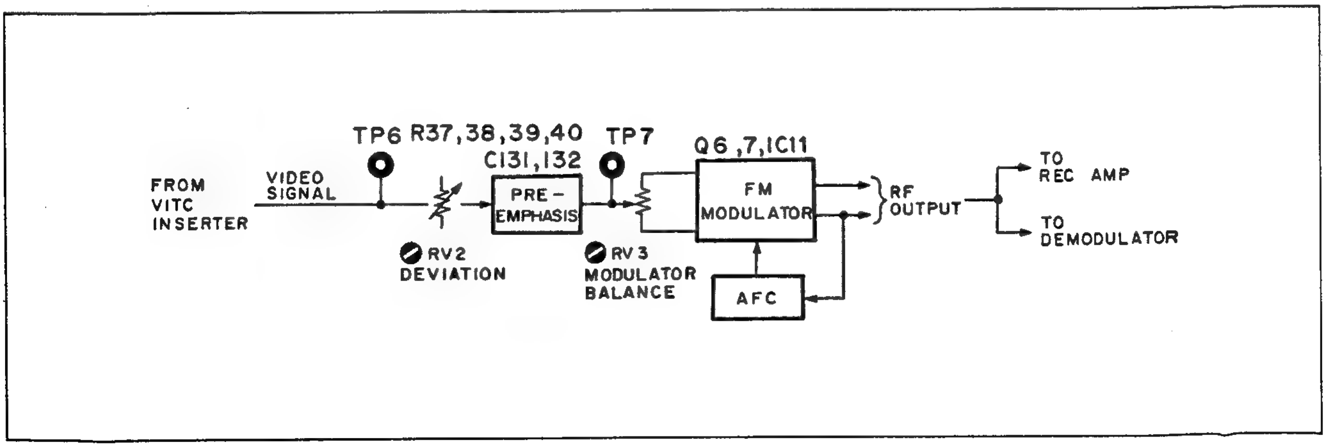


Fig. 4-3-7. FM Modulator (VO-16)

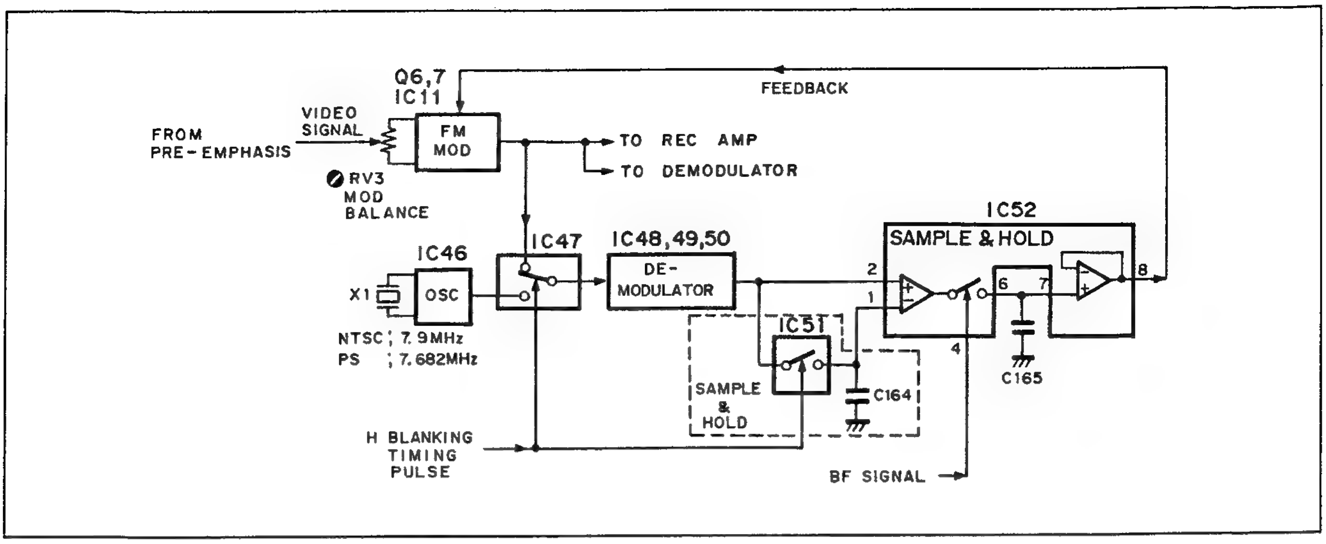


Fig. 4-3-8. AFC/FM Modulator (VO-16)

In order to stabilize the oscillation frequency of the FM modulator, the frequency of the pedestal portion of the modulator output is compared with the 7.9MHz (or 7.682MHz for the PAL/SECAM system) output frequency of the crystal oscillator and the resulting output is fed back to the modulator. The modulator output of the horizontal blanking period and the output of the crystal oscillator are multiplexed in IC47 by the TP3 timing signal. This is then demodulated into the video signal by IC48, 49 and 50 and by the low-pass filter.
The level of the horizontal blanking portion in the demodulated video signal is sampled and held by IC51 and C164, and this level is compared with the level produced by demodulating the crystal oscillator output. The comparison output is then sampled and held again by IC52 and C165 and fed back to the modulator in the form of a DC voltage. As a result, the FM modulator is controlled so that the oscillation frequency of the pedestal portion tallies with the frequency of the crystal oscillator.
The FM modulator output is sent to the recording amplifier as the recording signal and to the demodulator as the EE signal.

(7) Video recording amplifier (VO-16, RP-32 boards)

The equalizer circuit on the VO-16 board functions to compensate the frequency response, differential gain and differential phase of the FM modulator output. The same circuit also functions to adjust the recording current level. The equalizer output is sent to the recording amplifier on the RP-32 board.
On the RP-32 board, the signal passes through buffer amplifier Q1 and is distributed to the video channel and sync channel recording amplifiers. The respective recording amplifiers function as differential amplifiers in order to reduce interference of noise, and the only adjustment made here relates to the balance of the differential input circuit. The recording current is turned on and off by the initial stage unbalanced-balanced converter section.

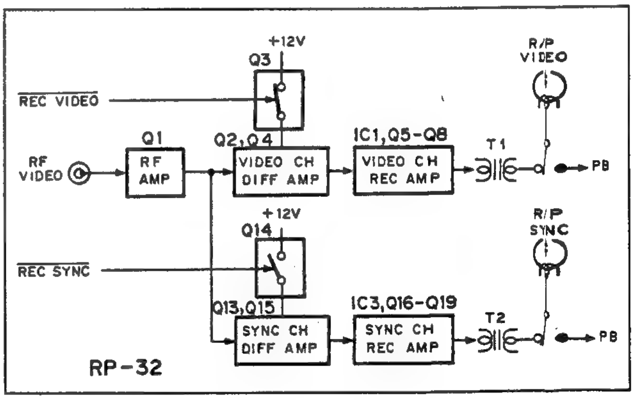


Fig. 4-3-9. Video Recording Amplifier (RP-32)

(8) Rotary erase circuit (RP-32 board)

Erase oscillators are provided both for the video channel and sync channel. The respective oscillator outputs drive the video and sync erase heads through the rotary transformers. The only adjustments made relate to the tuning between the heads and the levels.

4-3-3. Video Signal Playback System (RP-32, DR-13, VO-16 Boards)

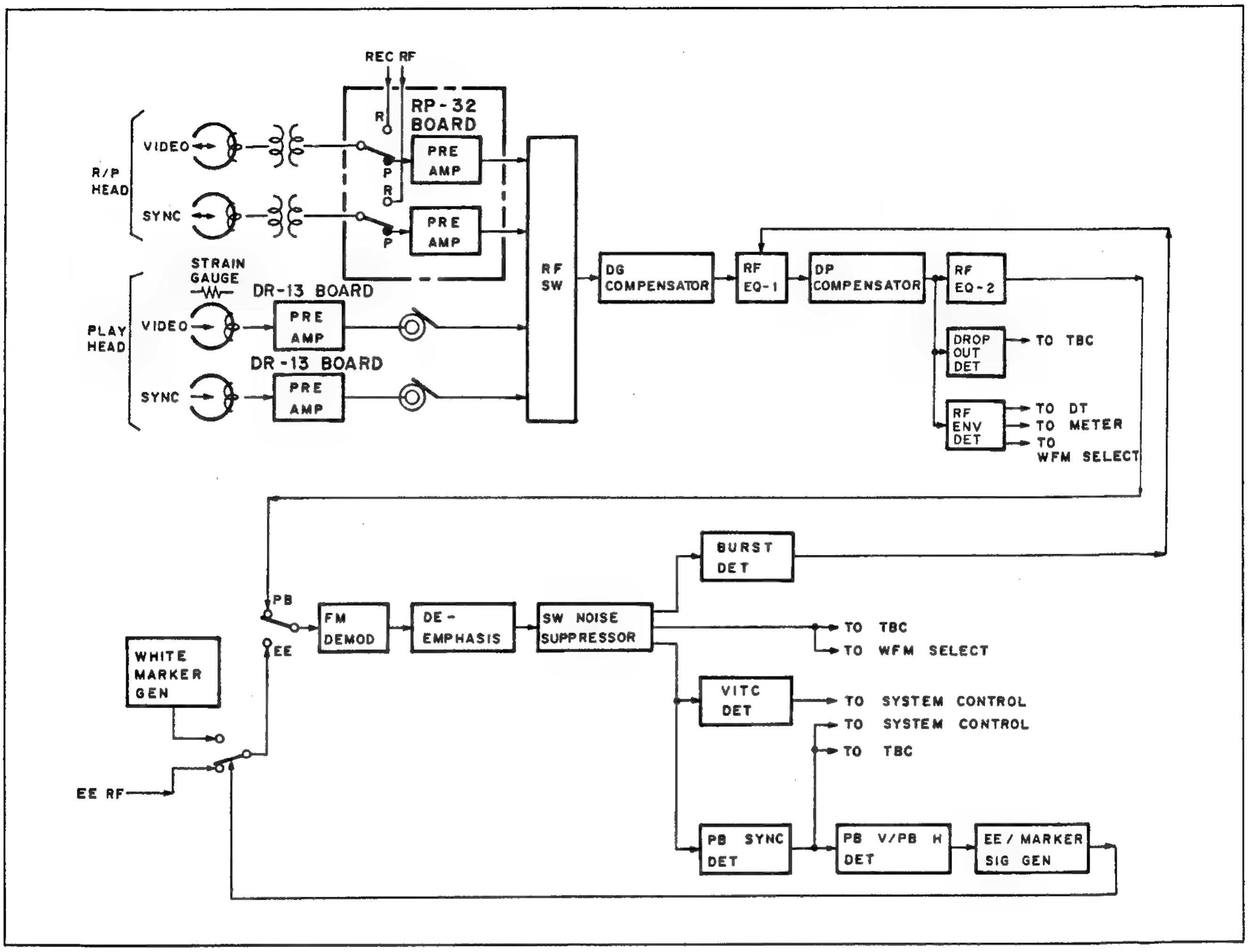


Fig. 4-3-10. Video Signal Playback System (VO-16)

(1) Preamplifiers (RP-32, DR-13 boards)

The preamplifiers for the video head and sync head are composed of a BX1156B hybrid IC for each channel, and their gain is approximately 46dB.
The R/P head preamplifiers are located on the RP-32 board ; the PLAY head (DT head) pre-amplifiers are located on the DR-13 board inside the upper drum.

(2) RF switcher (VO-16 board)

The R/P video and R/P sync RF signals from the RP-32 board as well as the PLAY video and PLAY sync RF signals from the DR-13 board are selected by controller IC15 and 16 and by switcher IC17, 18, 19 and 29.
When the EE mode has been selected, all the switchers are off. The level of the switcher output (TP16) is 100mVp-p.

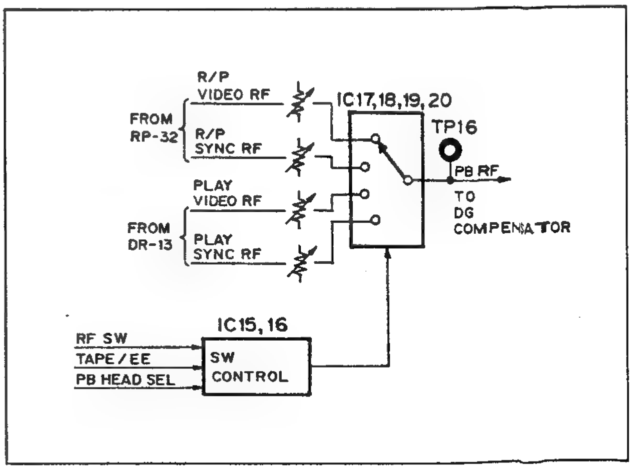


Fig. 4-3-11. RF Switcher (VO-16)

(3) DG compensator (VO-16 board)

The differential gain is compensated by varying the Q of the resonator circuit which is composed of R291, L19, C444 and Q9.
During playback by the PLAY heads, this gain is compensated by the value produced by superimposing the compensation value for the PLAY head onto the compensation value for the R/P head.

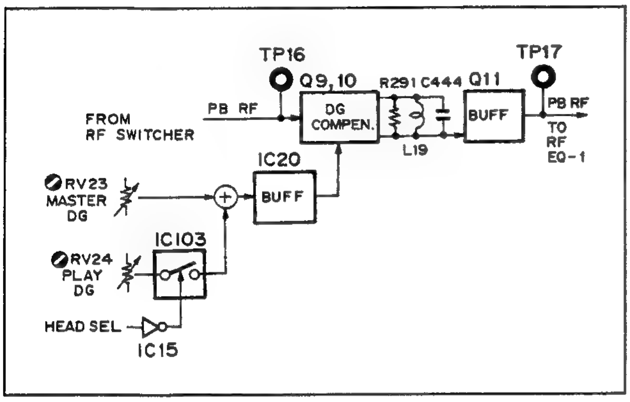


Fig. 4-3-12. DG Compensator (VO-16)

(4) RF equalizer 1 (VO-16 board)

Using a cosine equalizer configuration, the amplitude characteristics are changed without changing the phase characteristics, and the amplitude characteristics of the lower side band of the RF signal are compensated.
The input end of delay line DL1 is impedance-matched but the output end is unmatched with a high impedance. This means that the RF signal is configured as a reflected wave at the output end, that it returns to the input end and that it is superimposed onto the input signal.
If it is assumed that the delay time of the delay line is "t_d" and that input signal "e_a" at point A is "$\sin \omega t$," then signal "e_b" at point B will be equal to "$\sin \omega (t-t_d)$."
Since signal "e_c" at point C is a signal produced by superimposing the input signal and the reflected wave, it is equal to "$\sin \omega t+\sin \omega (t-2t_d)$" which, in turn, is equal to $2\sin \omega (t-t_d) \cos \omega t_d$.
If signal "e_d" at point D is given an attenuation factor of K, then it is equal to $2K\sin \omega (t-t_d) \cos \omega t_d$.
Circuit output "e_o" is the difference between the "e_b" and "e_d" signals and so:

$$e_o=\sin \omega (t-t_d) -2K\sin \omega (t-t_d) \cos \omega t_d$$
$$= (1-2K\cos \omega t_d) \sin \omega (t-t_d)$$

The output amplitude is $1-2K\cos \omega t_d$ and its characteristics are proportionate to the cosine waves.

When attenuation factor K is changed, It is possible to adjust and compensate the amplitude without affecting the group delay response (t_d=constant).
It is possible to select the auto mode in which a DC voltage corresponding to the burst level is fed back in order to keep the burst level of the video signal in the demodulator output constant or the manual mode in which adjustment is made using the equalizer control on the level control panel.

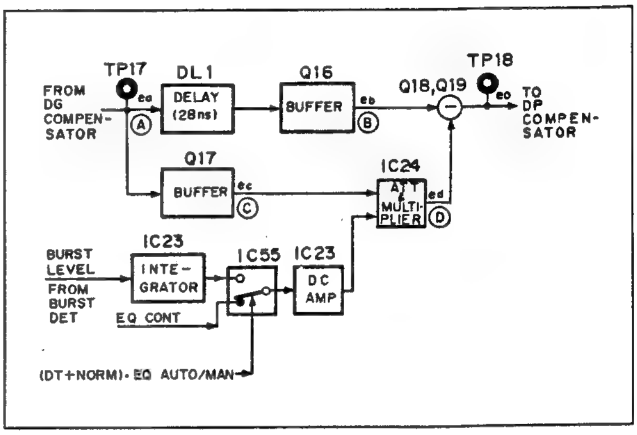


Fig. 4-3-13. RF Equalizer 1 (VO-16)

(5) DP compensator (VO-16 board)

The RF equalizer 1 output (TP18) enters the DP compensator.
The circuit is a phase equalizer composed of differential amplifier IC21 as well as C447, L20, R357 and RV25 and 26. It compensates the differential phase by varying only the phase characteristics without changing the amplitude characteristics. The RF signal whose differential phase has been compensated is then sent to the RF equalizer 2 and RF envelope detector circuit.

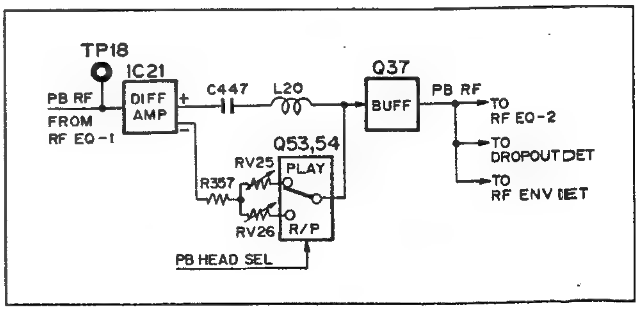


Fig. 4-3-14. DP Compensator (VO-16)

(6) RF equalizer 2 (VO-16 board)

This is the second stage RF equalizer and its configuration does not differ in any significant way from the first stage RF equalizer. It is here that the equalizer adjustments for the R/P head (RV28) and PLAY head (RV27) are made.

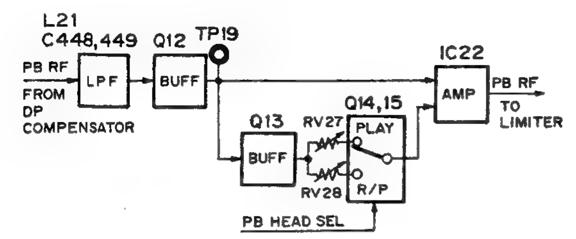


Fig. 4-3-15. RF Equalizer 2 (VO-16)

(7) RF envelope detector (VO-16 board)

One output from the DP compensator enters the RF envelope detector where its peak is detected. The peak detection output signal (TP20) is divided so that 3 separate signals are formed : the RF ENV signal (TP22) for the DT circuit, the RF LEVEL signal (TP23) for the RF meter and the RF ENVELOPE signal (TP24) for the waveform monitor output.
The RF ENV signal for the DT circuit is produced by passing the peak detection output through the buffer amplifier. The RF LEVEL signal for the RF meter is produced by sampling and holding the peak detection output field by field. The RF ENVELOPE signal for the waveform monitor output is produced by inserting a 0V DC voltage using a 9.5 μ sec pulse created from the horizontal sync pulse into the peak detection output.

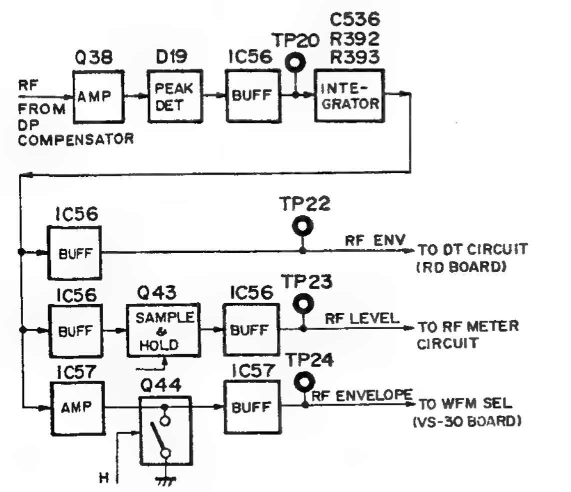


Fig. 4-3-16. RF Envelope Detector (VO-16)

(8) Dropout detector (VO-16 board)

Due to marks, damage or dust on the tape, the level of the playback RF signal may fall sharply and drop below the threshold level of the demodulator. When these variations occur, they are called dropouts and they appear as noise in the demodulator output. The dropout detector circuit serves to detect drops in the level of the RF signal and also to detect the length of the period (dropout width) during which the level has dropped.
The RF signal which has arrived from the DP compensator has its frequency response compensated by Q39 and it is then supplied to the inverted input pin of voltage comparator IC61. Meanwhile, the peak detection output of the RF signal is integrated with the long time constant of R395×C454 (approximately 50msec) and supplied to the non-inverted pin. Any reduction in the RF signal level is detected by comparing these two input levels.
Next, retriggerable monostable multivibrator IC62 is triggered by this voltage comparator output. If the next trigger pulse arrives within the time constant of the monostable multivibrator, the Q output (TP21) level of IC62 is kept high. If it takes a long time before the next trigger pulse arrives or, in other words, if the RF signal is missed, the Q output level is set low. The detection time constant for the dropout length (width) is selected by the operating mode of the VTR. In the FAST BIDIREX mode the time constant is extended while in other modes it is reduced. The DO pulse created in this manner is sent to the CK board and to other boards as well.

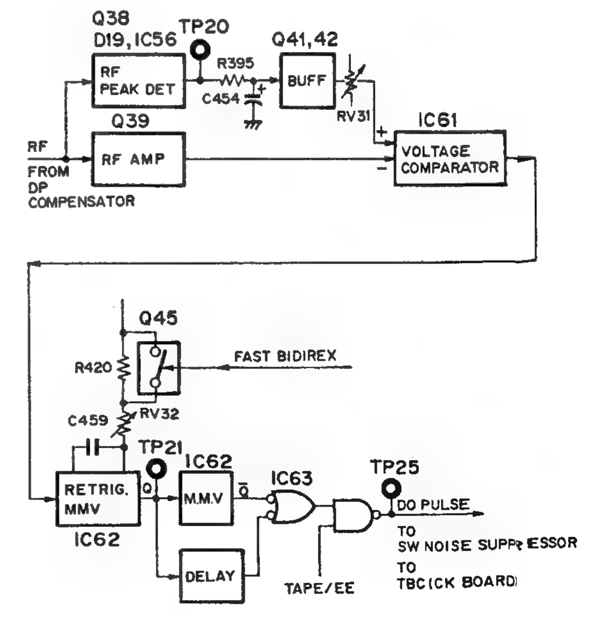


Fig. 4-3-17. Dropout Detector (VO-16)

(9) White reference marker inserter (VO-16 board)

In order to facilitate the deviation adjustment of the modulator, a circuit is provided which inserts the output of the crystal oscillator, whose frequency (10MHz for NTSC ; 8.9MHz for PAL／SECAM) corresponds to 100% white, into the EE RF signal. The insertion of this white reference marker is turned on／off by the select menu [S82. WHITE REFERENCE]. The insertion line is designated by the initial setup menu [I81. WHITE REF INS LINE].

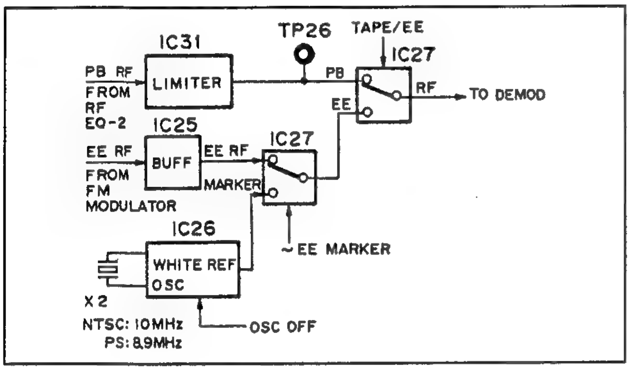


Fig. 4-3-18. White Reference Marker Inserter／EE-PB Selector (VO-16)

(10) EE／PB selector (VO-16 board)

In IC27, the EE signal which has passed through the white reference marker inserter and the PB RF signal (TP26) which has been ECL converted by IC31 serving as a limiter are selected by the TAPE／EE signal.

(11) FM demodulator (VO-16 board)

The configuration of the FM demodulator is described below. One part of the balanced input RF signal passes through a buffer amplifier; another part passes through delay circuit IC32, they are connected in a wired OR format, the (+) and (−) sides are AND-ed and an output is provided. If it is assumed that the amount of delay provided by the delay circuit is "td," then the RF signal is converted into a pulse train with pulse width "td" and with a frequency which is double the input frequency. This output is demodulated into the video signal by passing it through low-pass filter FL3.
In this process, the carrier frequency is doubled and separated from the video band and so this facilitates separation. The output is taken out by a balanced circuit which uses a charge pump and so the basic frequency components of the carrier can be canceled out.
One part of the low-pass filter output (TP28) is supplied to the AGC feedback circuit which is composed of IC36 and 38. This circuit serves to detect the DC level of the pedestal portion in the demodulated video signal and to control the delay time "td" of the delay circuit in the demodulator so that the DC voltage is always 0V.
Another part of the low-pass filter output (TP28) is supplied to the switching noise suppressor circuit via the video amplifier composed of Q31-35 and the de-emphasis circuit composed of Q40, R500-503, RV41, C479 and C480.

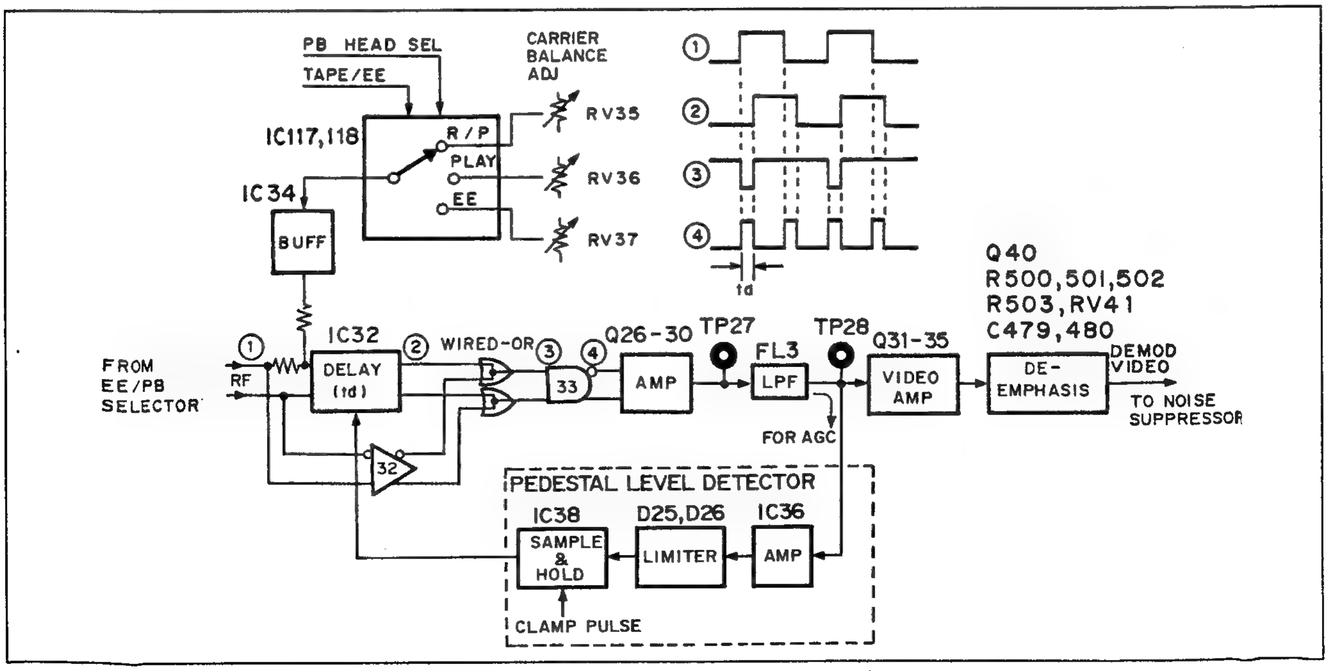


Fig. 4-3-19. FM Demodulator／Carrier Balancer (VO-16)

(12) Carrier balancer (VO-16 board)

One factor which results in the generation of moire is the deterioration in the symmetry of the RF signal waveforms due to non-linearity in the circuit, and this gives way to carrier leak in the modulator output. The carrier balancer circuit functions to DC shift part of the balanced input of the demodulator, control the symmetry of the RF signal waveforms and suppress any carrier leak in the demodulator output.
The DC voltages which have been respectively set at the R/P head side (RV35), the PLAY head side (RV36) and EE mode (RV37) are selected by the analog switchers IC117 and IC118, they pass through buffer amplifier IC34, and they are added to one of the demodulator's balanced inputs by resistors.

(13) Switching noise suppressor (VO-16 board)

The de-emphasized video signal enters the switching noise suppressor circuit where the various types of switching noise listed below and dropouts are replaced by the DC level (pedestal level) determined by RV15.

- Switching noise generated when the PLAY head is selected
- Switching noise generated when the RF signal is selected by the TAPE/EE signal
- Switching noise generated when the white reference marker insertion is selected on/off.
- Dropouts

To deal with the switching noise, 1.9 μ sec pulses are created by IC71 and their period is replaced by the DC voltage.
The noise suppressor output is supplied to 6dB amplifier IC37 and its gain is adjusted by RV16. The video signal then passes through buffer amplifier IC39 and low-pass filter FL2 (TP30) which is mainly designed to improve the signal-to-noise ratio, and it is sent to the two output buffers, IC40 and IC41.

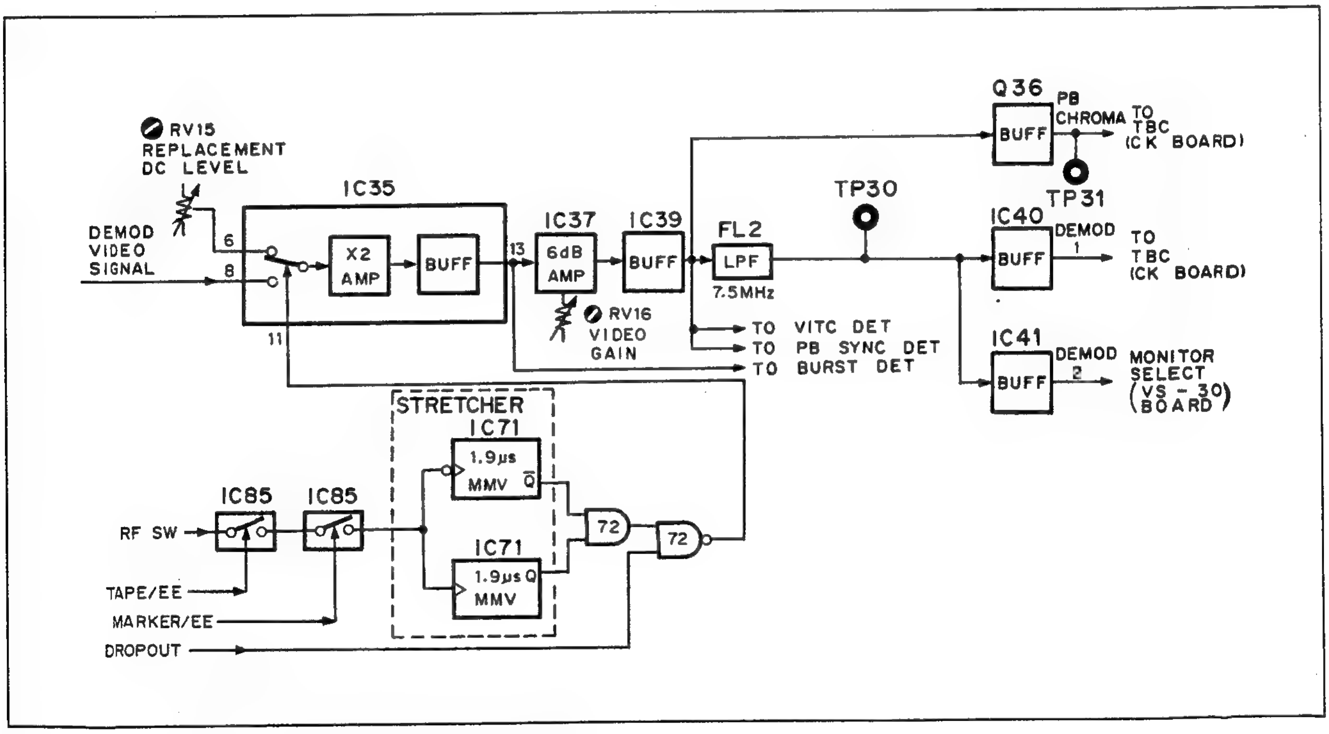


Fig. 4-3-20. Switching Noise Suppressor (VO-16)

(14) PB sync detector (VO-16 board)

The PB sync signal is an important signal which is used as a reference for the servo system and TBC write clock pulse generator, and so careful attention has been paid to how it is detected.
The PB VIDEO signal, which has been output from the 6dB amplifier of the switching noise suppressor, passes through buffer amplifiers IC67 and 68, and through the low-pass filter composed of L13 and C260 where its high-range components are filtered out.
IC69 performs a rough form of sync separation and a positive sync pulse is output. IC111-3, IC70-4 and IC73-12 configure a circuit which rejects half H pulses.
In IC75, the PB VIDEO signal is sampled and heldby the leading and trailing edge pulses of the sync-separated signal, and the sync tip level and pedestal level are both detected. The PB sync signal is produced by comparing in IC76 the voltage of the PB VIDEO signal with that of exactly one-half of the sync tip to pedestal level. This method enables an accurate PB sync signal, which is detected at the half level between the pedestal and sync tip, to be produced even if when such factors as APL fluctuations in the input signal, bounce or defective clamping by the modulator or demodulator are present.

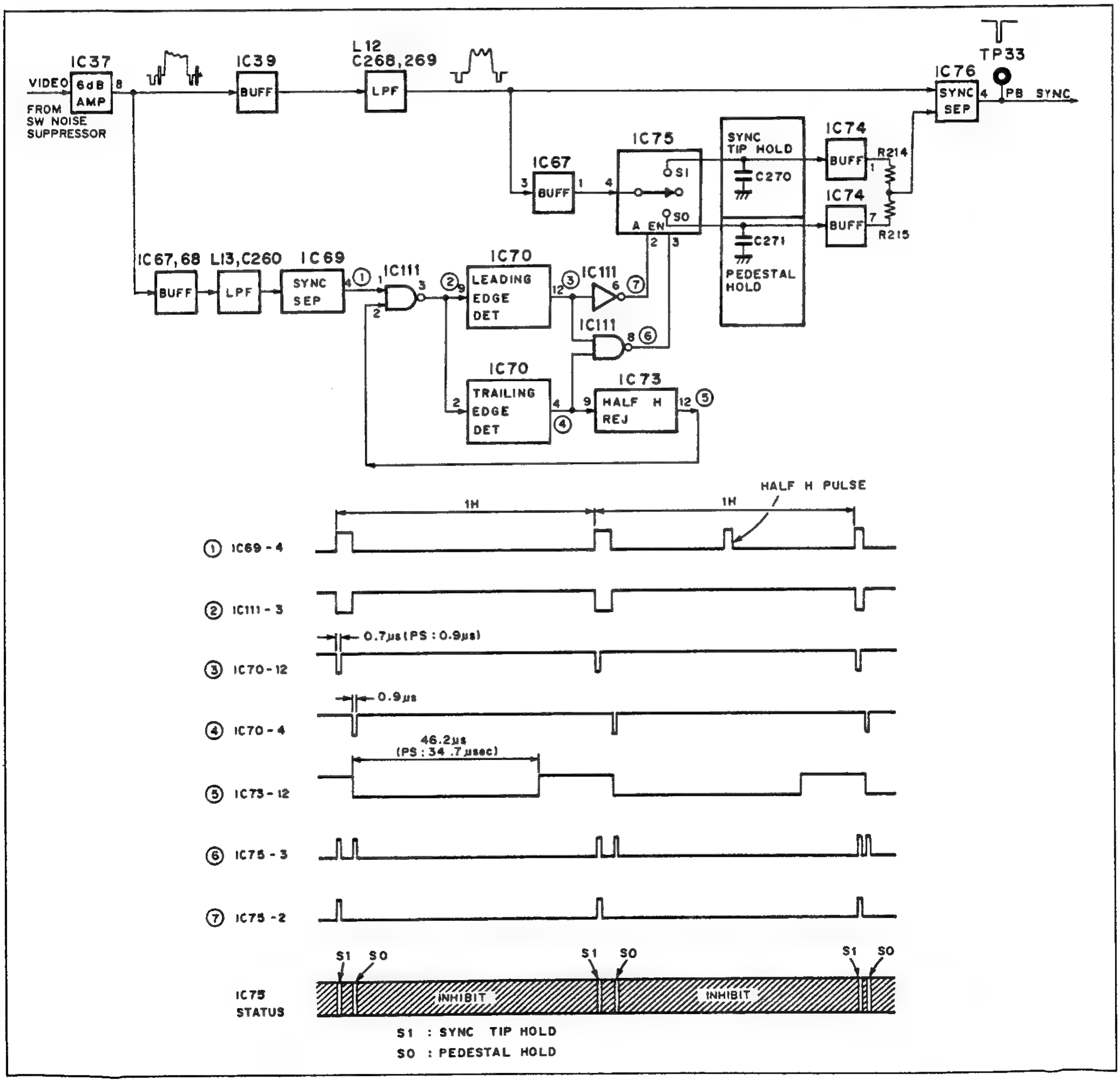


Fig. 4-3-21. PB Sync Detector (VO-16)

(15) VITC detector (VO-16 board)

This circuit serves to create a level corresponding to 40IRE (or 300mV with PAL/SECAM) from the sync tip level and pedestal level which were detected by the PB sync detector, and to compare its voltage with that of the PB video signal. The figure of 40IRE (or 300mV with PAL/SECAM) corresponds to virtually the center level of the VITC signal.

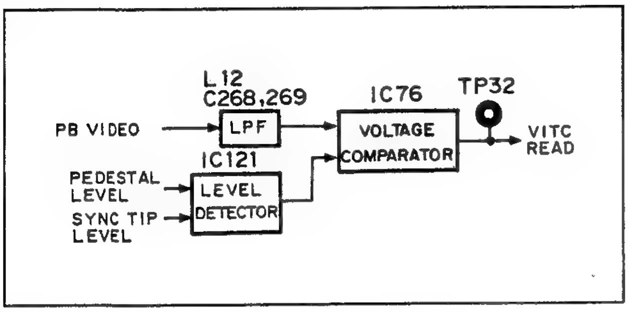


Fig. 4-3-22. VITC Detector (VO-16)

(16) Burst detector (VO-16 board)

This circuit serves to detect the burst level which is used to control the auto equalizer and to detect whether the burst is present or not. The PB video signal which is output from the noise suppressor has its level adjusted by RV17 and its chroma components are separated by the bandpass filter which is composed of L14-16 and C272-274. The envelope of the chroma signal is detected by IC77 and 79. IC80 samples the burst portion of the envelope detection output (TP34) using the clamp pulses generated by the PB sync detector circuit. The sampled signal passes through buffer amplifier IC79 and is sent to the RF equalizer section as the burst level signal (TP35).
This burst level signal detects the level in the vicinity of 0.75V using voltage comparator IC82 and it triggers retriggerable monostable multivibrator IC81 with its pulse width of 15msec. If the burst signal is present in the PB video signal or, in other words, if the PB video signal is the color signal, the IC81 output level is set high.

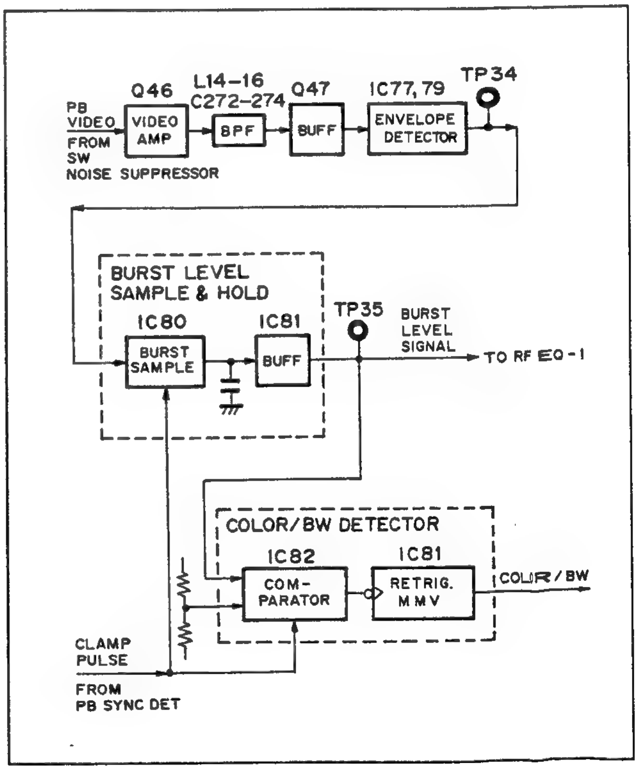


Fig. 4-3-23. Burst Detector (VO-16)

(17) PB V/PB H detector (VO-16 board)

These circuits serve to detect the PB V and PB H signals from the PB sync signal. Their outputs are used to determine the position where the white reference marker is to be inserted and they also serve as the servo reference signal.

In the PB V signal detector circuit, first IC87, 88, 89 and 105 are used to detect the trailing edge of the equalizing pulse before and behind the V sync pulse. A window is applied by the pulse which has a 1/4V width and which is created from the PB V signal for the signal that was detected at the trailing edge of the equalizing pulse, and only the first and second equalizing pulses are taken out.

Next, the second equalizing pulse is detected. Using the first monostable multivibrator IC90 output (pulsewidth of 3/4H), the effective period of the second monostable multivibrator IC90 trigger pulse is limited to a range within 3/4H from the first equalizer pulse, and only the second equalizing pulse is made to serve as the effective trigger. As a result, the PB V signal, which has a width of 1.55msec (approx. 24H) and which has been triggered by the second equalizing pulse, is produced from pin 4 of IC90.

The PB H signal detector circuit is composed of 2-stage monostable multivibrator IC95 which is triggered by the PB sync signal. The first stage functions to reject the half H with pulses having a width of 50.8 μ sec. The second stage functions to create pulses with a width of 4.8 μ sec and to output them as the PB H signal.

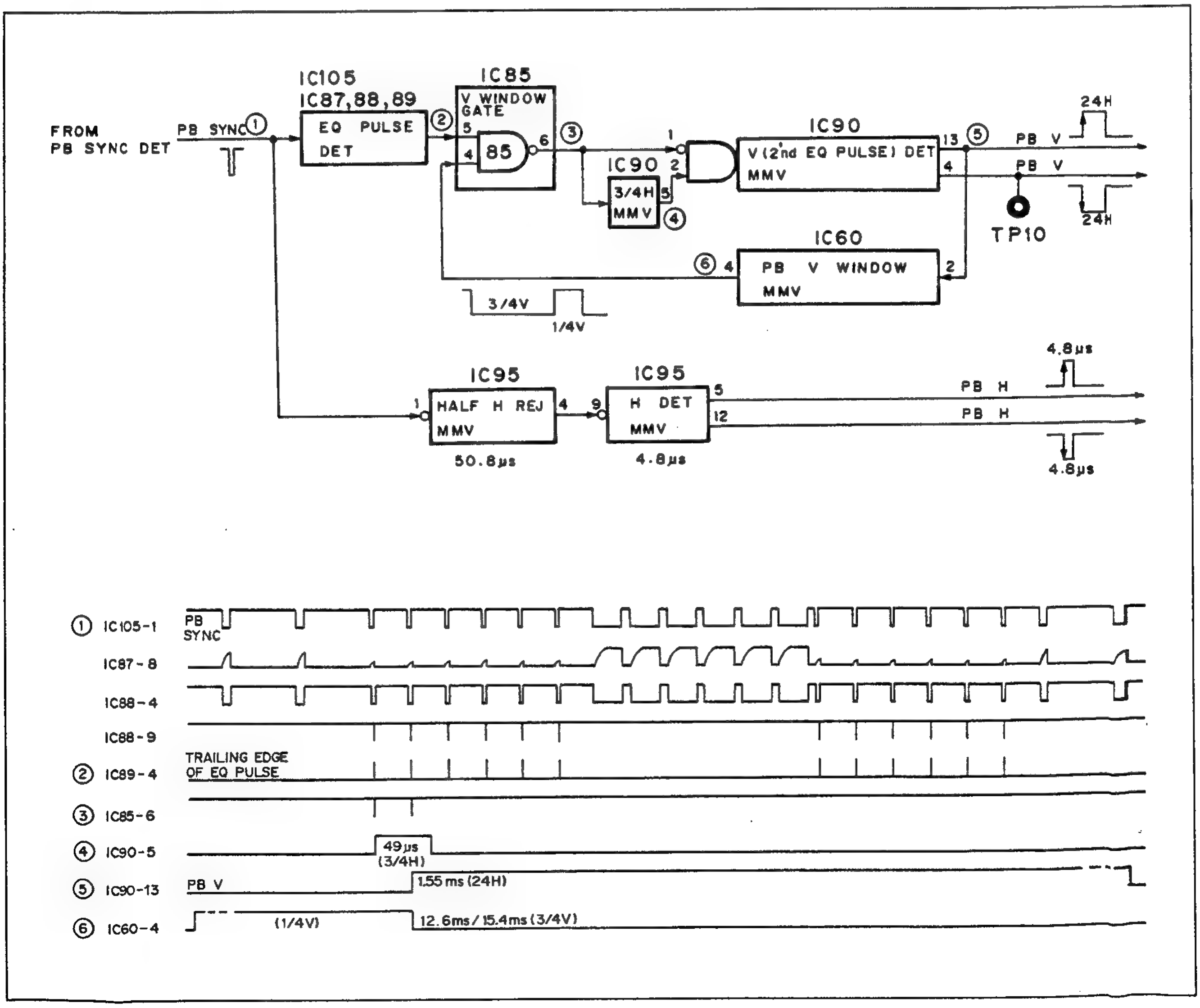


Fig. 4-3-34. PB V/PB H Detector (VO-16)

(18) EE/MARKER signal generator (VO-16 board)

This circuit generates the signal which determines the insertion line and insertion position for the white reference marker which is inserted into the EE signal. The command signal for inserting the white reference marker is sent from the CPU on the SV-90 board to the VO-16 board via the SV bus. Serial-parallel conversion is performed by I/O expander IC99 so that the signal is converted into 8-bit parallel data corresponding to the respective lines, and the signal is then sent to the S0-S7 input pins of multiplexer IC93.

IC92 is a binary counter which is driven by the PB H signal and its output selects one of the S0 through S7 input pins of the multiplexer. The starting point for the count is the starting point for the insertion of the white reference marker and so the timing signal for the insertion starting point is created by IC106 and IC91 from the PB V signal, and this is sent to the enable pin of the counter. As a result, the S0-S7 pins of IC93 correspond to every 2 lines from line No.10 through line No.25 (or line No.6 to 21 and No.319 to 334 in the PAL/SECAM system). IC94 and 96 function to prohibit the marker from being inserted in the horizontal blanking area and to control marker OFF.

(19) I/O expander (VO-16 board)

I/O expander IC99 communicates with the main CPU on the SV-90 board through the SV bus. It converts the time-shared 8-bit serial signals into parallel signals. With parallel ports, the I/O can be freely designated. In this case, 4 ports (PD0, 1, 2, 3) are secured for input applications and 24 ports are secured for output applications.

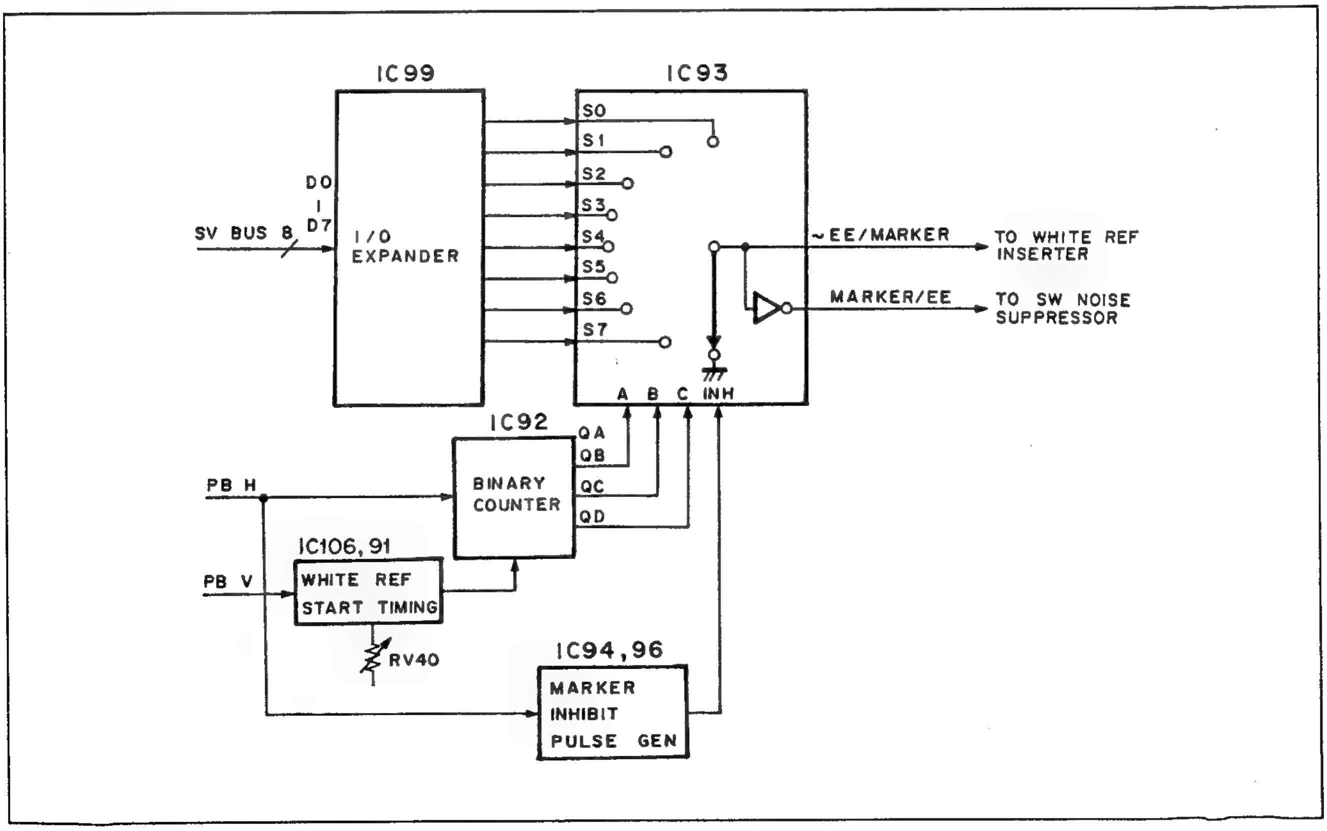


Fig. 4-3-25. EE/MARKER Signal Generator (VO-16)

4-4. TBC SYSTEM

4-4-1. Outline of TBC System

(1) Outline of circuit boards

The TBC system in both the BVH-3000PS and BVH-3100PS is composed of following circuit boards.
- CK-27 board
- RD-7 board
- PR-92 or PR-98 board (BKH-3020 or BKH-3060)

The user selects whether the standard processor PR-92 board/BKH-3020 or the high-quality processor PR-98 board/BKH-3060 is to be used.

(a) CK-27 board
The demodulated playback video signal is supplied to the CK-27 board where it is converted from analog into digital signals, its time base error is corrected and where freeze processing is undertaken. The time base error in the video signal which is caused by the tape/head system is corrected by first writing this signal into the 32-line main memory by the write clock (W CK) signal which is synchronized with the sync signal and the burst signal (the sync signal for the SECAM signal) of the playback video signal and then reading it out by the read clock (R CK) signal which is synchronized with the sync and the burst signal (the sync signal for the SECAM signal) of the reference video signal. The read clock (R CK) signal is generated on the RD board and the write clock (W CK) signal is generated on the CK board. The tape SC-H phase of the PAL signal is also detected on the CK board.

Freeze processing refers to the process of writing the digital video signals, which have been read out from the main memory, into the field memory (4M bits) and reading them out when necessary. This function is used for the following 3 objectives.
- When the still picture mode is specified, the tape tension is released and the field data stored in the memory are read out and then output as a still picture. This eliminates any head-to-tape contact and protects both the tape and the heads.
- While the drum is rotating, the field data stored in the memory are read out and output as a freeze picture to the monitor.
- When the STOP button is pressed in the play mode or DT playback mode, the image applying during the instant when the STOP button was pressed is output as a freeze picture. In the shuttle mode, the image applying during the instant when the tape has stopped is output as a freeze picture only when the PLAY head has been selected.

(b) RD-7 board
The RD-7 board serves to generate the read clock (R CK) signal for reading out the data from the main memory, the reference clock signal for decoding/encoding and the reference signals which are synchronized to the reference video signal, such as the blanking signal, sync signal and burst signal which are replaced by the PR board after D/A conversion. The reference SC-H phase of the PAL signal is also detected on the RD-7 board.
Besides the circuitry which generates the TBC reference signals, the RD-7 board also contains the servo reference circuit and DT control circuit.

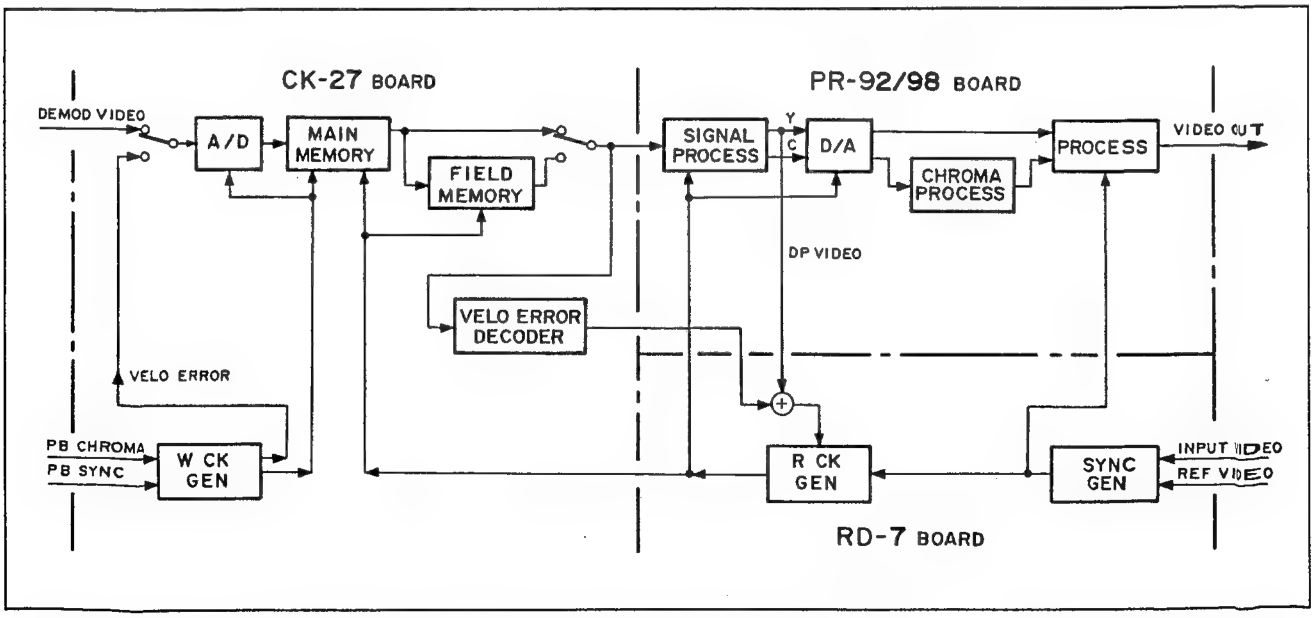


Fig. 4-4-1. Configuration of TBC System

(c) PR-92 board (BKH-3020)

The digital data read out from the main memory and field memory, on the CK-27 board are supplied to the PR-92 board. After the digital data have completed the dropout compensation and Y line adding processes, they are D/A converted and sent to the analog processor circuit.

The analog processor circuit serves to ensure that the chroma signal has the correct phase vis-a-vis the reference burst signal phase during variable speed playback. Also, it replaces the sync signal and burst signal with the sync and burst signals which have been synchronized with the reference video signal. The video level, chroma level and black level (PAL system only) can be adjusted, and dark clipping is also undertaken.

(d) PR-98 board (BKH-3060)

Although the basic circuit configuration of the PR-98 board is identical to that of the PR-92 board (standard processor : BKH-3020), a new Y-line adding and a dropout compensation system which employs adding lines before and after are featured. In particular, the picture quality in the DT mode is greatly improved as a result.

(2) Outline of video signal system

The playback video signal is supplied via the pre-filter on the CK-27 board to the A/D converter which converts it into 8-bit data at a sampling frequency of 4Fsc (1135FH for the SECAM signal). The converted digitial data are written into the 32-line main memory and read out by the 4Fsc (1135FH for the SECAM signal) clock signal of the reference system. The data which have been read out are output to the PR board. The PR board performs such operations as Y/C signal separation, dropout compensation and line adding, it replaces the pedestal level with a constant value and converts the data into an analog signal using its D/A converter. The chroma level and the black level (for PAL only) are controlled, the reference sync signal and burst signal (ID signal for the SECAM signal) supplied from the RD-7 board are added to the signal, and the resulting signal is the BVH-3000PS/3100PS output signal.

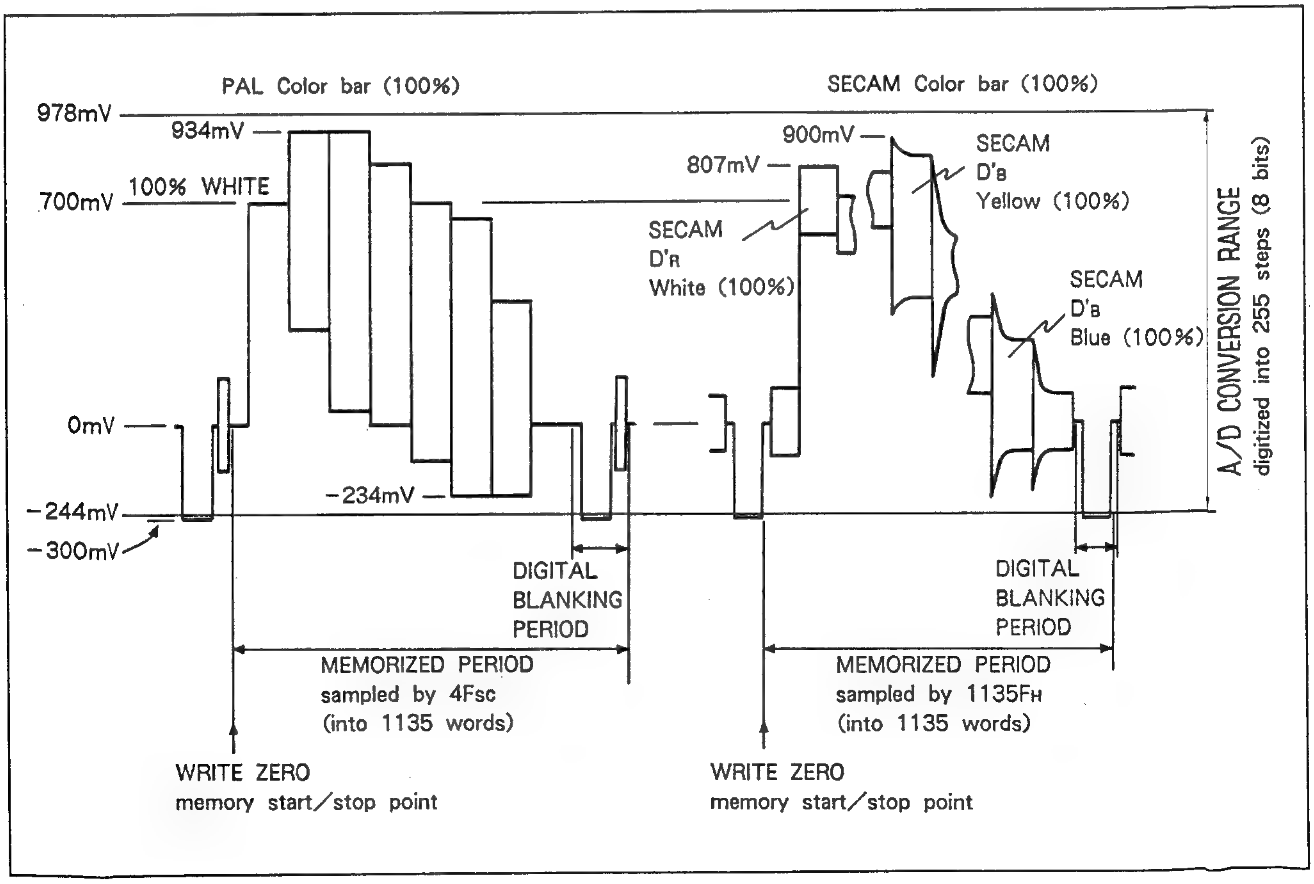


Fig. 4-4-2. TBC Processing of Video Signal

(3) Outline of control signal system

In the case of the PAL signal, the 4Fsc write clock (W CK) signal is generated by the APC system which uses the burst phase of the playback signal as the reference, and this is employed for A/D conversion and for memory writing. In this machine, the time base of the DT playback signal as well as the normal playback signal is corrected. Consequently, the W CK frequency is locked by the AFC to the PB sync signal so that it can be made to track the frequency fluctuations of the playback signals. This generation system enables the W CK signal to be color-locked to the playback signals which are played up to a a maximum of 8 times faster or slower than the normal tape speed. In the case of the SECAM signal, the 1135FH W CK signal is generated by the APC system which uses the PB sync signal as the reference.

The write zero (W ZERO) signal which indicates the start of main memory writing is always generated at a constant timing from the edge of the H sync signal. It is synchronized with the subcarrier frequency W SC signal (produced by dividing the W CK frequency by 4) at the write side. When this synchronizing occurs, the phase of the W SC signal is inverted every 2 lines so as to safeguard against a shift every 2 lines in the timing of the W ZERO signal equivalent to a half cycle of the subcarrier.

In the case of the PAL signal, velocity errors are compensated. The velocity error is detected through phase comparison of the W SC signal with the signal which has the phase of one subcarrier wave near the center of the playback burst signal. The detected error voltage is inserted in the horizontal blanking period of the playback video signal prior to A/D conversion, it is sent to the read-out side via the main memory and the phase of the R CK signal is modulated by means of second order approximation. This provides highly accurate velocity error compensation and reduces the residual phase error during the color processing to less than ±3 nsec.

The R CK signal used for D/A conversion and memory readout is created by multiplying 4-fold the subcarrier which is phase-locked to the burst signal of the video signal selected as the TBC reference signal in the RD-7 board. The TBC reference signal can be specified independently from the servo reference signal. For the PAL signal, the phase of the R CK signal is modulated for both velocity error compensation and DP compensation, and it can be controlled externally so that the burst-chroma phase can be adjusted.

The read zero (R ZERO) signal indicating the read start of the main memory is created at a constant point from the horizontal sync signal, as with the W ZERO signal. The phase of this signal as opposed to the phase of the horizontal sync signal can be adjusted across a 5-step range, with 1 step serving as a subcarrier cycle. This enables the TBC output video phase to be shifted up to a maximum of ±0.45 μ sec. The phase of the subcarrier at the readout side for synchronizing the R ZERO signal is inverted 2-line by 2-line so as to accommodate the phase inversion of the W SC signal. The main memory write address (W ADDRESS) signal and read address (R ADDRESS) signal are created from the W CK and R CK signals. A total of 2k words are allocated to 1 line in the main memory and approximately 1135 words are addressed.

Dropouts are compensated for on the main memory read-out side PR board. The digital video data (WD2") before being written in the main memory are replaced by "1" (FFH) while the DO pulse is input so that the DO pulse which is the signal that indicates the dropouts in the playback video signal is stored in the memory. The "1" (FFH) existing in the original digital video data is replaced with "FEH." The DO pulse is written into the main memory along with the W N/I and W O/E signals which indicate the line inversion of the subcarrier phase on the write side. As with the video data, the written data are read out by the R CK signal of the reference system. The pulse widths and delays of the Y DO signal and C DO signal are adjusted and these signals are used as the timing signals for dropout compensation.

The sync generator is provided on the RD-7 board and this generates the TBC reference sync signals (TBC SYNC, TBC VD) as well as the blanking and burst flag signals. Either the signal supplied to the REFERENCE VIDEO INPUT connector or the signal supplied to the VIDEO INPUT connector is selected and this is input as the external sync signal to the sync generator. The "S86: TBC REF SELECT" select menu decides which of the two signals is selected. In addition, any line from line 7 (320) to line 22 (335) can be selected as the vertical blanking line. The "I80: BLANKING LINE" setup menu decides which line is selected.

The PAL reference video signal and off-tape video signal SC-H phase are respectively displayed by the LEDs on the meter panel.

4-4-2. Input Circuit, A/D Converter and Memory Circuit (CK-27 Board)

(1) Input circuit and A/D converter (CK-27 board)

The DEMOD 1 video signal which has been played back is supplied through R1 to pre-filter LPF1. The output impedances of the VO-16 board is approximately 50 ohms and so the 100 Ω R1 resistance is added here for LPF1 impedance matching. The level of the LPF1 output is first adjusted by RV1 and then the signal is amplified 6 dB by ICB21.

Fixed bias is applied by RV2 to the ICB21 output and pedestal clamping is provided by IC3, B19 and B17. The pedestal level is determined by RV3.

The pedestal-clamped signal enters the ICC17 A/D converter where it is converted into 8-bit digital data by the 4Fsc write clock signal, and then its ECL level is converted into the TTL level by ICF17 and E17.

Fig. 4-4-4 shows the A/D conversion range. In the case of the PAL signal, the velocity error (an analog voltage) is inserted into the horizontal sync section. Switch IC3 is used to switch between the velocity error signal and the main signal line. As described in the following section, the Y DO, C DO, W N/I (PAL system only) and W O/E (or line identification with SECAM system) information is added to the digital video data which have just been A/D converted.

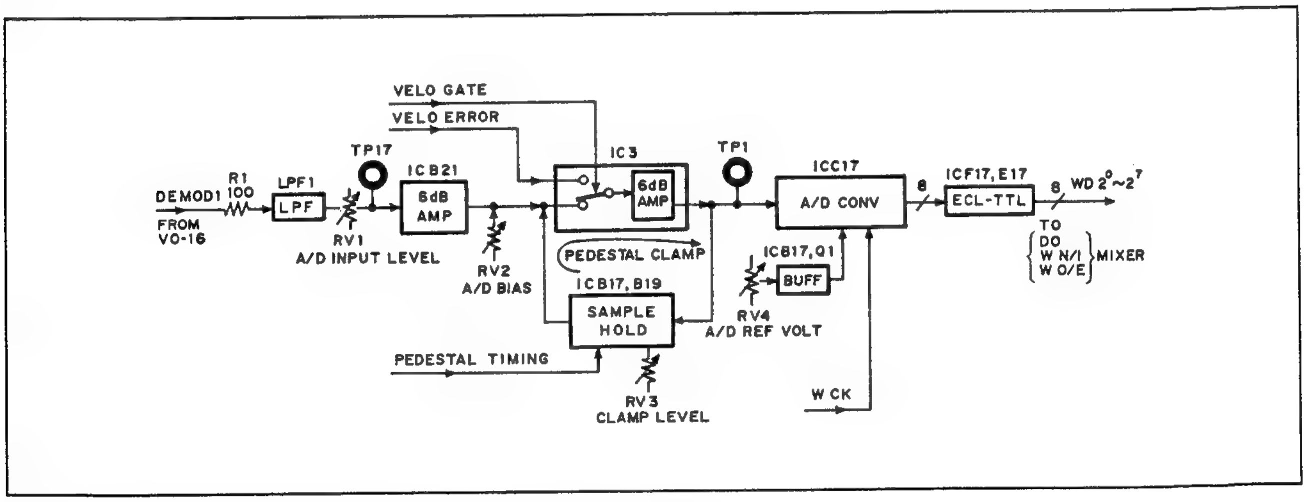


Fig. 4-4-3. Input Circuit and A/D Converter (CK-27 Board)

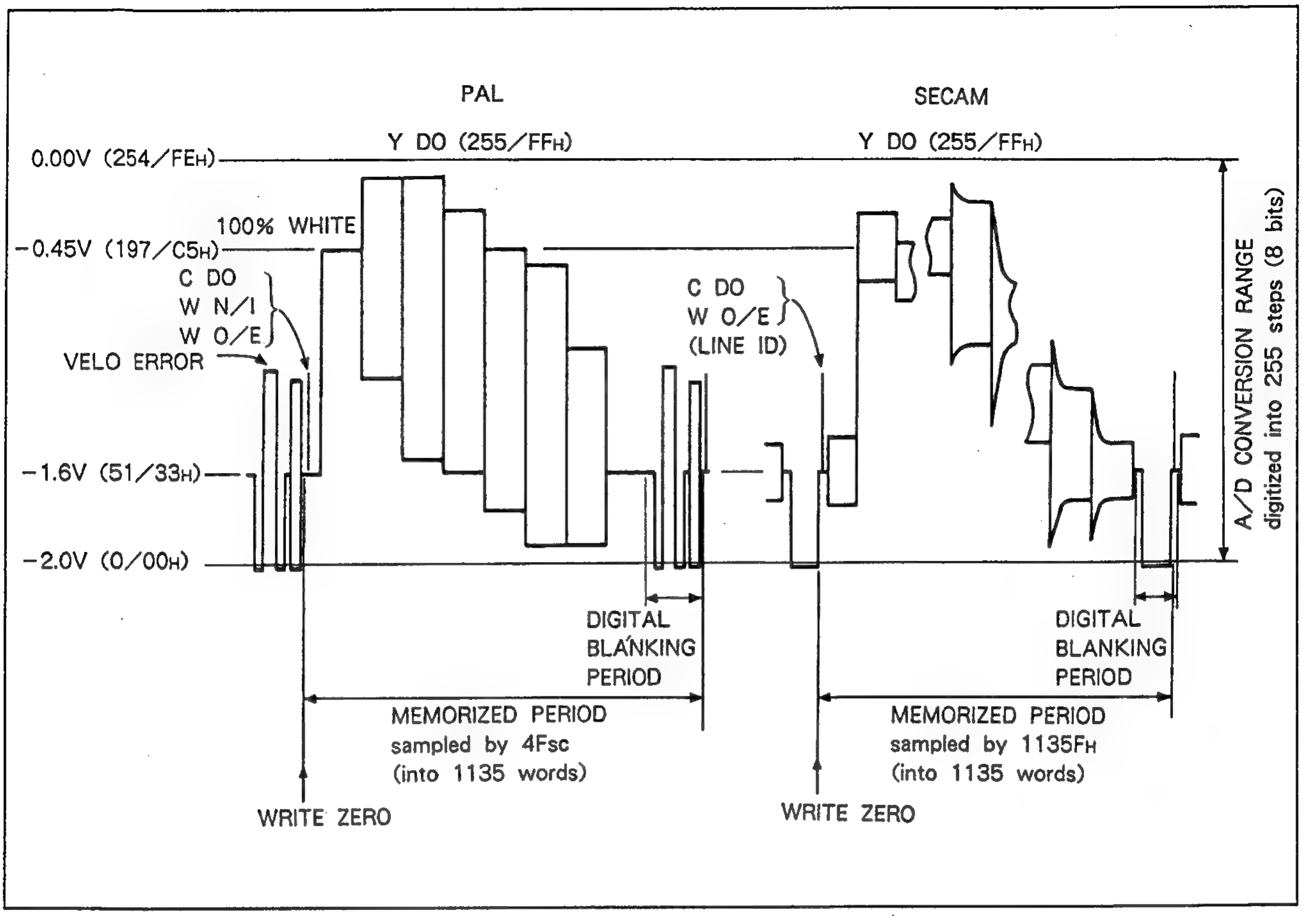


Fig. 4-4-4. A/D Conversion Range (TP1/CK-27)

(2) DO pulse, W N/I and W O/E mixer (CK-27 board)

It is here that the following signals are added to the 8-bit digital video data.

- Y DO (Y dropout pulse)
- C DO (chroma dropout pulse)
- W N/I (write normal/invert signal) : PAL system only
- W O/E (write line odd/even signal with PAL system ; DR' /DB' line ID signal with SECAM system)

The Y DO signal is added as FFH so as to accommodate the video data with the clock rate. Therefore, when FFH is in the video signal, it is treated as the DO pulse and so it is clipped to FEH so that it does not exist in the video data. The clipper is configured by ICF16 and ICJ12. ICF14 and ICF15 together replace the Y DO pulse with FFH and also add the C DO, W N/I and W O/E signals by means of the timing pulse. The C DO, W N/I and W O/E signals are 1-bit information per 1H and they are added at a position which is delayed by an amount equivalent to 2 clock pulses from the W ZERO signal.

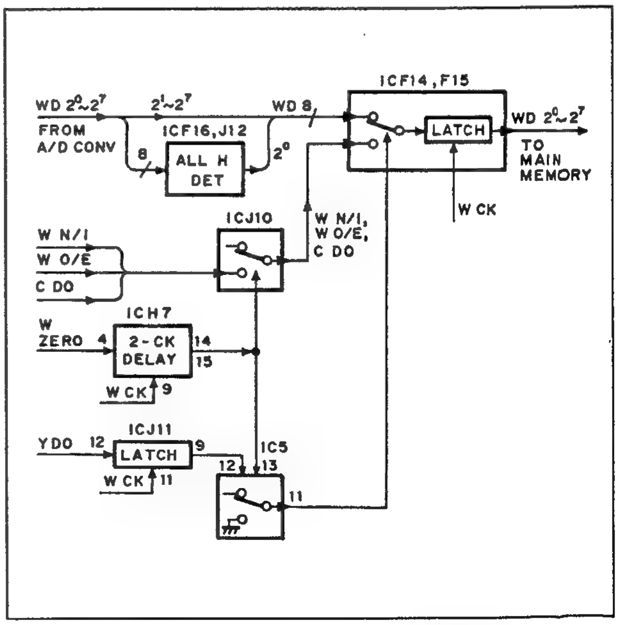


Fig. 4-4-5. Y DO, C DO, W N/I, W O/E Mixer(CK-27)

(3) Main memory (CK-27 board)

ICE14 and E11 (CXD1020Q) are a 1-8-1 serial-parallel-serial (S-P-S) converter. Eight MB8464 8k×8-bit SRAMs are used for the memory for a total size of 31 lines.
This section features a configuration which takes into account the fact not only that the write and read systems are not synchronized but also that the frequencies change.

The 30 Hp-p window is given to the memory since it is convenient for a ± (7H+ α) memory window to be provided even during DT playback at speeds ranging from +3 to −1 of the normal tape speed. Furthermore, during playback at +50 normal tape speed, the write clock signal has a frequency of approximately 27 MHz and sufficient access time to the memory is provided by the 8-phase serial-parallel-serial conversion.

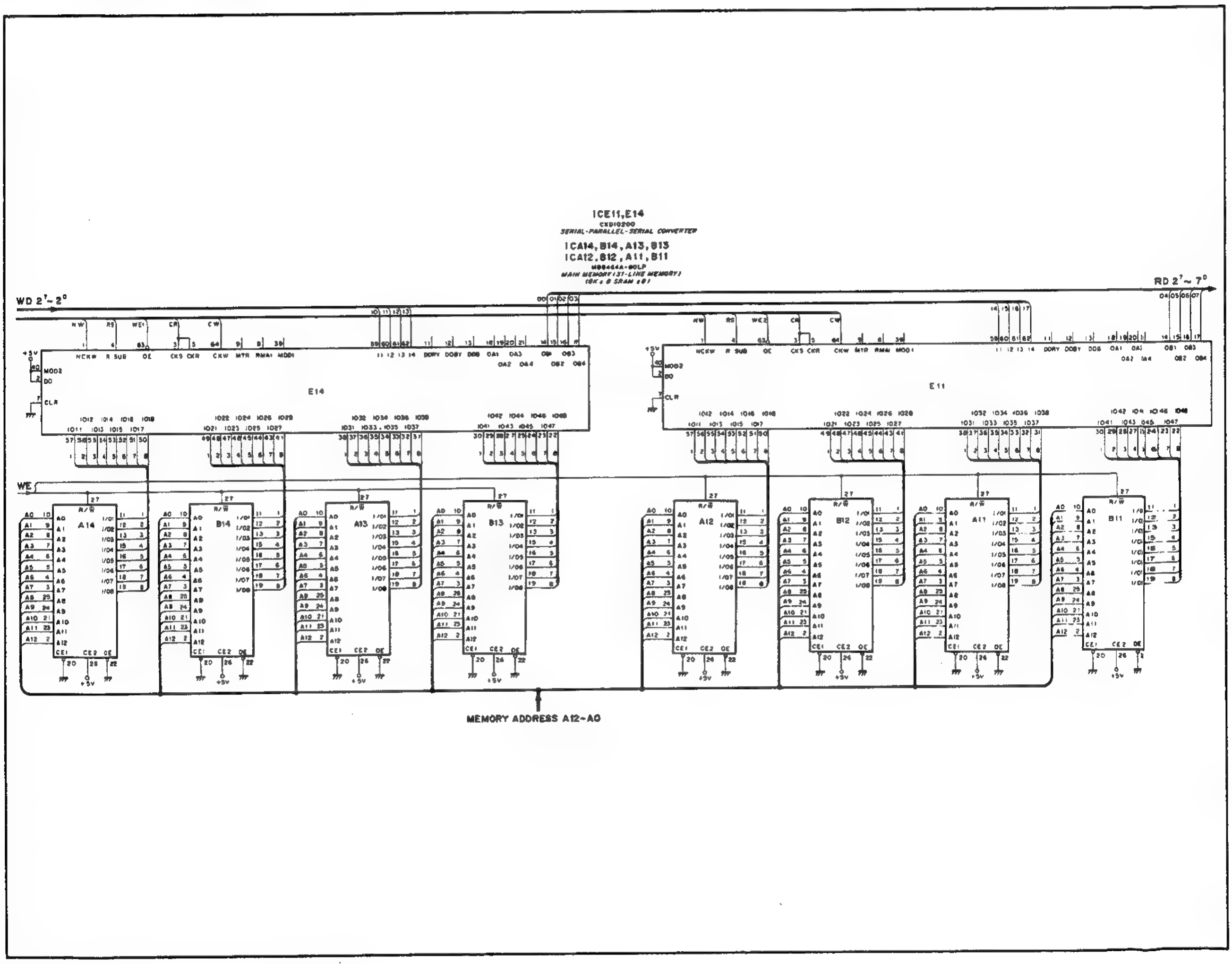


Fig. 4-4-6. Main Memory (CK-27)

Memory control is outlined below.
The 11-bit counter is configured by ICG7, G8 and G9 and 00 0000 1000 is loaded with each R ZERO signal. This is how the read addresses are created. Since an 8-phase drive is featured, the upper 8 bits form the read address which is set in address 1 by loading 00 0000 1000.

The write addresses are created by ICH9, H10 and H11. As with the read addresses, they are composed of the upper 8 bits. NCKW which is created by ICJ9, and J12 is the timing pulse for the serial-parallel conversion of serial-parallel-serial converter ICE14 and E11.

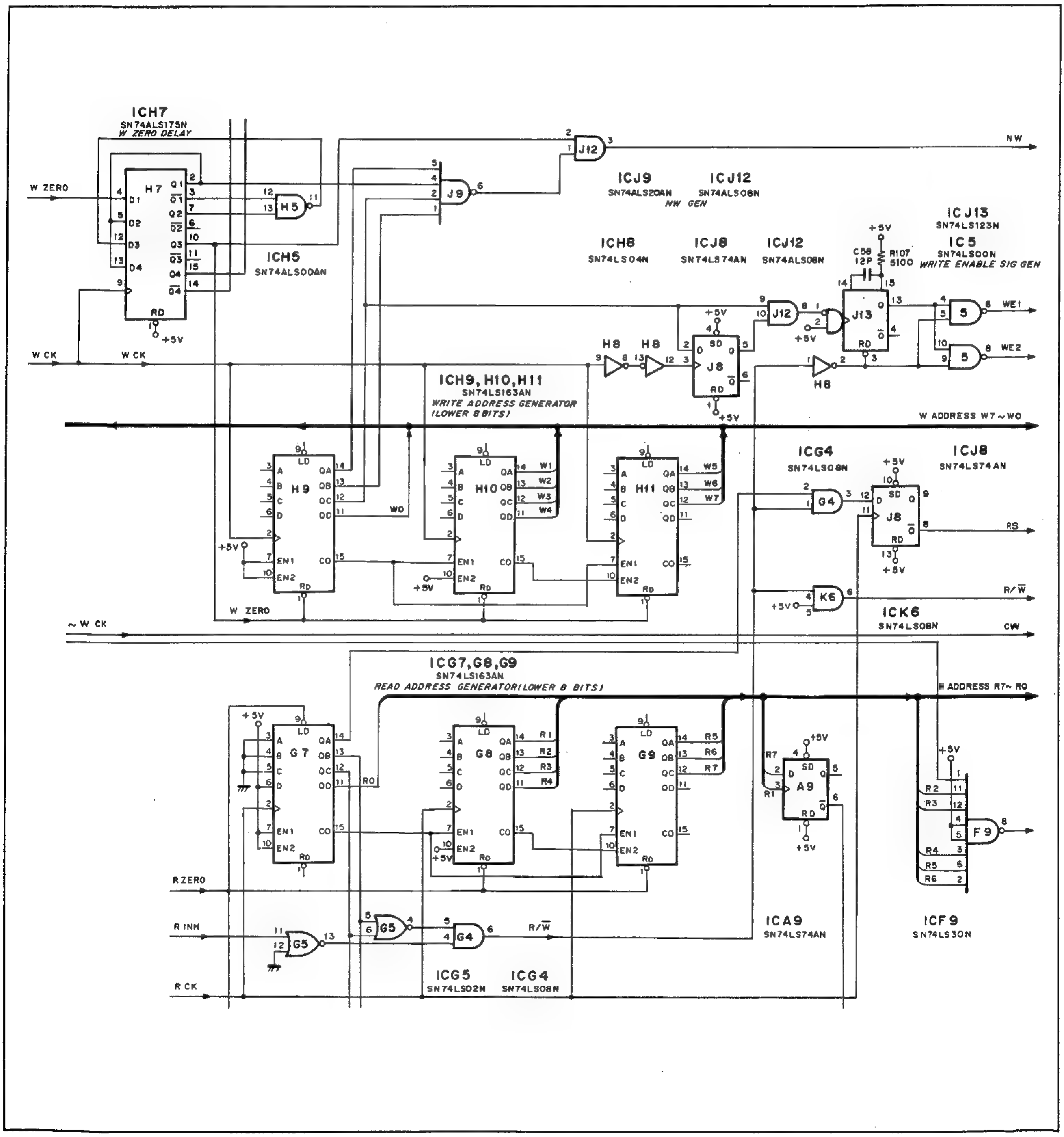


Fig. 4-4-7. Address Generator and Memory Control (CK-27)

The significant point of the memory control is the WE (write enable) signal generator which is configured by ICJ8, J12, J13 and IC5. The main memory circuit performs 3 read/write operations per one cycle by 8-phase.
The WE signal generator decides whether writing is possible or not and when it is possible, it outputs the WE signal. This is shown in Fig. 4-4-8. Since the write and read systems are not synchronized, this figure shows 3 different cases. In case 1, an attempt is made to trigger monostable multivibrator ICJ13 at pin 8/ICJ12 but since pin 2/ICH8 (read cycle) is low, the WE signal (pins 6 and 8/IC5) is not set low. Instead, the monostable multivibrator is triggered at the pin 2/ICH8 rise and the WE signal is output (set low) after the read cycle has been completed. In case 2, at times when the read cycle has arrived after the WE signal has been output, WE is output again upon completion of the read cycle. In such cases, writing is done twice. In case 3, it is not possible for writing to be done twice. When the second WE signal is incomplete, the writing will not be done properly the second time even if it is done properly the first time. In order to avoid this, a pulse with a width enabling the W cycle is output from pin 8/ICJ12 and the monostable multivibrator is not triggered at the pin 2/ICH8 rise.
The lower 8 bits of the memory address are obtained by switching between the read address and write address by means of ICF10 and F11 using the R/W signal. The lower 8 bits are the address inside 1 line. The memory addresses are composed of the lower 8-bit address and of the higher 5 bits which determine the line address. The higher 5 bits represent the V LOCK and memory jump controlled address.

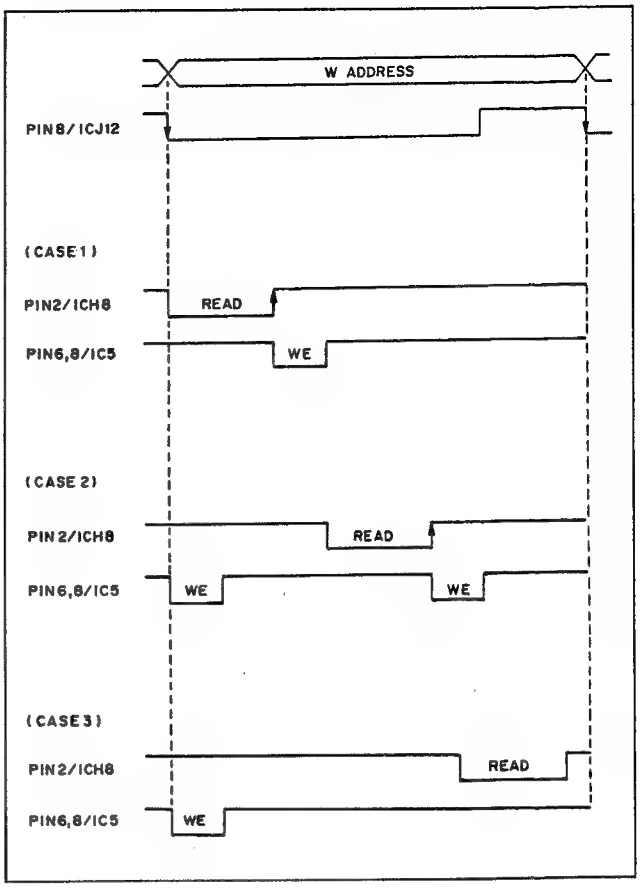


Fig. 4-4-8. WE Timing Chart (CK-27)

(4) V lock and jump control (CK-27 board)

ICG15 and H14 are the write line address generator and ICG14 and H15 the read line address generator. ICH13 and J15 provide memory jump control. ICF12 and G12 are the line address selector. The value of the write line address is latched by ICJ14 at the SEL PB V timing and this is then loaded in ICG14 and H15 by the SEL REF V timing. As a result, the read line address generated by ICG14 and H15 is locked to V. In order to read out from 2H before the velocity error which has been inserted into the sync section, ICF13 adds 2 to the read line address in this section.

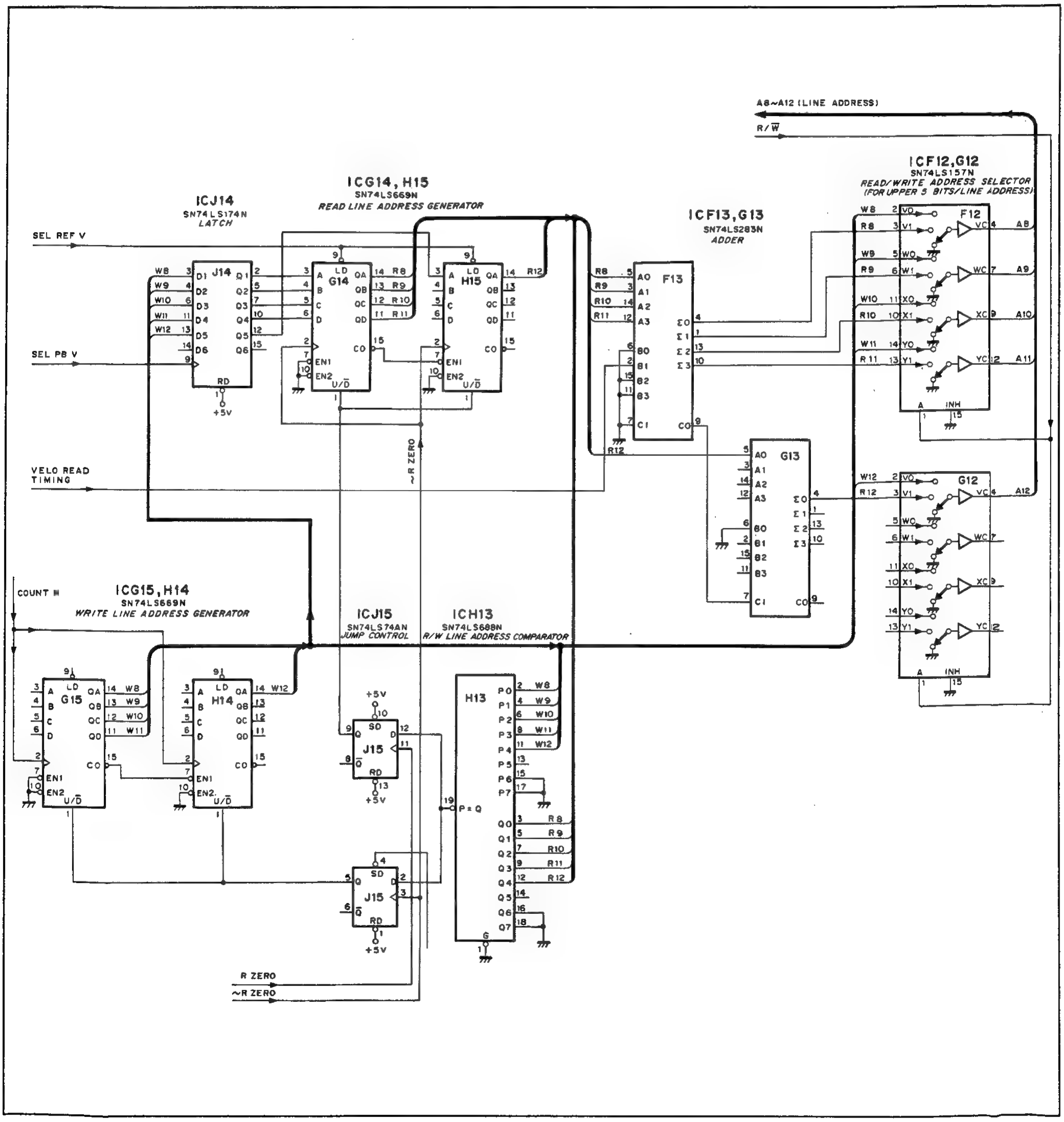


Fig. 4-4-9. Line Address Generator and Address Selector (CK-27)

The process described next is "jump control". When there is no time base error, the digitized video signal is written into the main memory at a timing which is 16H ahead of the readout timing. In other words, the write address is normally 16H ahead of the read address, as shown in Fig. 4-4-10, but in the variable speed play, it may advance by a further 16H and catch up with the read address or, conversely, it may be delayed and the read address may catch up with the write address. At times like these, the picture will shift by 32H. In order to safeguard against this, the address which has caught up is returned to 1H before when either the write or read address has caught up with the other.

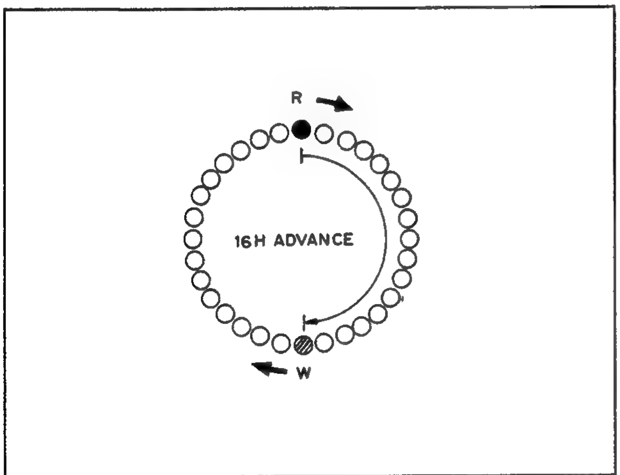


Fig. 4-4-10. Write/Read Phase

ICJ15 serves to judge whether the write address or read address has caught up with the other. Fig. 4-4-11 is a timing chart. When, as shown in the figure, the write address is behind the read address, the comparator ICH13 output is set low after the read address, it is latched at the timing of the trailing edge of the R ZERO signal and pin 9/ICJ15 is set low. In this case, the U/D (up/down) input of the ICG14 and H15 read address counter is set low and the read address is returned to 1 before. Conversely, when the write address is ahead of the read address, the ICH13 output is set low before the read address, it is latched at the timing of the leading edge of the R ZERO signal and pin 5/ICJ15 is set low. The U/D input of the write address counter is set low and the write address is returned to 1 before.

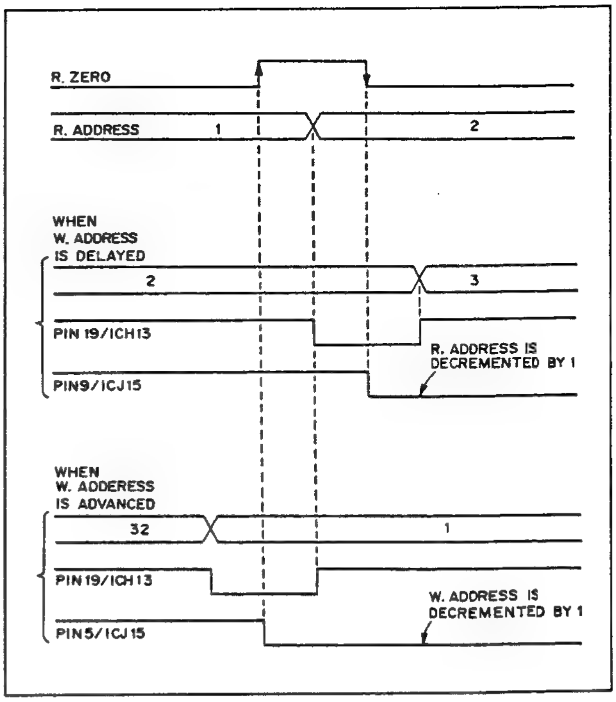


Fig. 4-4-11. Jump Control Timing (CK-27)

The V lock operation is now outlined. This determines the V phase of the TBC output picture, and 16-line locking applies with the BVH-3000PS/3100PS. The 16-line locking means that the 16-line write address of the playback signal is latched at the SEL PB V timing and then loaded at the SEL REF V timing into the read address corresponding to 16 lines of the reference signal.

ICJ1 is the SEL· REF V signal selector which exercises control in two different ways. One way is V locking in the zero advance state which means that the vertical phase is delayed by 4H when the PB signal (including EE) is not in advance of the reference signal. The second way is used for vertically shifting the picture for the V SHIFT mode and Y ADD mode during DT playback. 0, −1H and +1H control is exercised by the RD CONT 1 and RD CONT 2 signals sent from the PR board.

RD CONT 2	RD CONT 1	DELAY
0	0	0H
0	1	−1H
1	0	+1H
1	1	0H

ICK2 is the SEL PB V signal selector. The PB V signal is mostly correct and the DT V signal is in its correct phase during ×1 speed playback (NOR mode) and during DT playback, which means that the DT V (rise) signal is selected in the EE or NOR DT mode and that the pulse created from the REF VD signal is selected during bidirex playback since the DT V signal cannot be relied upon.

ICK3 controls the freeze memory V phase. As with ICJ1, it is controlled by the RD CONT 1 and RD CONT 2 signals. This operation is coupled with Y ADD on/off and the same picture quality is achieved in the DT still picture and freeze modes.

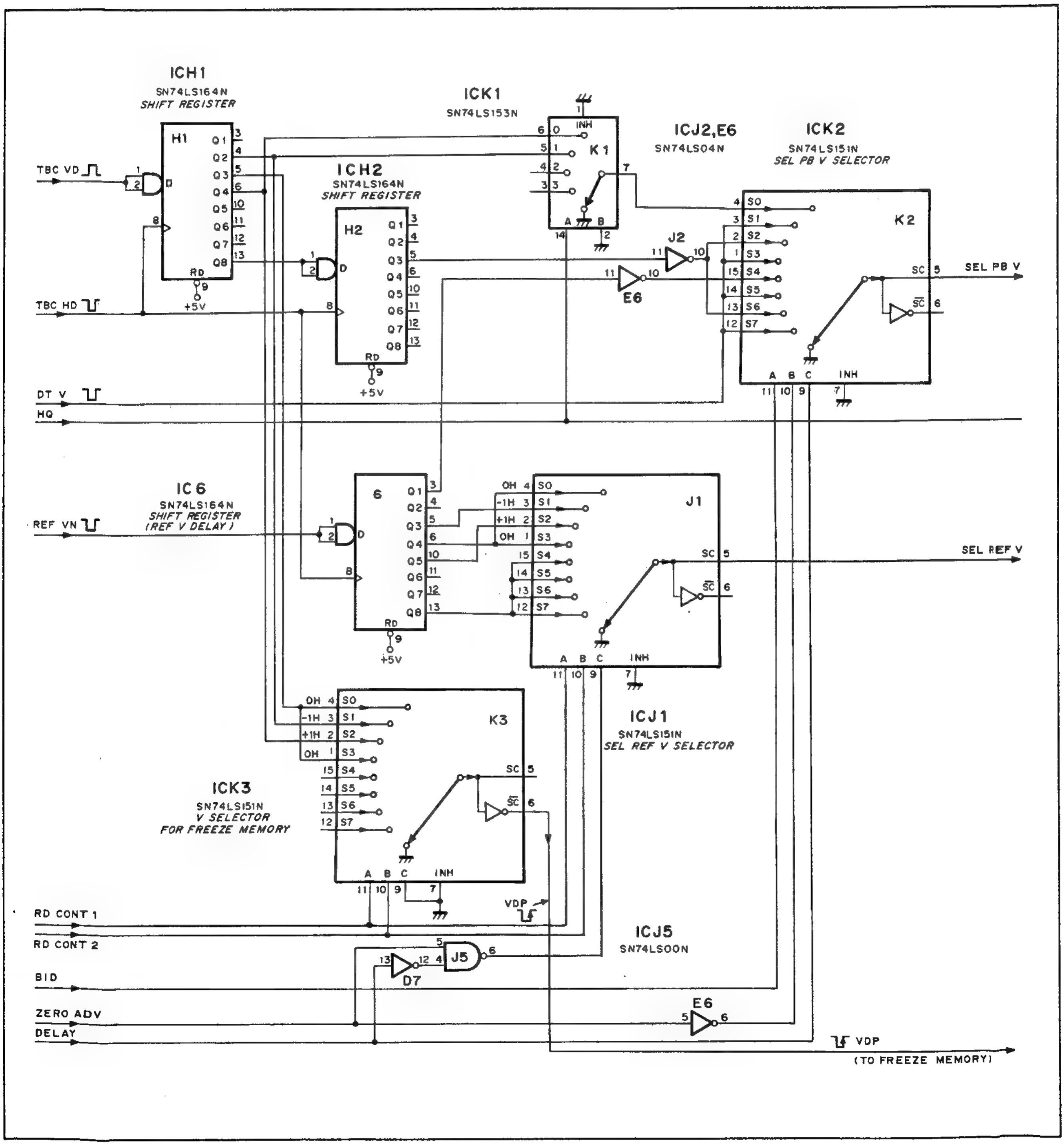


Fig. 4-4-12. V Lock Timing Signal Generator (CK-27)

(5) Freeze memory (CK-27 board)

The data whose time base error has been removed in the main memory are sent to the main signal line circuit and freeze memory circuit.
ICD2 and D5 are a 1-8-1 serial-parallel-serial (S-P-S) converter. Sixteen MB81464 64k×4 DRAMs are used for the memory to store the data of one field. One line is configured with 1135 samples but because of its memory size the freeze memory stores only 1024 samples. The remaining 111 samples (6.26 μ sec) are allocated to part of the blanking period and they are replaced when output from TBC. In the case of the SECAM signal, the start of the data writing into the memory is before the burst signal and this burst signal is also stored. In the case of the PAL signal, the start of the writing is after the burst signal.

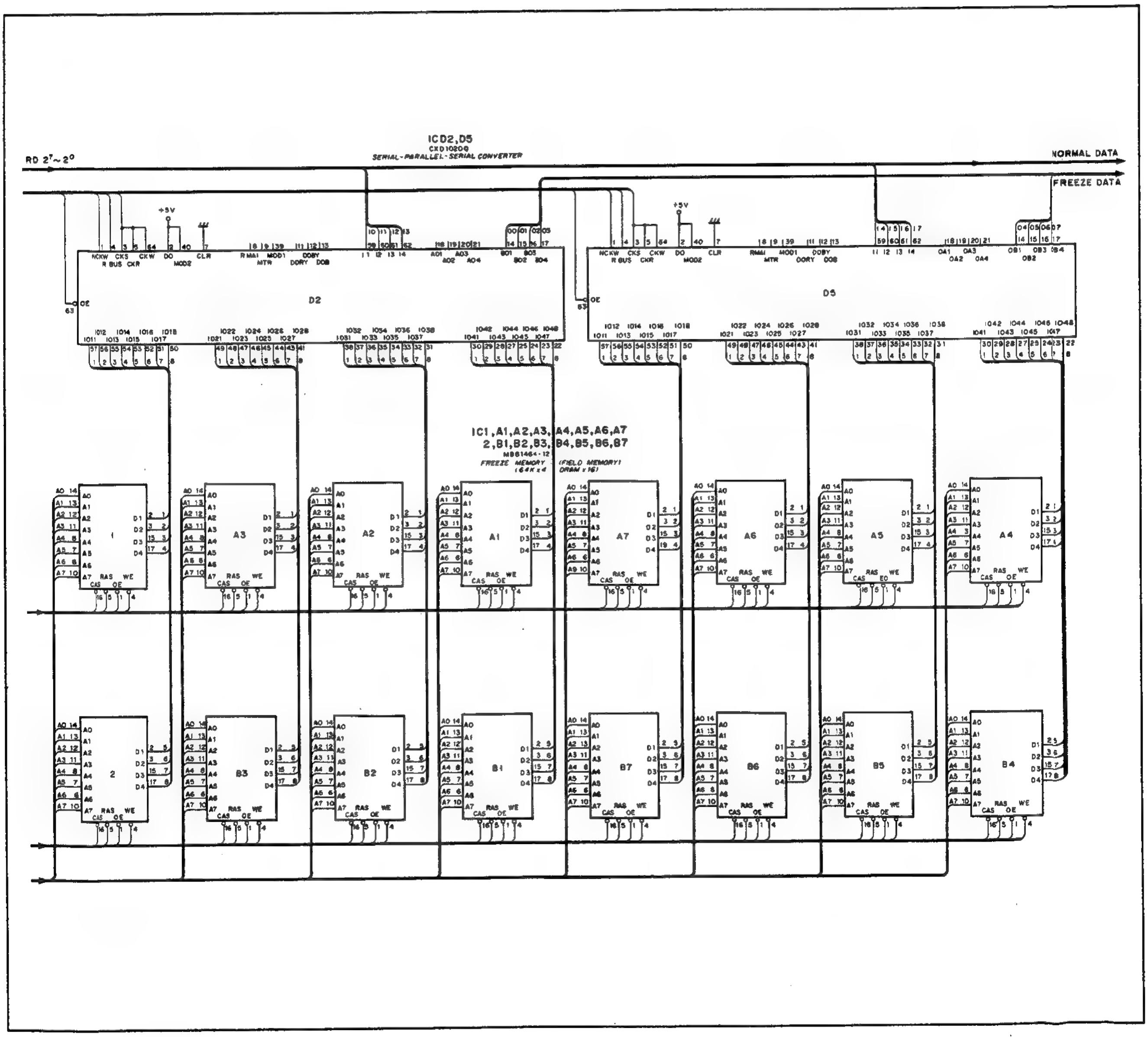


Fig. 4-4-13. Freeze Memory (CK-27)

ICD8, D9 and D10 generate the address within 1 line and this becomes the lower 8-bit address. ICC10 (or ICC8, C9 and C10 with a CK-27 board bearing the -11 suffix) generates the line address and this becomes the upper 8-bit address. ICB9 and B10 configure the RAS/CAS address selector of the DRAM. In order to obviate the need for DRAM refreshing, the lower address is set to RAS and the upper address to CAS.

The reason why the FREEZE signal is input to the D preset pin of address generation counter ICD8 is so that the data will be read out 1 address earlier and so that the delay in the freeze memory output will be reduced. This operation is the same as that for the main memory in that during write operations the data are written not from address 0 but from address 1.

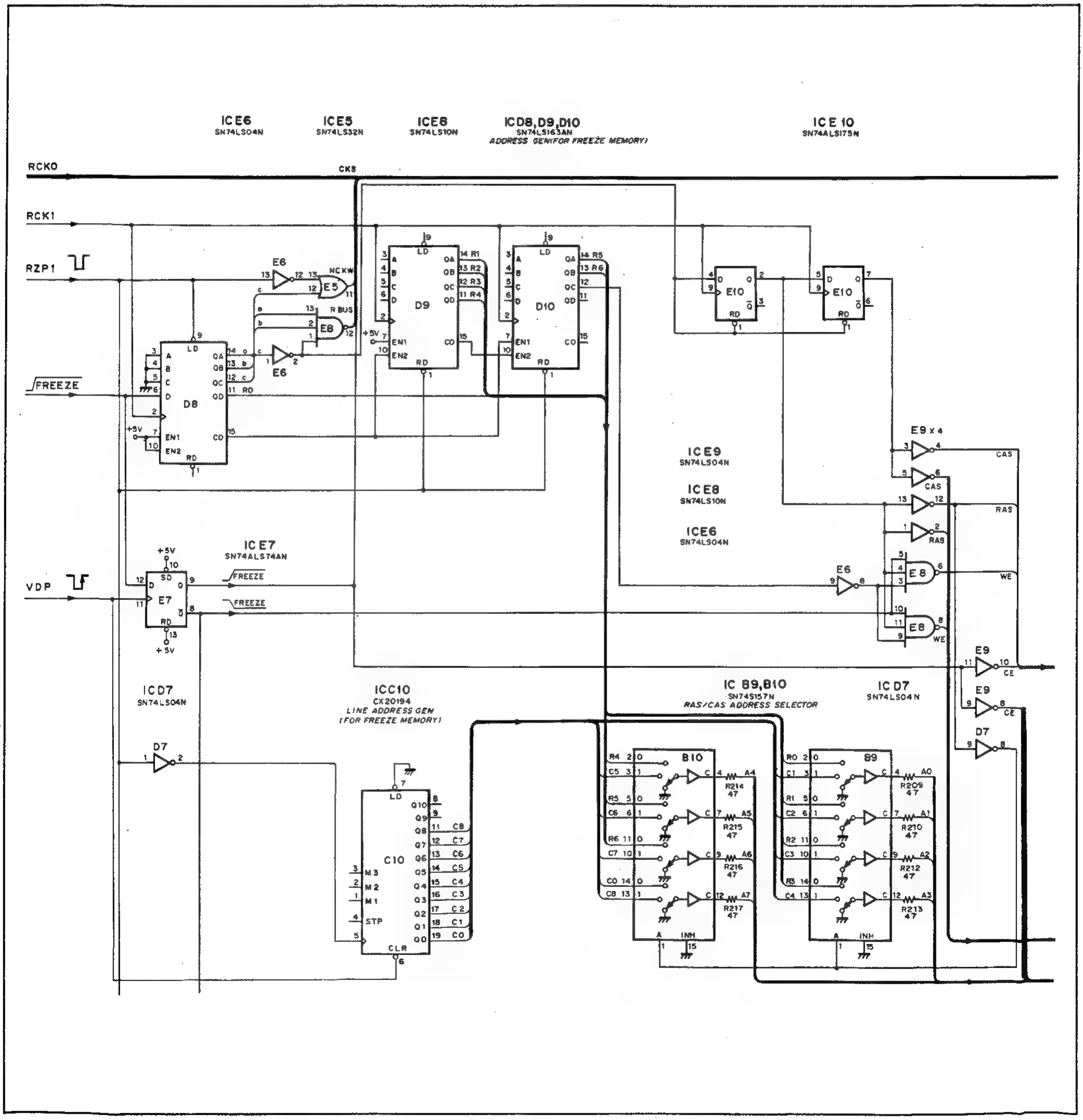


Fig. 4-4-14. Freeze Memory Address Generator (CK-27)

(6) Y DO, C DO, W N/I and W O/E decoder (CK-27 board)

Either the normal data or the freeze data are selected by ICF5 and F6. ICF8 and F7 provide the normal data with a 7-clock pulse delay so that the data will be matched with the delay in the freeze memory.

After having passed through the NORMAL/FREEZE selector, the 8-bit data sent to selector IC102 and 103 which determines whether they are to be delayed by 1H in ICF4 (μ PD41102C) or whether they are to bypass this IC. In the normal playback mode, the 1H delayed data are selected by the RD CONT 3 signal when there is mismatching in the write side and read side odd field/even field.

The Y DO pulse inserted as FFH is decoded by the ICE4 NAND gate, latched by ICG2 and output to the PR board. Pin 4 of ICG2 is a guard which prevents an incorrect Y DO pulse from being output due to a data error in the vicinity of the W ZERO signal. The C DO pulse has been inserted in the section at the start of each line of the data 2^2 and so it is decoded by the signal delayed from the W ZERO signal and output to the PR board.

The 8-bit data selected by IC102 and 103 are 1H delayed by IC101, latched by ICF1 and then output to the PR board. The 1H delay provided by IC101 is supplied for SECAM dropout processing. If there are any dropouts in the Y signal in the case of the SECAM signal, the chroma signal of the whole line is replaced with the chroma signal in the previous line. Thus, the read data are 1H delayed by IC101, the Y DO signal is detected from the data prior to the delay and this is made the C DO signal.

The W N/I and W O/E signals, which were inserted into data 2^1 and 2^0, are similarly decoded and output to the PR board.

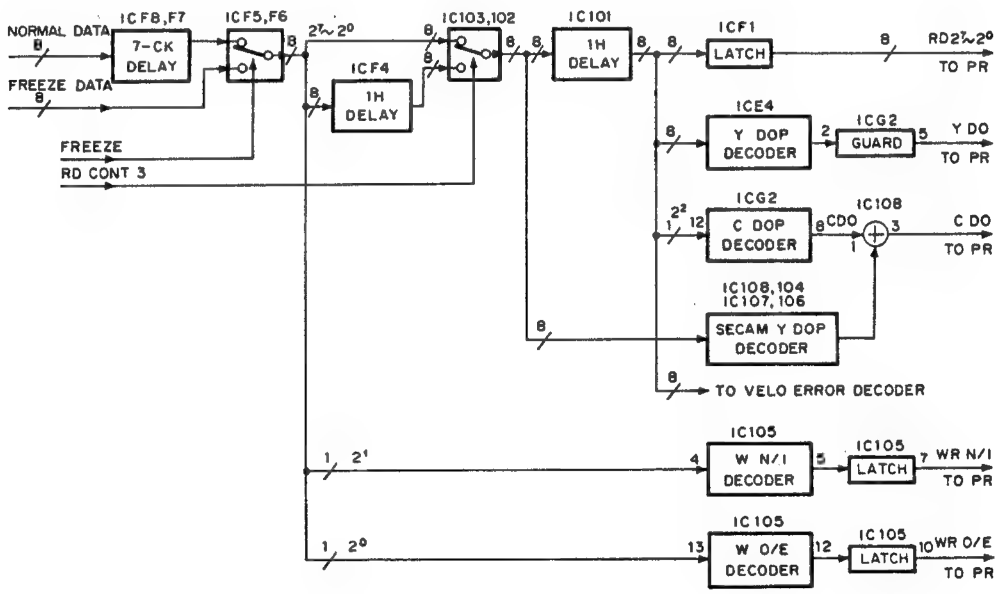


Fig. 4-4-15. Y DO, C DO, W N/I and W O/E Decoder (CK-27)

(7) Velocity error decoder (CK-27 board)

The velocity error inserted into the main signal line sync section is decoded by ICE3 and after its timing is adjusted by ICE2, it is D/A converted by ICE1 and output as analog data.
Since the velocity error data inserted into the video data are delayed 2H behind the video data, they are read out 2H ahead by this decoder.

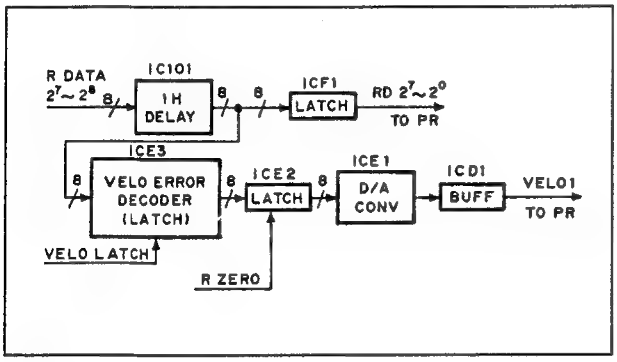


Fig. 4-4-16. Velocity Error Decoder (CK-27)

4-4-3. Write Clock Generator (CK-27 Board)

The 4Fsc write clock signal of the PAL signal is generated by the APC based on the burst signal which is taken out from the PB CHROMA signal and on the 4Fsc signal which is generated by the AFC from the PB SYNC signal.
In the case of the SECAM signal, the 1135FH write clock signal is generated by the AFC and APC with the PB SYNC signal serving as the reference.

(1) PH (PAL H) generator (CK-27 board)

The purpose of this circuit is 3-fold: (1) in the case PAL signals, to remove the PAL offset from the H pulse period so that the AFC frequency locked to the horizontal sync is not 1135FH but 1135FH + 100 Hz, (2) to identify any pulses with a width below 3.6 μsec from the PB SYNC signal as noise and to remove this noise, and (3) to reduce the burden placed on the W ZERO loop in the color mode during variable speed playback and to reduce the range which must be tracked.
Sawtooth waveforms with a 1V/μsec ramp are generated by C40, Q10, Q9 and ICL19 from the PB SYNC signal fall timing. The TAPE SPEED signal (a tape speed of ±50 times normal tape speed is equivalent to ±4.5V with the TAPE SPEED signal) which is supplied to the Q9 and ICL19 constant current source serves to control the current in accordance with the changes in the PB SYNC pulse width and to make the amplitude of the TP8 sawtooth waves constant. During variable speed playback, this has the effect of eliminating the same amount of noise as that during normal speed playback and of reducing the burden placed on the W ZERO loop.
The sawtooth waves generated in this way are sliced by DC 3.6V (TP9) in the ICK19 comparator. As a result, PB SYNC pulses below 3.6 μsec are eliminated.
In the case of PAL signals, the PB CF adjustment voltage and V rate sawtooth waves are added to the slice voltage of the comparator in order to eliminate the PAL offset from the H pulse period. The value of the PB CF adjustment voltage is based on the PRESET (DC 0V), LOCAL (RV9) or remote control setting. It is selected on the [S88. PB CF DET MODE] select menu. ICM21 is an integrator which generates the V rate sawtooth waves by discharging the integrating capacitor with the V pulses. By adding the sawtooth waves generated by ICM21 to the slice voltage, the leading edge phase of the H pulse in the comparator output is modulated and the PAL offset is eliminated from the H pulse period.
In the case of SECAM signals, the integrating capacitor is shorted and ICM21 outputs a constant voltage.
The comparator output is supplied to the ICG19 D-type flip-flop. The PB SYNC signal guarded by the DO pulse is supplied to the ICG19 clear pin and ICG19 removes the dummy sync which is present in the slow bidirex mode. The leading edge of the ICG19 output is the reference timing of the latter stage circuitry and its trailing edge is reset by the trailing edge of the PB SYNC signal. The signal which is output from ICG19 is known as the PH (PAL H) signal.

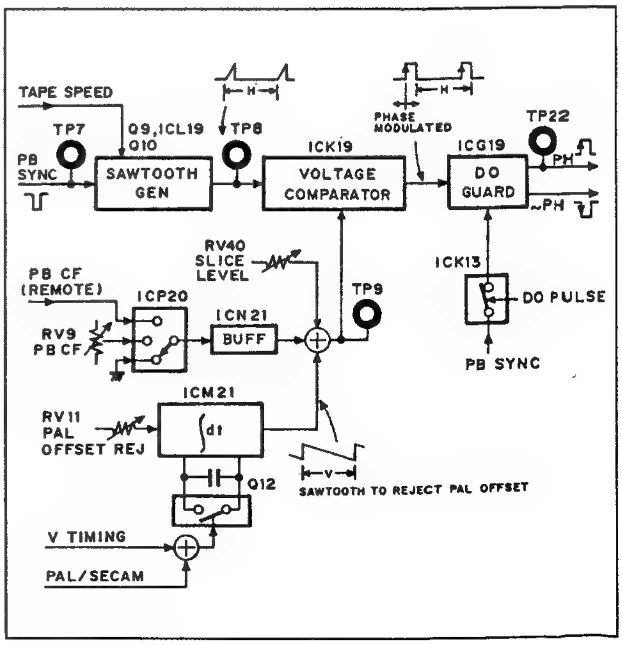


Fig. 4-4-17. PH Generator (CK-27)

(2) SELECT H circuit (CK-27 board)

This circuit focuses on the periodicity of the sync signals, it removes as noise the discontinuous pulses among the PH pulses (PB H signal) which is output from the PH generator circuit, and it prevents the AFC operation from being disturbed by noise. Conversely, in the fast bidirex mode (more than ±8 times normal tape speed), this circuit is bypassed so that as many PB SYNC signals as possible are obtained even if the AFC is disturbed. Fig. 4-4-18 is the SELECT H circuit block diagram and Fig. 4-4-19 is its timing chart. A pulse with a width of approximately 42 μ sec is generated by the ICN11 monostable multivibrator from the fall of the ~PH pulse, and a pulse with a width of approximately 21 μ sec is generated by ICN10 (pin 13) from its fall. A 0.8 μ sec pulse is created by ICN10 pin 5 from the fall of the ICN10 pin 13 output, and the phases of the fall of this pulse and the ~PH pulse fall are compared by ICM8. The widths of the pulses generated by these two monostable multivibrators (ICN11 , N10) are controlled by the ICM8 output so that the ICM13 pin 5 pulse will approach the PH pulse which is to arrive next. Only the PH pulses appearing within the ICM13 pin 5 pulse range are output as the SELECT H signal. The ICM13 pin 5 pulse width is about 1.6 μ sec and any pulses with a width exceeding ±0.8 μ sec from periodic signals are not output as the SELECT H signal.

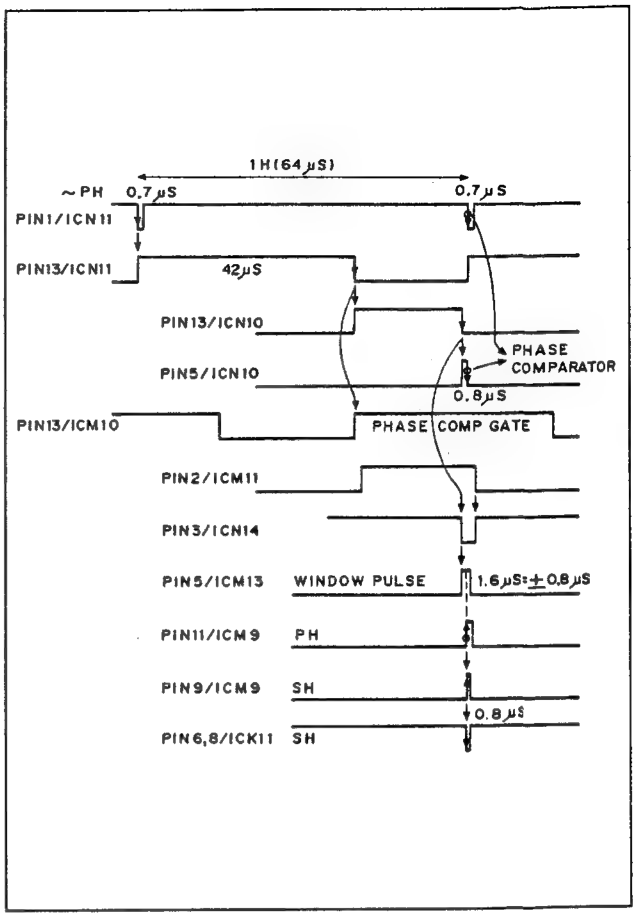


Fig. 4-4-19. SELECT H Timing Chart (CK-27)

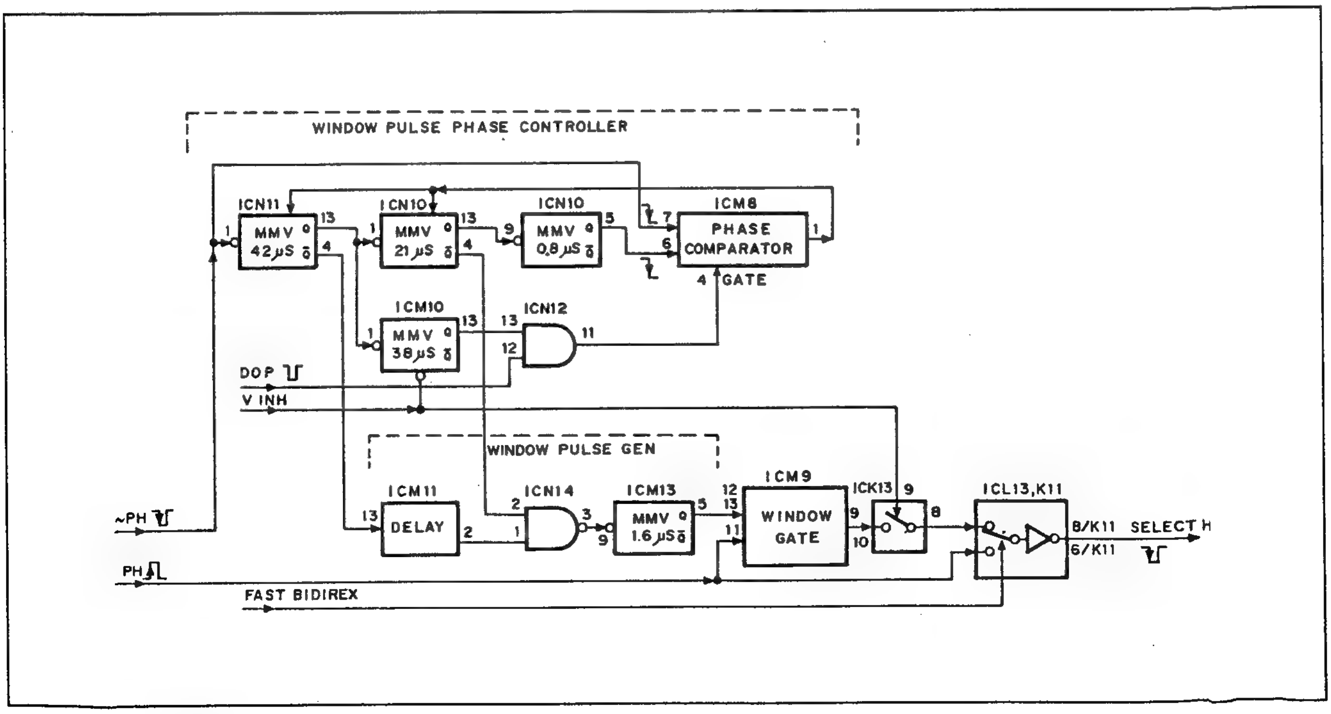


Fig. 4-4-18. SELECT H Generator (CK-27)

(3) AFC (CK-27 board)

The AFC circuit is driven by a pulse which has a width of approximately 450 nsec and which is created from the SELECT H signal. As shown in Fig. 4-4-20, it is composed of a closed loop (ICN14 →M19→M18→P18→P13→P7→P12→N14) and an open loop based on the TAPE SPEED signal supplied to ICM18.
In order to accelerate the AFC pull-in during the shuttle mode or when skew has arisen, this AFC resets the counter under any deviation from the window of approximately ±220 nsec. The range for the change in the VCO frequency is from 8 to 26 MHz. The VCO is controlled so that it oscillates at a frequency which is equivalent to 1135 times that of the SELECT H signal. With a PAL system, the phase of the SELECT H signal is modulated by the PH generator circuit and so the VCO center frequency is 1135FH + 100 Hz.
Fig. 4-4-21 is a timing chart of the various sections. The pulse, which has a width of approximately 400 nsec and which is created by monostable multivibrator ICN11 from the SELECT H signal, is supplied to ICN14 and ICM19 which configure a phase comparator. In order that the TP11 (ICP12 pin 14) fall timing will be locked at the intermediate point of the 450 nsec pulse, VCO ICP18 is controlled by the ICM19 error voltage, and the VCO output drives counter ICP7. When the SELECT H signal (ICN11 pin 5) is supplied within the range of the window created by ICP5 (pins 1, 2 and 3), the counter is not reset ; when it deviates from the window, ICM9 pin 5 is set high, the reset pulse is generated at ICN14 pin 11 and counter ICP7 is reset. ICP7 is reset not to zero but to "11." As a result, the next window after resetting appears at the proper position.

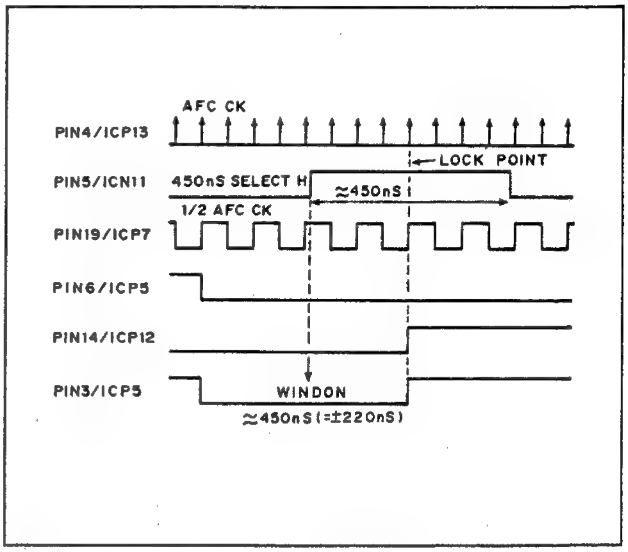


Fig. 4-4-21. AFC Window (CK-27)

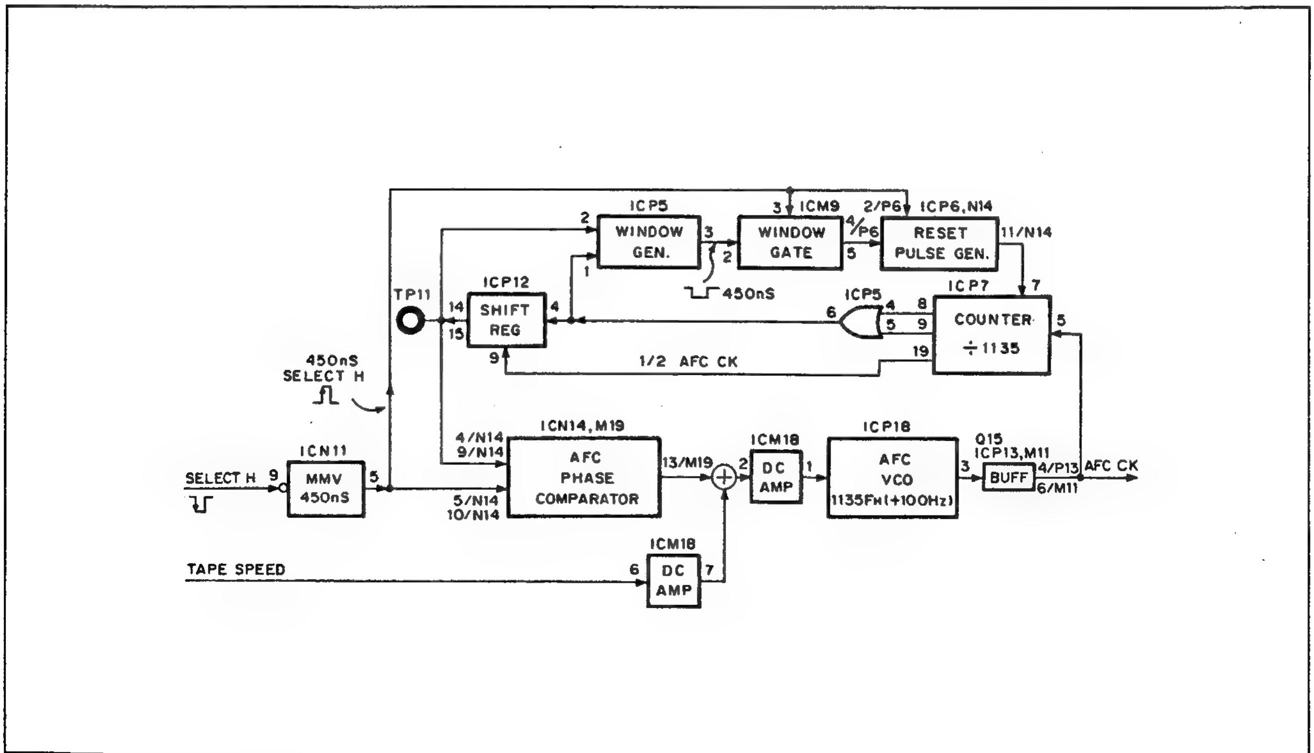


Fig. 4-4-20. AFC (CK-27)

(4) Burst signal detector (CK-27 board)

This circuit takes out the burst signal from the PB CHROMA signal. The bandpass filter (FL1 and LV1) with its center frequency of 4.43 MHz takes out the chroma signal from the PB CHROMA signal which contains the Y components and which has been supplied from the VO-16 board. Next, the burst signal is separated from the chroma signal by ICK21. The TTL level burst signal is then output from ICK21.

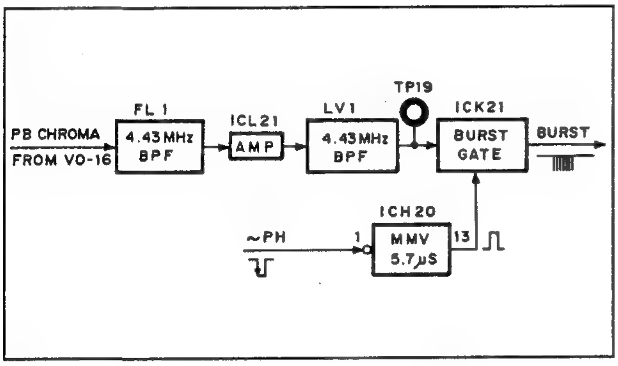


Fig. 4-4-22. Burst Signal Detector (CK-27)

(5) APC start pulse generator (CK-27 board)

This circuit serves to take out one wave of the burst signal from the burst signal which has been converted to the TLL level in the burst detector and to trigger monostable multivibrator ICG18 (pin 10). Which wave is taken out depends on the pulse width of the reset signal (TP4) of the ICG21 shift register. When the TP4 pulse width has been adjusted to 2.7 μ sec, the sixth wave is taken out. The ICG18 (pin 5), K13 and E21 loop is configured so that the width of the monostable multivibrator output pulse is aligned accurately with one burst wave. The pulse generated here is the start pulse for starting and stopping the oscillation of the APC VCO.

ICG18 (pin 13) and G19 detect the continuity of the one burst wave and when it is discontinuous, the start pulse is not allowed to be output. The start pulse is created from the one burst wave only in the PAL color mode. The burst signal cannot be detected in the SECAM, black-and-white and fast bidirex modes and so, in this case, the pulse created from the ~PH signal by ICH21 is supplied to ICG18 (pin 9) to generate the start pulse.

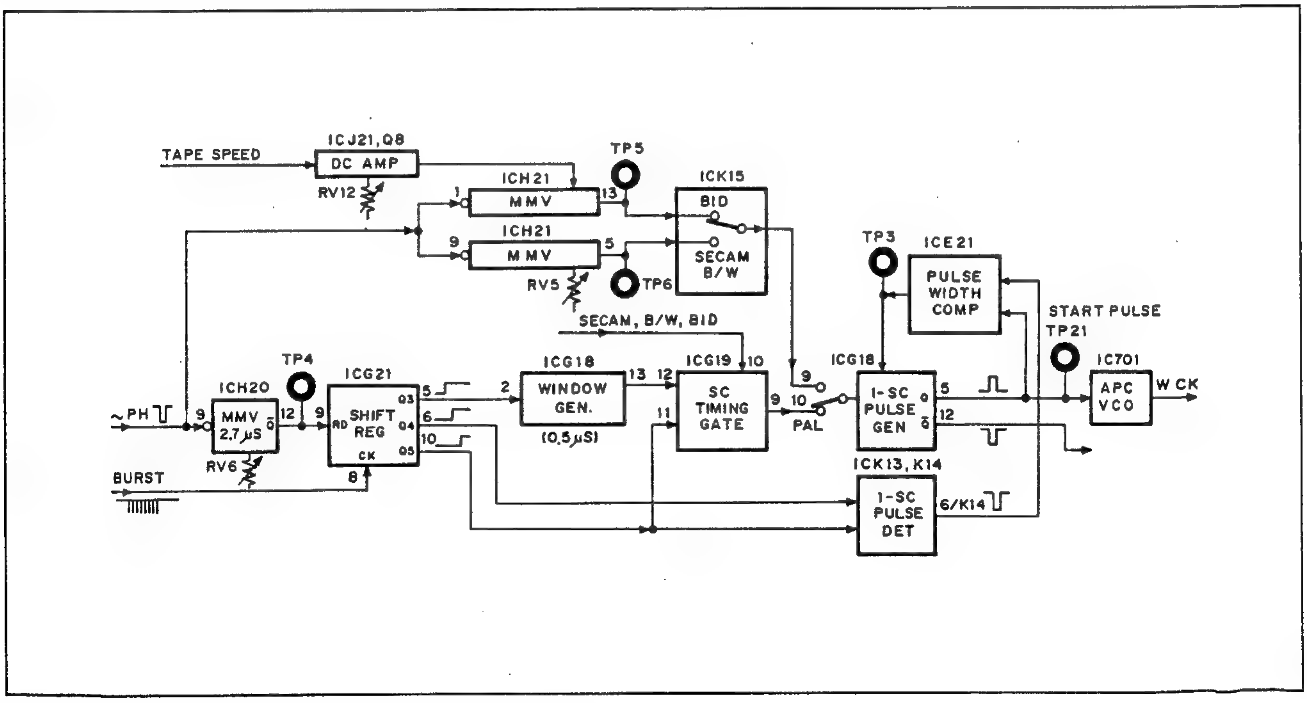


Fig. 4-4-23. APC Start Pulse Generator (CK-27)

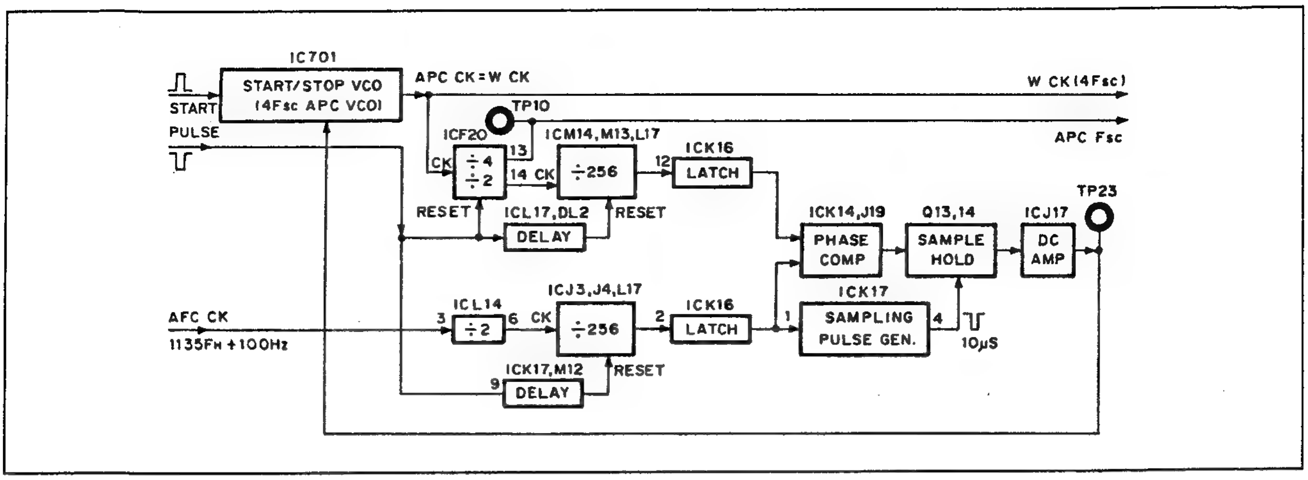


Fig. 4-4-24. APC and AFC Locking (CK-27)

(6) AFC and APC locking (CK-27 board)

The APC start/stop VCO oscillates at a frequency of 4Fsc and its phase is locked to the phase of the burst signal by the start pulse.
By means of comparison with the AFC VCO frequency, the APC VCO frequency is controlled so that it is matched with the AFC VCO frequency. The range across which the APC VCO frequency can be varied extends from 8 MHz to 26 MHz. The APC CK pulse output from the APC VCO is the W CK (write clock) pulse.
The frequency of the 4Fsc APC CK signal is first halved by ICF20 and then the resulting signal enters the 256 counter which is composed of ICM14, M13 and L17. When this counter executes a 256 count, the counting will stop until the counter is next reset. The reset pulse is generated from the APC start pulse and so this means that the counter output is an H rate pulse with a duty ratio of approximately 45%.
An H rate pulse with a duty of 45% is also simultaneously generated from the AFC CK pulse. By comparing the phases of the two pulses in ICK14 and J19 and by controlling the APC VCO with the resulting error voltage, the APC VCO frequency is matched with the AFC VCO frequency.

(7) W O/E detector and velocity error detector (CK-27 board)

The W Fsc signal is locked to the burst signal line by line, and the PAL system line O/E is detected by latching the W Fsc signal by the burst signal of the next line.
The velocity error voltage is created by using a charge pump to T/V convert the difference in the phases of the W Fsc signal and of the burst signal in the following line. The phase difference is detected by ICE19 (pins 11 and 12) and F18 (pins 6 and 3) and converted into a voltage by ICD19. The velocity error voltage is reset line by line using Q4. The level of this voltage is then shifted and inserted into the H sync section of the video signal prior to A/D conversion.

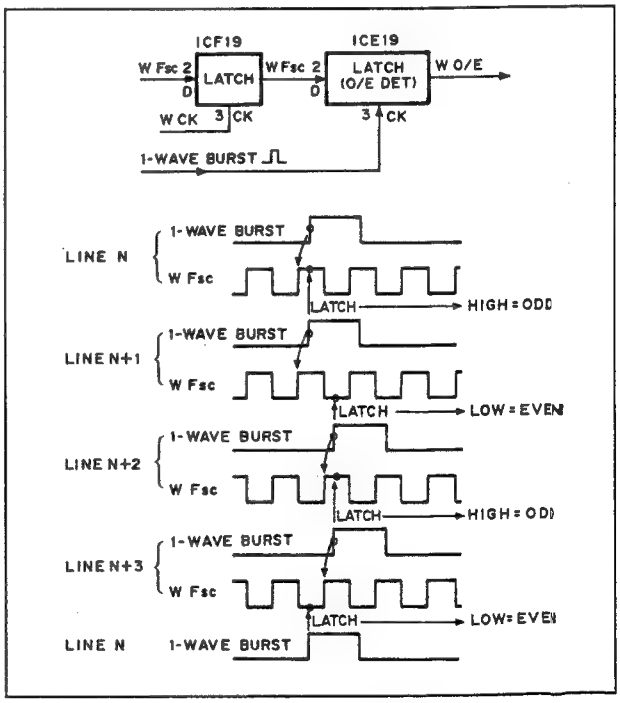


Fig. 4-4-25. W O/E Detector (CK-27)

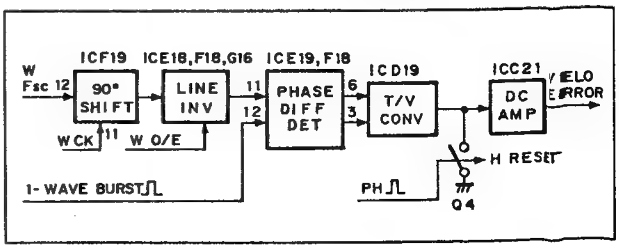


Fig. 4-4-26. Velocity Error Detector (CK-27)

(8) W ZERO generator (CK-27)

It is vital that the W ZERO (write zero) signal, which is the memory write start signal, be output at a high degree of stability and reproducibility with the same phase no matter what happens to the SC-H phase.
The PH pulse phase is compared by IC11 with the phase of the H pulse output from the AFC, and the delay in the PH pulse is controlled by the resulting error voltage. The time constant of the phase comparator is configured with a large-capacity capacitor (C109) and so the ICN9 and IC11 circuit functions as a kind of low-pass filter which does not track high phase fluctuations.
After its noise components have been filtered out by the low-pass filter, the H pulse now triggers the variable-width monostable multivibrator (ICP9) in the W ZERO loop. The output of this multivibrator is first latched by SC** (W Fsc which has been inverted by W N/I) and then supplied to the phase comparator composed of ICM5 and N8. The phase error (TP27) is fed back to the variable-width monostable multivibrator (ICP9) to control the pulse width of ICP9. R172 is added to pin 10 so that the pulse width supplied to pin 7 of charge pump ICN8 is made one-half of the width of the pulse supplied to pin 5.
The ICN6 comparator determines the tracking range of the W ZERO loop. This range is approximately ±270° . When the error voltage resulting from phase comparison exceeds the ICN6 threshold voltage, ICN8 is reset and returned to the center voltage.

Comparator ICN5 and M7 detect that the W ZERO loop is in the center of the locking range and they cause the PB CF LED to light up.
The output of variable - width monostable multivibrator ICP9 pin 4 is first latched by ICM6 pin 6, and then it resets ICP15 which is counting the W CK pulses. The ICP15 output is the W ZERO signal. The W ZERO loop circuit enables a timing signal which maintains the phase relationship with W Fsc to be provided no matter what the SC-H phase of the signal supplied may be, and it enables ICP15 to count the W CK pulses correctly. This counter is designed to turn at the 1135 count so that the W ZERO pulses are not missing.
In the bidirex, SECAM or black-and-white mode, the H pulse created from the PH pulses by the APC start pulse circuit serves as the reset pulse for ICP15.

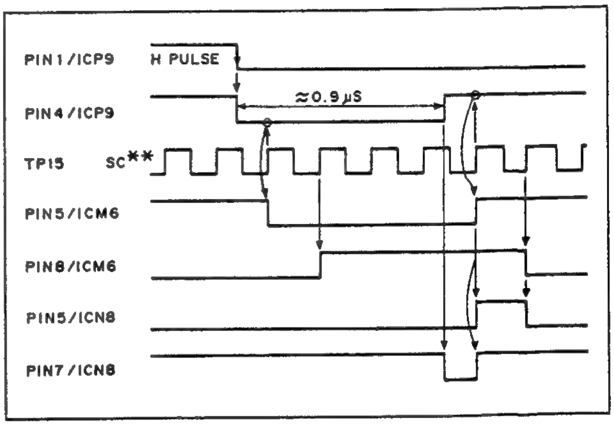


Fig. 4-4-28. W ZERO Loop (CK-27)

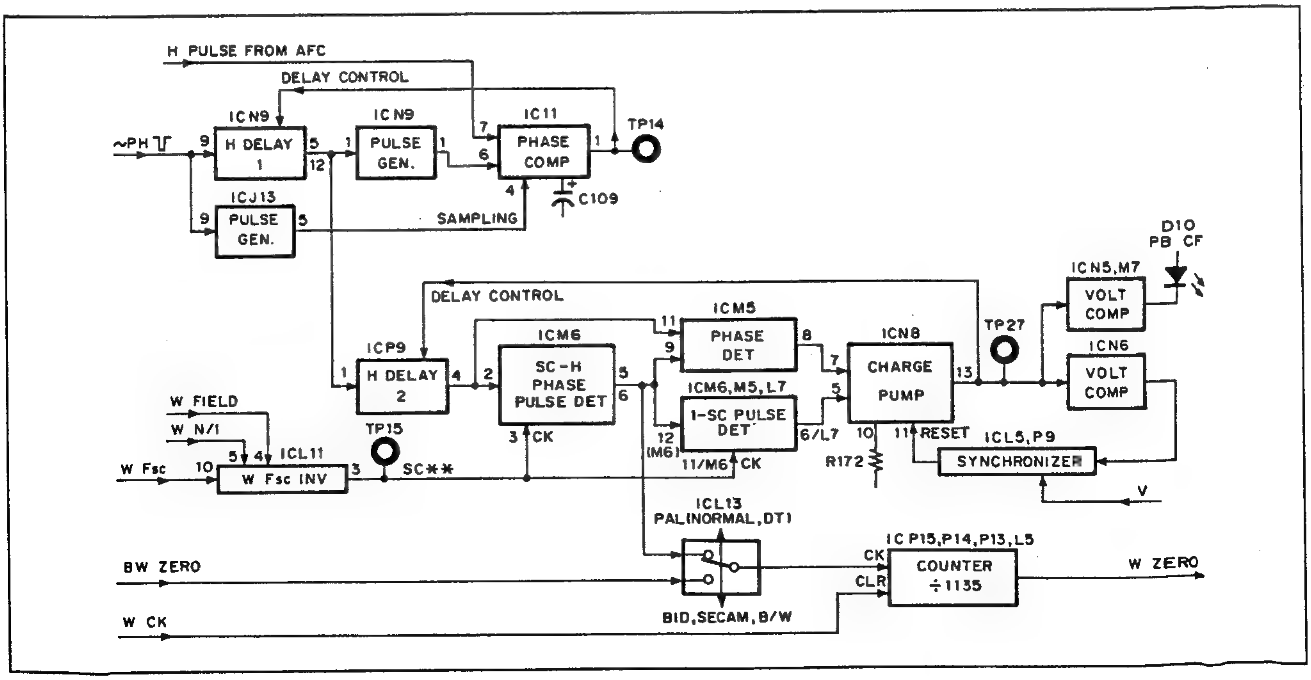


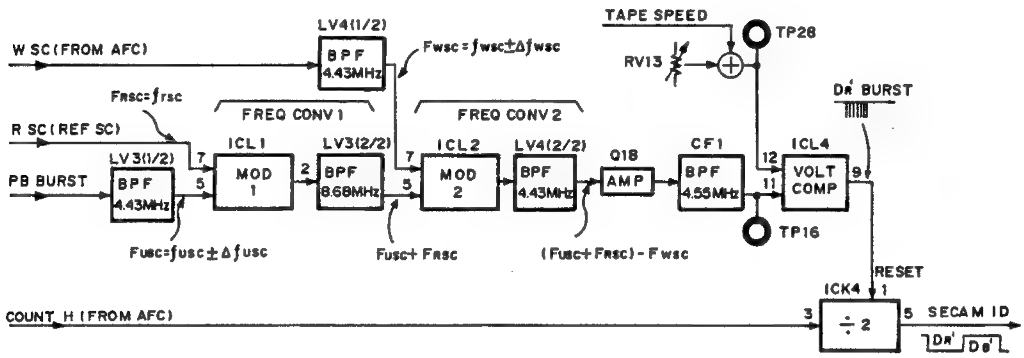
Fig. 4-4-27. W ZERO Generator (CK-27)

(9) SECAM DR' /DB' line ID detector (CK-27 board)

DR' line/DB' line detection makes use of the fact that the frequency of the burst (unmodulated subcarrier) signal which is added to the head of each line of the SECAM signal is switched every horizontal line. The DR' line burst signal frequency is 4.406 MHz and that of the DB' line is 4.250 MHz.

On a CK-27 circuit board which has the number 1-621-749-11 or -12, the effects of the tape speed are first removed from the burst signal frequency using a double-heterodyne system and then the difference in the frequency is converted into a voltage difference by the filter to detect the DR' line.

On a CK-27 circuit board which has the number 1-621-749-13 or higher, the difference in the DR' and DB' line burst signal frequencies is converted into a voltage difference by the FM demodulator and the DR' and DB' lines are detected.



Freq of PB BURST: $F_{usc} = f_{usc} \pm \Delta f_{usc}$ (f_{usc} ; CENTER FREQUENCY, Δf_{usc} ; FREQUENCY DEVIATION)

Freq of REF SC: $F_{RSC} = f_{RSC}$

Freq of W SC: $F_{wsc} = f_{wsc} \pm \Delta f_{wsc}$ (f_{wsc} ; CENTER FREQUENCY, Δf_{wsc} ; FREQUENCY DEVIATION)

Freq of F.CONV 1 OUT: $F_{usc} + F_{RSC} = (f_{usc} + f_{RSC}) \pm \Delta f_{usc}$

Freq of F.CONV 2 OUT: $(F_{usc} + F_{RSC}) - F_{wsc}$

$$= (f_{usc} + f_{RSC}) \pm \Delta f_{usc} - (f_{wsc} \pm \Delta f_{wsc})$$
$$= f_{usc} + (f_{RSC} - f_{wsc}) + (\pm \Delta f_{usc}) - (\pm \Delta f_{wsc})$$
$$= f_{usc}$$

Fig. 4-4-29. SECAM DR' /DB' Line ID Detector (CK-27-11/12)

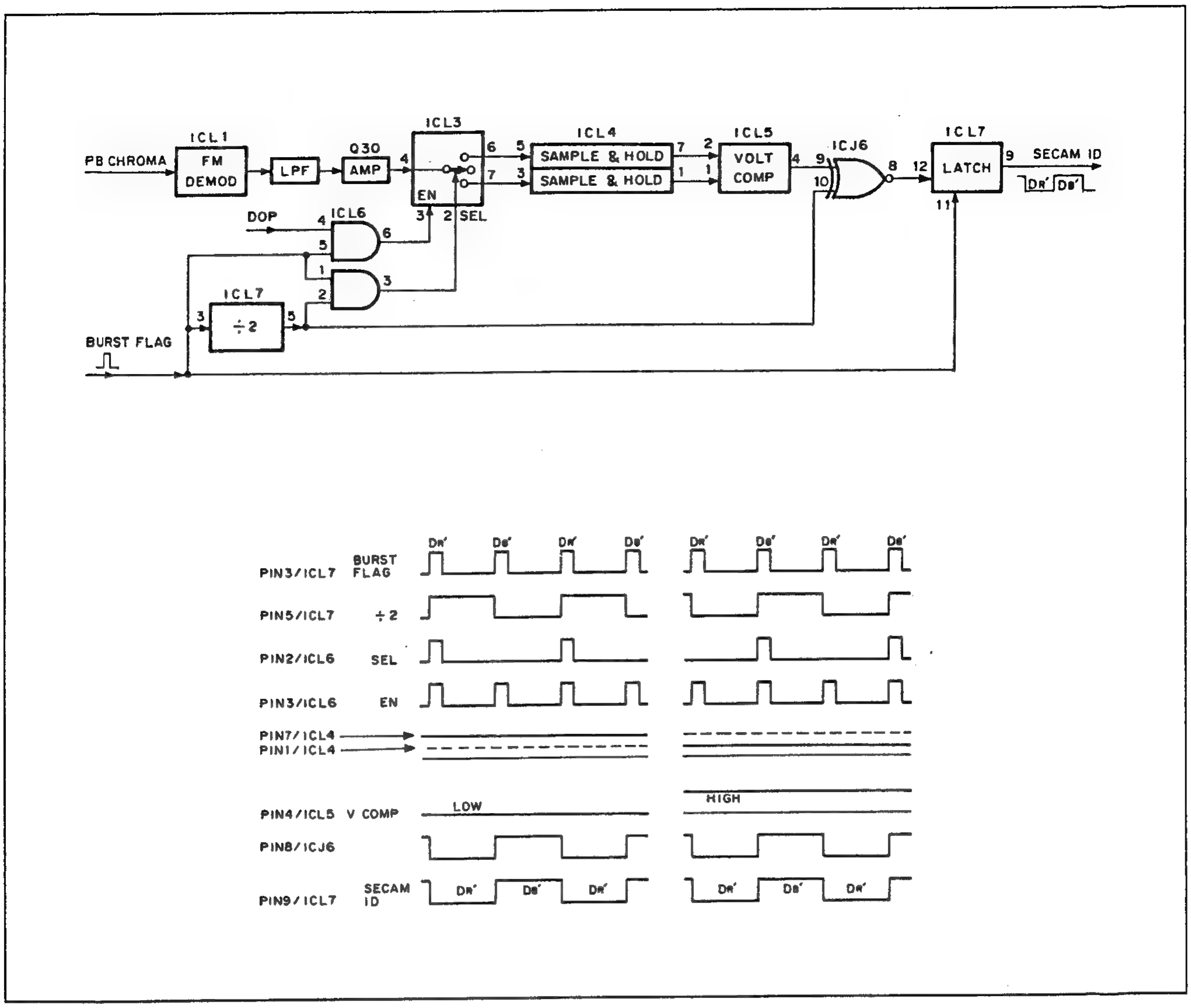


Fig. 4-4-30. SECAM DR' /DB' Line ID Detector (CK-27-13)

(10) W O/E and W N/I generator (CK-27 board)

In the case of the PAL signals, the lines are identified with two types of signals, O/E (odd/even) and N/I (normal/invert), and so a cycle for line identification involves 4 lines. Since a field is composed of 312.5 lines and there is an offset of 3.5H between the tracks on the tape, N/I and O/E are discontinuous when the head jumps to a discontinuous track such as during DT playback. N/I and O/E are therefore corrected by the DT head jump information from the DT control circuit (RD board).

The DT head jump information is supplied to the CK board as the 3-bit parallel data (J STATUS 1, 2 and 3), and it is decoded into the N/I and O/E correction signals at ICK5, H6, K8 (pin 8) and J9 (pin 8).

DT head jump	J STATUS			O/E	N/I
	3	2	1		
3-pitch	0	0	0	INV	
2-pitch	0	0	1		INV
1-pitch	0	1	0	INV	INV
0-pitch	0	1	1		
−1-pitch	1	0	0	INV	
−2-pitch	1	0	1		INV
−3-pitch	1	1	0	INV	INV
not used	1	1	1		

0-pitch jump = normal playback

The output, produced by halving the frequency of the counter (ICK10) signal which uses the COUNT H pulse created by dividing down the frequency of the AFC clock as the clock pulse, is the O/E signal. The ICK10, L8, L9, L10 and G5 loop configures the O/E correction circuit. This circuit has inertia and it functions to prevent O/E from being inverted until the mismatching with the O/E signals provided from the playback burst signal is detected 16 times (16 lines). This is because if O/E is inverted as soon as it has been detected in error, the color will appear on the screen unevenly which makes it hard to see the picture.
Both of the O/E signal (or SECAM ID signal in the case of SECAM signals) detected from the burst signal and the O/E signal produced by halving the frequency of the COUNT H pulse are supplied to the ICL8 exclusive OR circuit. If the O/E signal has been created properly, two O/E signals (ICL8 pins 9 and 10) will have mutually opposing polarities, the ICL8 output (pin 8) will be set high, the ICL9 output (pin 6) will be set low, and the ICL10 error counter will be prohibited from counting. If the O/E signal has not been created properly, the two O/E signals will have the same polarity, the ICL8 output will be set low, and the ICL10 error counter will count the COUNT H pulse. When the counter counts 16 COUNT H pulses, a pulse is output to the CO (carry output) pin. The error counter output is supplied to the ICK10 enable pin and the ICK10 count is stopped once. As a result, the polarity of the W O/E signal is inverted.
The OR signal of the O/E INV signal which has been created from the jump status information and the error counter output signal is supplied to the ICK10 enable pin. When the O/E INV signal is generated from the jump status information, the ICK10 count is stopped regardless of the error counter and the polarity of the W O/E signal is inverted.
The ICL10 error counter is reset with each vertical sync pulse. In the bidirex or SECAM mode, the maximum value of the error counter is changed from 16 to 1 and the O/E signal polarity is inverted with each O/E error.
The W N/I signal is created by halving the frequency of the O/E signal at ICL9 (pins 11 and 9). ICL9 is reset by the output of ICK8 pin 6. The reset pulse is output at the REF 8F and DTV timing and this is the CF reset pulse. As detailed below, the CF reset pulse is generated when the VTR mode is changed.

- BIDIREX

DT → EE ⇄ PLAY STATUS
(Servo lock status at ×1 speed)

- In the PLAY STATUS condition,
  CONFI ⇄ $\overline{\text{CONFI}}$
  EDIT PRESET ⇄ EDIT PRESET
- When the mode is changed from the no-signal status to the play status
- When the power has been switched on
- When the REF4 signal is disturbed
- When the black-and-white mode has been changed to the color mode

The ICL9 pin 9 output is inverted by ICL8 in accordance with the jump status information of the DT head to form the W N/I signal.

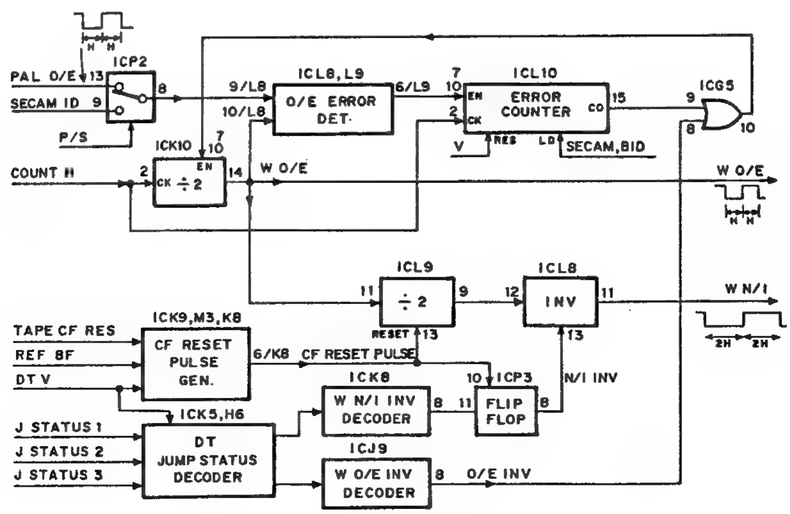


Fig. 4-4-31. W O/E and W N/I Generator (CK-27)

4-4-4. TAPE SC-H Detector (CK-27 Board)

"SC-H" denotes the phase relationship between the sync signal and burst signal. In the case of PAL signals, 8 fields are treated as one cycle for which the sync and burst signals are provided with a phase relationship. The BVH-3000/3100 use LED indication on the front panel to display the SC-H phase and this facilitates SC-H phase control during editing operations. The SC-H phase of the reference video signal is detected on the RD board. The SC-H phase of the playback video signal (or input video signal in the EE mode) is detected by the CK board, A/D converted on the RD board, sent to the front panel by the data bus and displayed by the LEDs.
As with the PH (PAL H) generator, H pulses with a period from which PAL offset has been eliminated are generated by generating sawtooth waves from the PB SYNC signal and slicing these waves with V rate sawtooth waves.
Furthermore, in ICK4, pulses with a width equivalent to the SC-H phase difference are generated by latching the SC* pulse (W Fsc signal whose phase is aligned line by line). This pulse width is converted into a voltage by the ICN17 charge pump and the resulting voltage is sent to the RD board.
ICL16 and L15 serve to narrow the width of the SC* pulse and widen the detection range of the SC-H phase.
In order to reduce the susceptibility to the effects of dropouts and velocity errors, the window comparator composed of ICP16, 301, 302, Q14 and 23 (ICP16, M16, M15, Q24 and 23) removes the SC-H voltage which is not included in the window. The ICN16 low-pass filter eliminates fluctuations from the SC-H voltage.

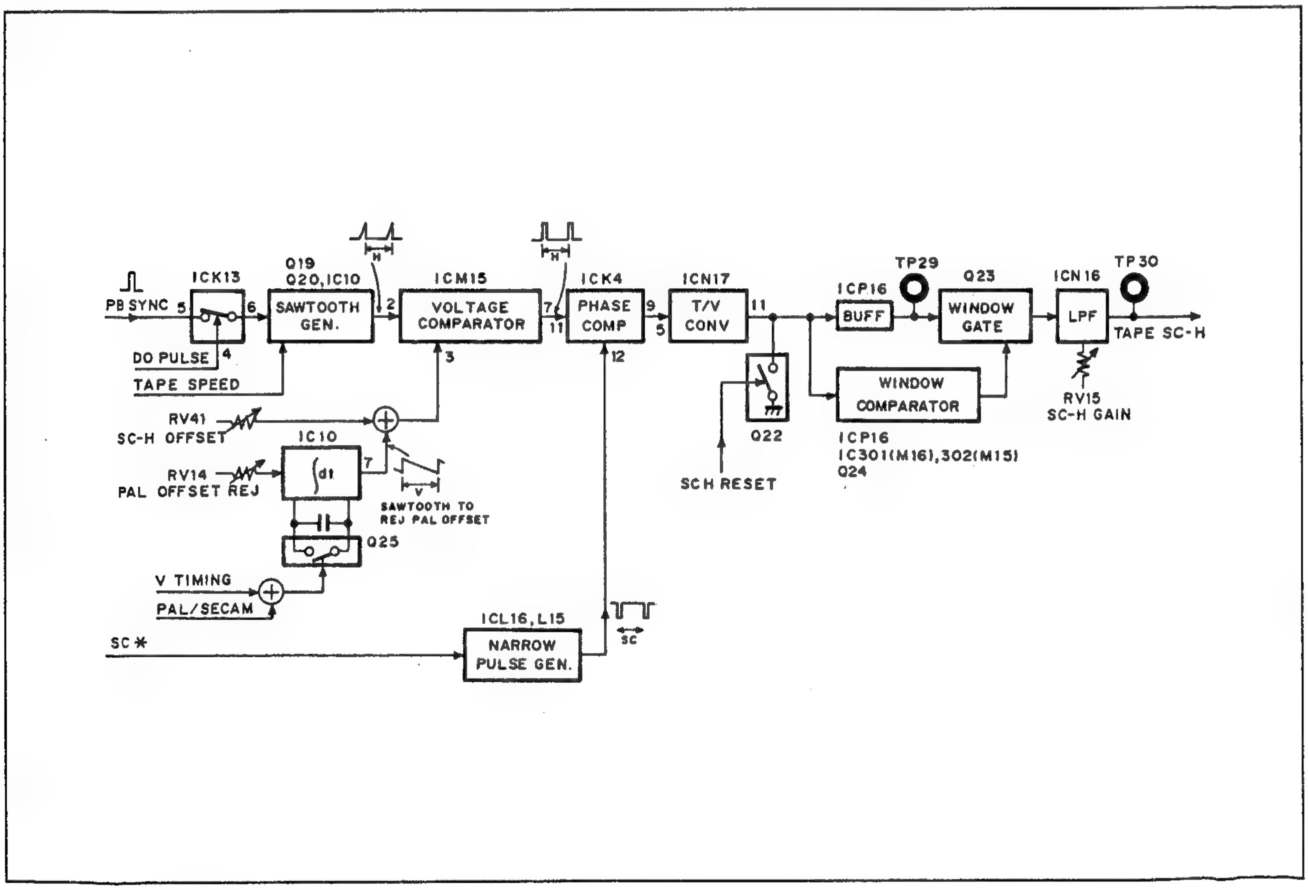


Fig. 4-4-32. TAPE SC-H Detector (CK-27)

4-4-5. CK Board Mode Decoder (CK-27 Board)

Since the switches on the circuit boards have been removed and servicing is performed based on menus, all the mode signals in the BVH-3000/3100 are sent from the SY/SV board by the data bus. The mode decoder circuit serves to decode the signals arriving in the data bus into the mode signals. The CK board functions only to receive the data and because of the low number, the data are decoded by latches.
Shown below are the modes which are decoded by ICN1 and N2.

Pin/IC	Signal	Function
19/N2	PB CF R/L	PB CF adjustment (H : remote ; L : local)
2/N2	ZERO ADV	Zero advance (TBC) (H : other ; L : zero advance)
16/N2	BID	Indicates bidirex mode (H : bidirex ; L : other)
5/N2	PB CF	Indicates PB CF preset (H : other ; L : preset)
15/N2	F.BID	More than ±8 times normal speed (H : fast bidirex ; L : other)
6/N2	B&W	Monochrome (H : B&W ; L : other)
12/N2	DOC OFF	DOC ON/OFF (H : DOC OFF ; L : DOC ON)
9/N2	CF RESET	TAPE CF reset
19/N1	F REW	Indicates fast bidirex in reverse direction (H : other ; L : fast rewind)
2/N1	EE	(H : other ; L : EE)
16/N1	NOT USED	
5/N1	P/S	(H : SECAM ; L : PAL)
15/N1	PLAY STATUS	(H : other ; L : play status)
6/N1	HQ	Indicates HQ PR board (PR-98) (H : HQ ; L : standard)
12/N1	DELAY	1/3V delay with CONF (H : delay ; L : other)
9/N1	FREEZE	Indicates freeze (H : freeze ; L : other)

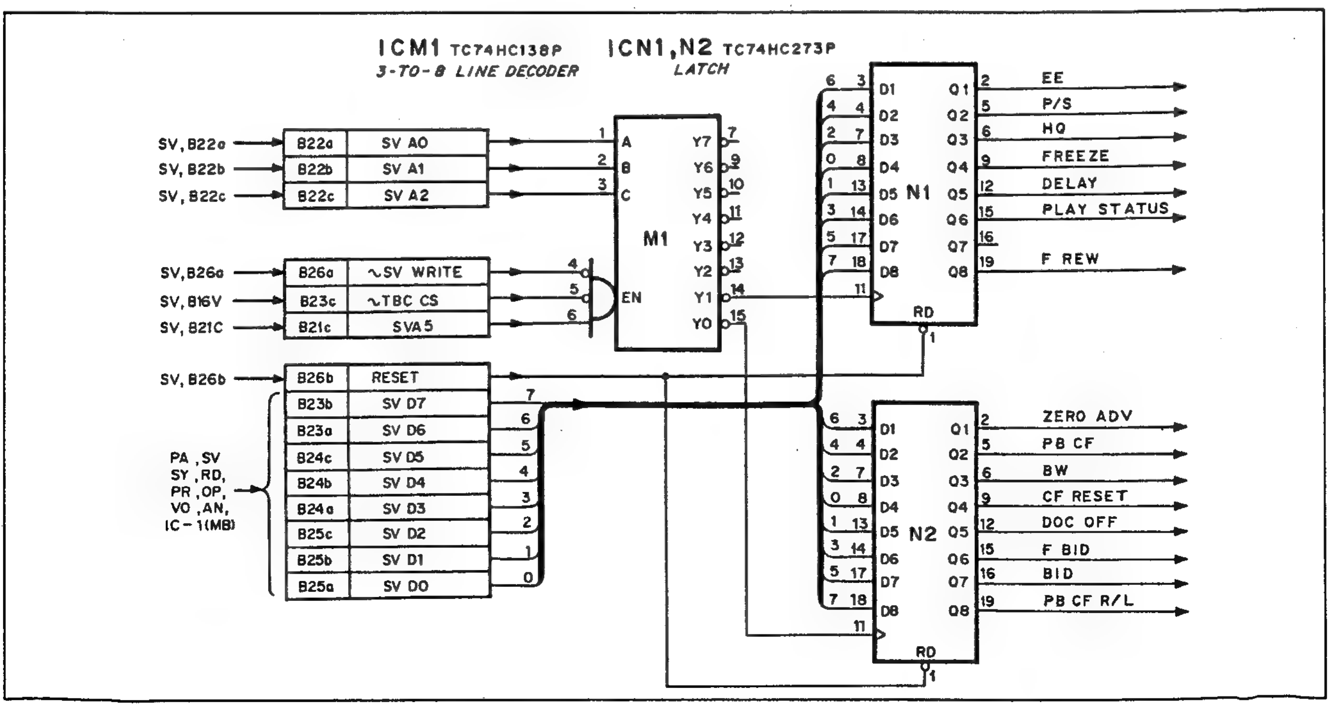


Fig. 4-4-33. Mode Decoder (CK-27)

4-4-6. TBC Reference Signal Generator (RD-7 Board)

The RD-7 board is composed of the TBC reference signal generator, servo reference signal generator and DT control circuit.
The TBC reference signal generator is composed of the four following circuits.

1. **TBC reference video signal selector**
   This circuit selects either the INPUT VIDEO signal or INPUT REF VIDEO signal as the TBC reference signal.
2. **RD CK (read clock) generator**
   This circuit generates the read clock signal which is synchronized with the burst signal in the reference signal. It also provides differential phase compensation and velocity error compensation for the PAL signal.
3. **Sync generator**
   This circuit generates the various signals which are synchronized with the sync signal in the reference signal.
4. **R ZERO (read zero) generator**
   This circuit generates the main memory read timing signals from the H sync signal and from the RD CK signal which has been synchronized with the burst signal.

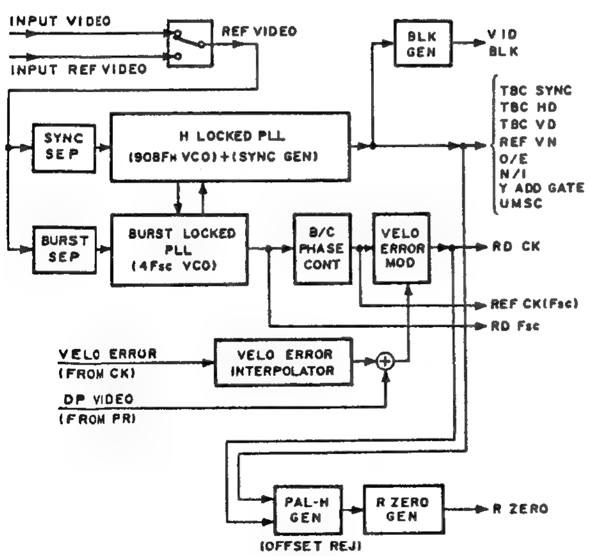


Fig. 4-4-34. Outline of TBC Reference Signal Generator (RD-7)

(1) TBC reference video signal selector (RD-7 board)

This selector circuit functions to select either the INPUT VIDEO signal, which has been supplied from the external source, or the INPUT REF VIDEO signal as the TBC reference signal.
When [EXT REF] is selected on the [S86. TBC REF SELECT] menu, the INPUT REF VIDEO signal is selected ; when [SERVO] is selected, one of the signals designated by the [S40. SERVO REF SELECT] menu shown below is selected.

		S86. TBC REF SELECT	
		SERVO	EXT REF
S40. SERVO REF SELECT	EXT REF	INPUT REF VIDEO	INPUT REF VIDEO
	AUTO	Recording : INPUT VIDEO Editing : INPUT VIDEO Others : INPUT REF VIDEO	
	INPUT	INPUT VIDEO	

The video signal supplied to this circuit has a level of 0.5 Vp-p. After the INPUT VIDEO signal or INPUT REF VIDEO signal has been selected by ICF1, it is amplified by ICF1 and F3 to a level of approximately 4.5 Vp-p. The amplified signal is then sent to the reference sync separator and subcarrier generator.

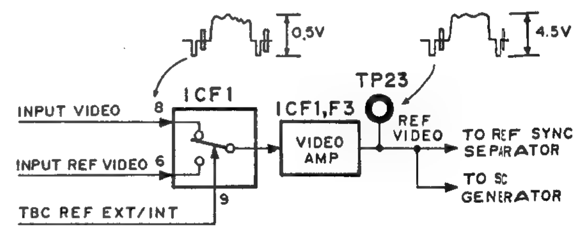


Fig. 4-4-35. TBC Reference Video Signal Selector (RD-7)

(2) **Reference sync separator (RD-7 board)**

This circuit separates the sync signal from the reference video signal which was selected by the TBC reference video signal selector.

The Y component is taken out from the reference video signal by the low-pass filter composed of C118, L12 and C119, and its pedestal level is clamped to 0V by Q9, ICF8 (pin 14), IC1 (pin 1) and IC1 (pin 7). The sync tip is sampled and held by ICF8 (pin 4) and ICF9 (pin 1), and the sync signal level is detected. The level of the detected sync signal is divided by (R243+R391) and R242 to produce a voltage which is one-half of the sync level. The sync signal is separated by a process of comparing in ICF10 the Y signal whose pedestal has been clamped to 0V and the voltage which is one-half of the sync tip level.

ICF8 (pin 10) switches the voltage division ratio of the sync level using R243, R391 and R242. Apart from the leading edge of the sync signal, the voltage which is compared by ICF10 approaches the tip of the sync signal and makes it harder for noise to cause disturbances.

Q8 and ICF6 form the rough sync separator. The pedestal clamp pulse and sync tip sampling pulse are then created from the sync signal, which is separated in this circuit, by ICF7.

The separated reference sync signal is sent to the gen-lock driver of the ICF12 sync generator.

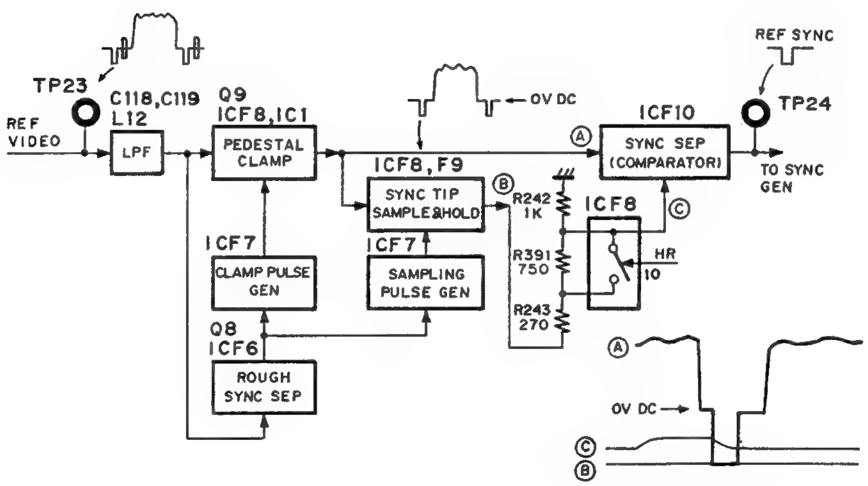


Fig. 4-4-36. Reference Sync Separator (RD-7)

(3) Sync and subcarrier locking (RD-7 board)

After it has been separated, the REF SYNC signal is supplied to the sync generator which is composed of the gen-lock driver IC (ICF12 : CX7903), sync generator IC (ICG17 : CX773B), 908FH VCO (X3) and sync phase controller (ICG15). This sync generator serves to generate various sync pulses and the HCK (908FH) pulse which is synchronized to the REF SYNC signal.
The subcarrier generator is composed of the 4.43 MHz bandpass filter, phase comparator (ICD2, ICD5), 4Fsc VCO (X4) and counter (ICD10). It serves to generate the RCK (4Fsc) pulse which is synchronized with the burst signal in the REF VIDEO signal.
For operation, the connections between the sync generator and subcarrier generator are changed for each of the 5 modes listed below.

(a) PAL • EXT • COLOR mode
(b) PAL • EXT • B&W mode
(c) PAL • INT mode
(d) SECAM • EXT mode
(e) SECAM • INT mode

(a) PAL • EXT • COLOR mode

In this mode the sync generator and subcarrier generator operate independently.
In the sync generator loop, the 908FH frequency signal output from the VCO (X3) is divided down in ICG17 by 908 to form the FH pulse. The phase of this FH pulse is adjusted in the sync delay circuit by the SYNC CONT voltage, after which the signal is supplied to ICF12 and its phase is compared with that of the reference sync signal. The resulting phase difference is converted into a voltage which is supplied to VCO (X3), and a loop is configured. It is in this loop that the various sync signals and 908FH signal which is synchronized with the reference sync signal are generated.
The sync delay circuit is composed of a monostable multivibrator (ICG15) and integrator (ICG2D and ICE13). The FH pulse (pin 23/ICG17) is output to

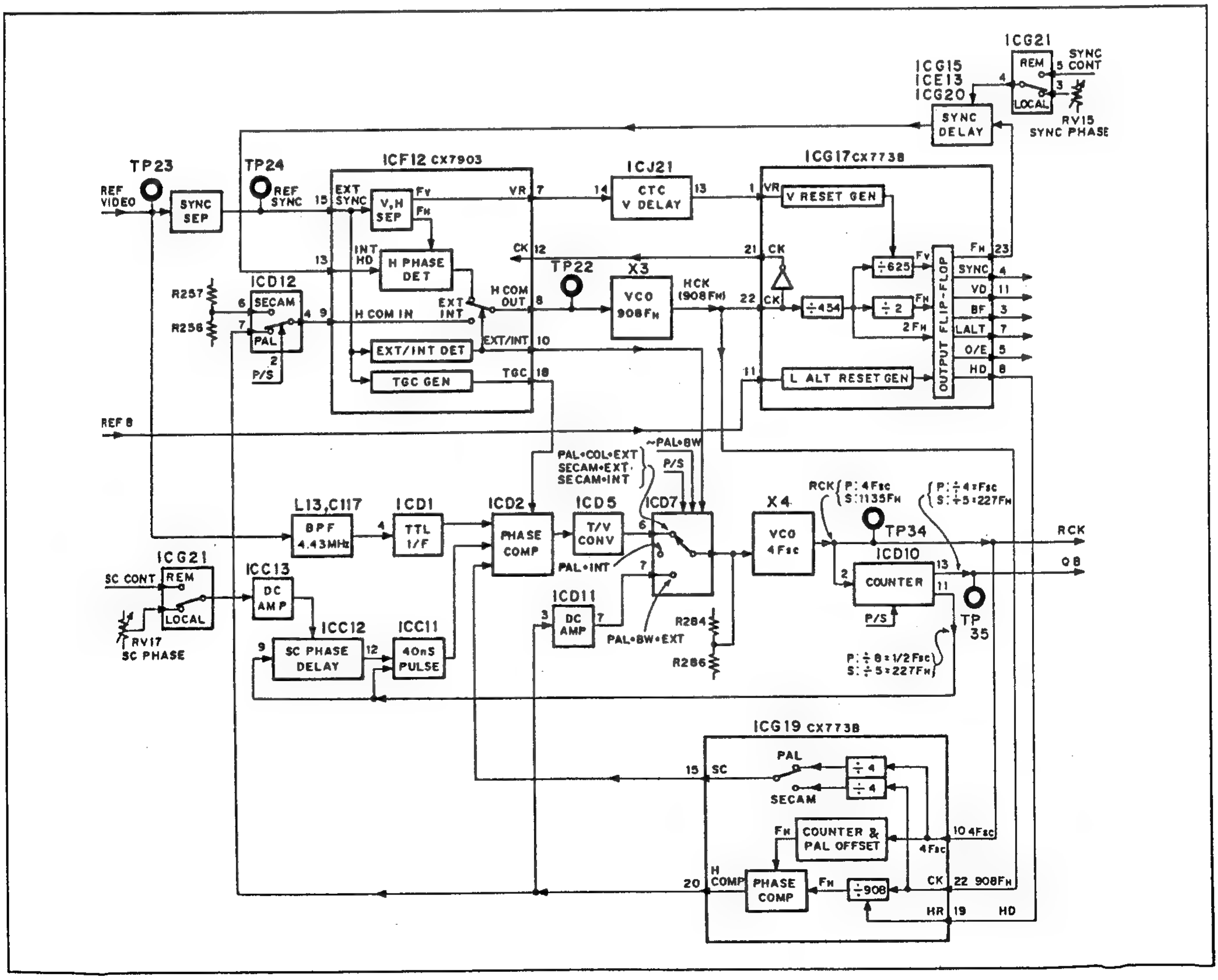


Fig. 4-4-37. Sync/Subcarrier Generators (RD-7)

a position which is ahead of the TBC SYNC signal (TP30 : A23C) by 174 clock pulses (equivalent to 12.3 μ sec). ICG15 is triggered by the FH pulse and the loop operates so that the fall edge of the ICG15 output signal is aligned with the leading edge phase of the reference sync signal. The ICG15 pulse width

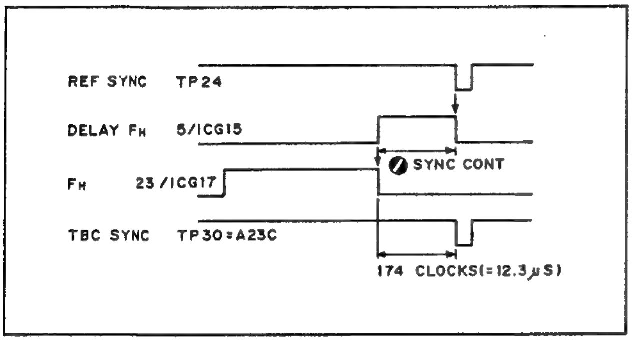


Fig. 4-4-38. Sync Delay Control Circuit (RD-7)

is controlled by the SYNC CONT voltage and, as a result, it is possible to yield an adjustment of the TBC SYNC signal phase across a −1 to +3 μ sec range with respect to the reference sync signal.

In the subcarrier generator loop, the 4Fsc frequency signal which is output by the VCO (x4) is divided down by 8 in ICD10 to form the 1/2 Fsc signal which is then supplied to the ICC12 monostable multivibrator. The delay of this signal is first adjusted by the SC CONT voltage, after which a pulse with a width of 40 nsec is created by ICC11. While the burst gate pulse (TGC : pin 18/ICF12) is high, the phase of this 40 nsec pulse is compared by ICD2 with the phase of the burst signal in the reference signal, the resulting phase difference is converted into a voltage by ICD5 and supplied to VCO (X4), and a loop is configured. It is in this loop that the 4Fsc pulse synchronized to the burst signal in the reference signal is generated.

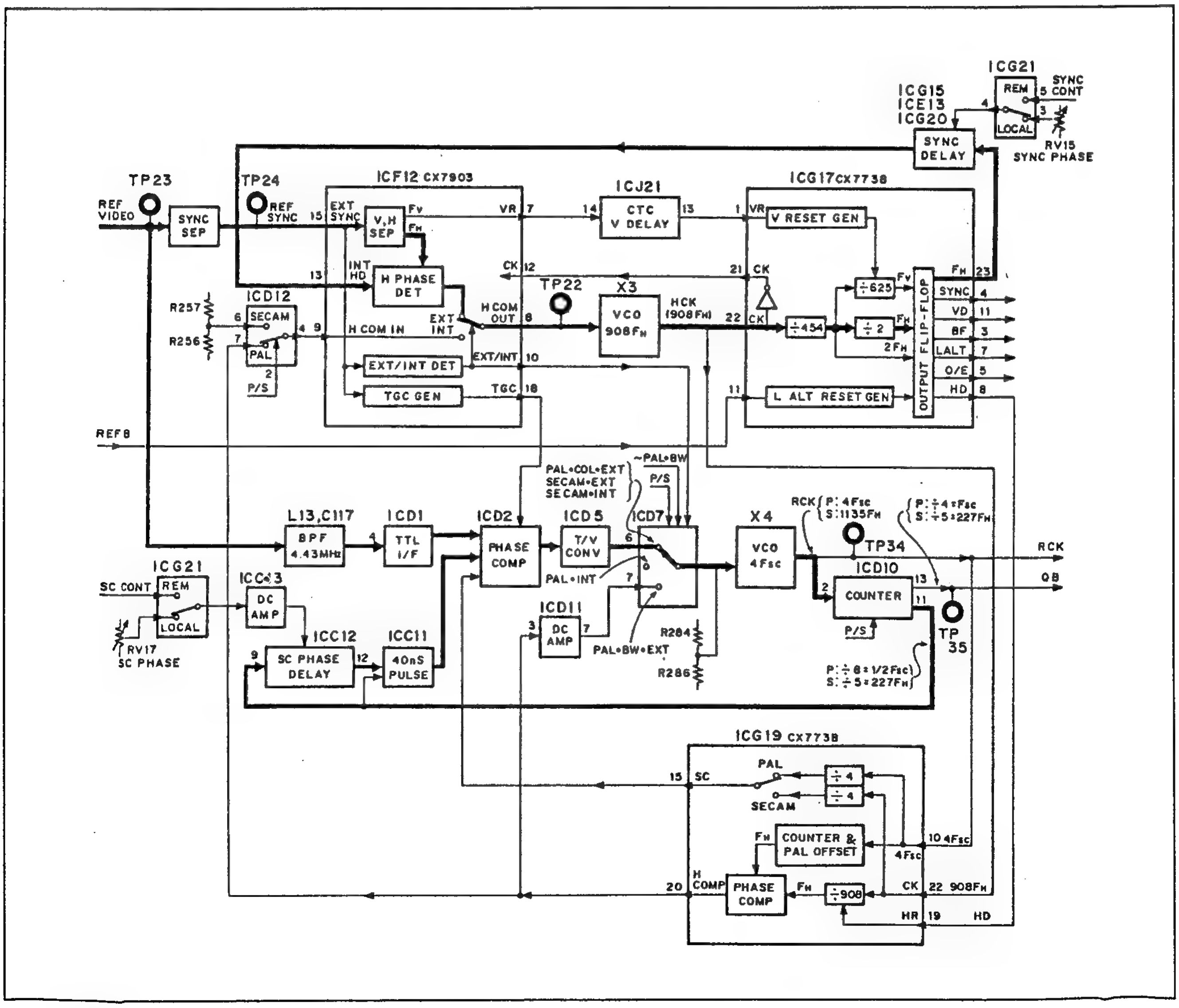


Fig. 4-4-39. Sync/Subcarrier Generators : PAL · EXT · COLOR Mode (RD-7)

(b) PAL・EXT・B&W mode

In this mode, the 908FH frequency signal which is synchronized to the REF SYNC signal is generated and the 4Fsc signal is created for synchronization with the 908FH signal.

As with the PAL・EXT・COLOR mode, the 908FH signal is similarly generated in the sync generator loop.

The 908FH signal synchronized with the REF SYNC signal and the 4Fsc VCO (X4) output are supplied to the phase comparator circuit (ICG19 : CX773B). ICG19 divides down the 908FH and 4Fsc signals to create two FH pulses. PAL offset is applied to the FH pulse created from the 4Fsc signal. The phases of these two FH pulses are compared, the voltage arising from the resulting phase difference is output from ICG19 pin 20 and supplied to the 4Fsc VCO, and a loop is configured. The Fsc and FH pulses stand in the following relationship :

$$4Fsc = \left(1135 + \frac{4}{625}\right) F_H$$

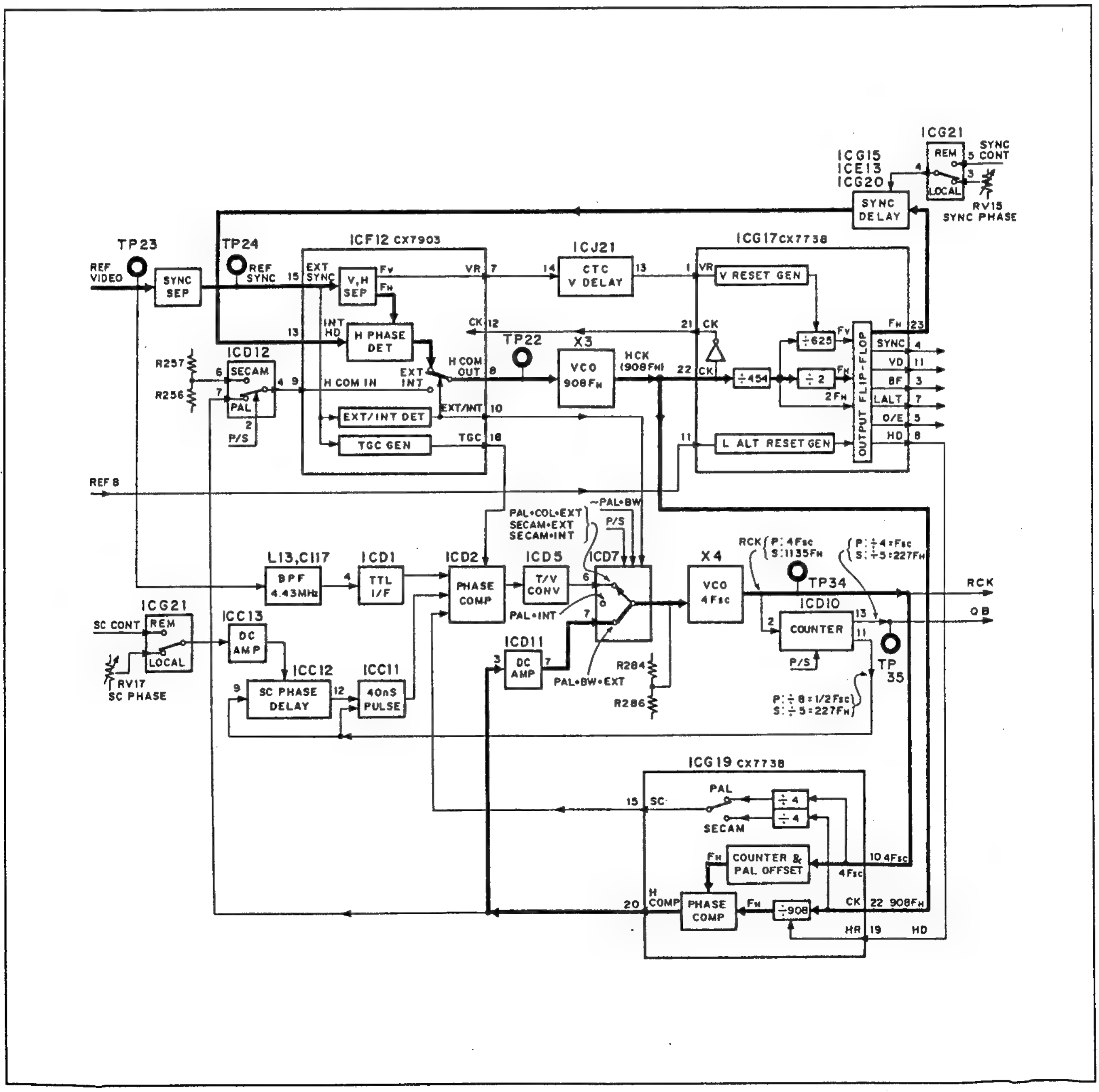


Fig. 4-4-40. Sync/Subcarrier Generators : PAL・EXT・B&W Mode (RD-7)

(c) PAL・INT mode

In this mode, fixed oscillation is provided by the 4Fsc VCO (X4) and the 908FH VCO is synchronized with it.

In the PAL・INT mode, the ICD7 selector selects a high impedance and the voltage produced by dividing +5V by R284 and R286 serves as the 4Fsc VCO control voltage.

As with the PAL・EXT・B&W mode, the phase of the 908FH VCO (X3) output signal is compared by ICG19 with the phase of the 4Fsc VCO output signal, the voltage arising from the phase difference is supplied to the 908FH VCO, and a loop is configured. The Fsc and FH pulses stand in the following relationship :

$$4Fsc = \left(1135 + \frac{4}{625}\right) F_H$$

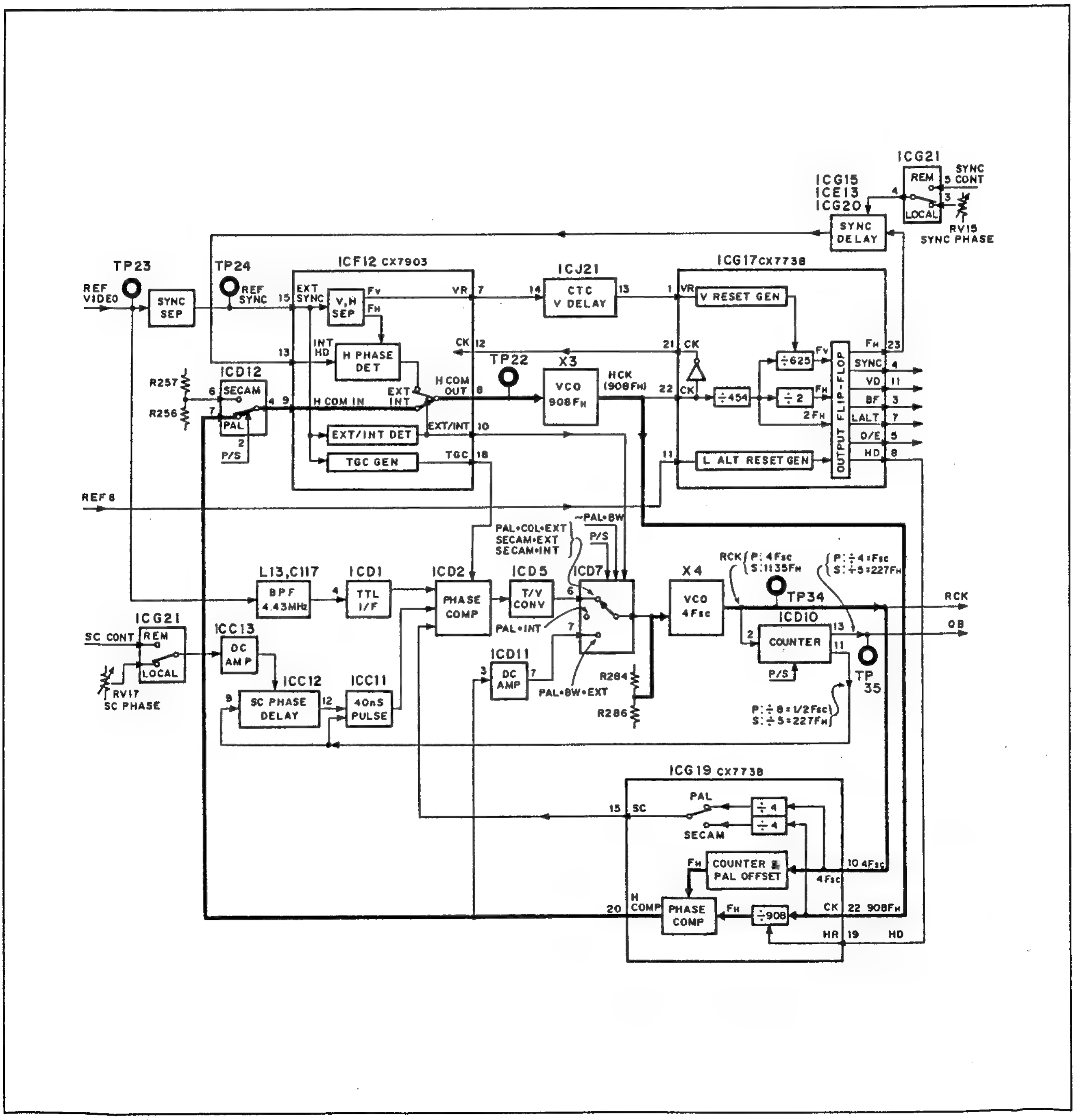


Fig. 4-4-41. Sync/Subcarrier Generators : PAL・INT Mode (RD-7)

(d) SECAM • EXT mode

In this mode, the 908FH (HCK) signal synchronized with the REF SYNC signal is generated by VCO X3 and the RCK signal synchronized with this is generated by VCO X4.

The 908FH signal is generated in the same way as in the PAL • EXT • COLOR mode.

The VCO X4 output signal is divided down by 5 in ICD10 and the phase of the resulting signal is compared in ICD2 with the phase of the VCO X3 (908FH) output signal which has been divided by 4. The phase difference is converted into a voltage by ICD5 and supplied to VCO X4, and a loop is configured. The frequencies of the RCK and HCK signals applying in this case stand in the following relationship.

$$RCK = \frac{5}{4} HCK$$

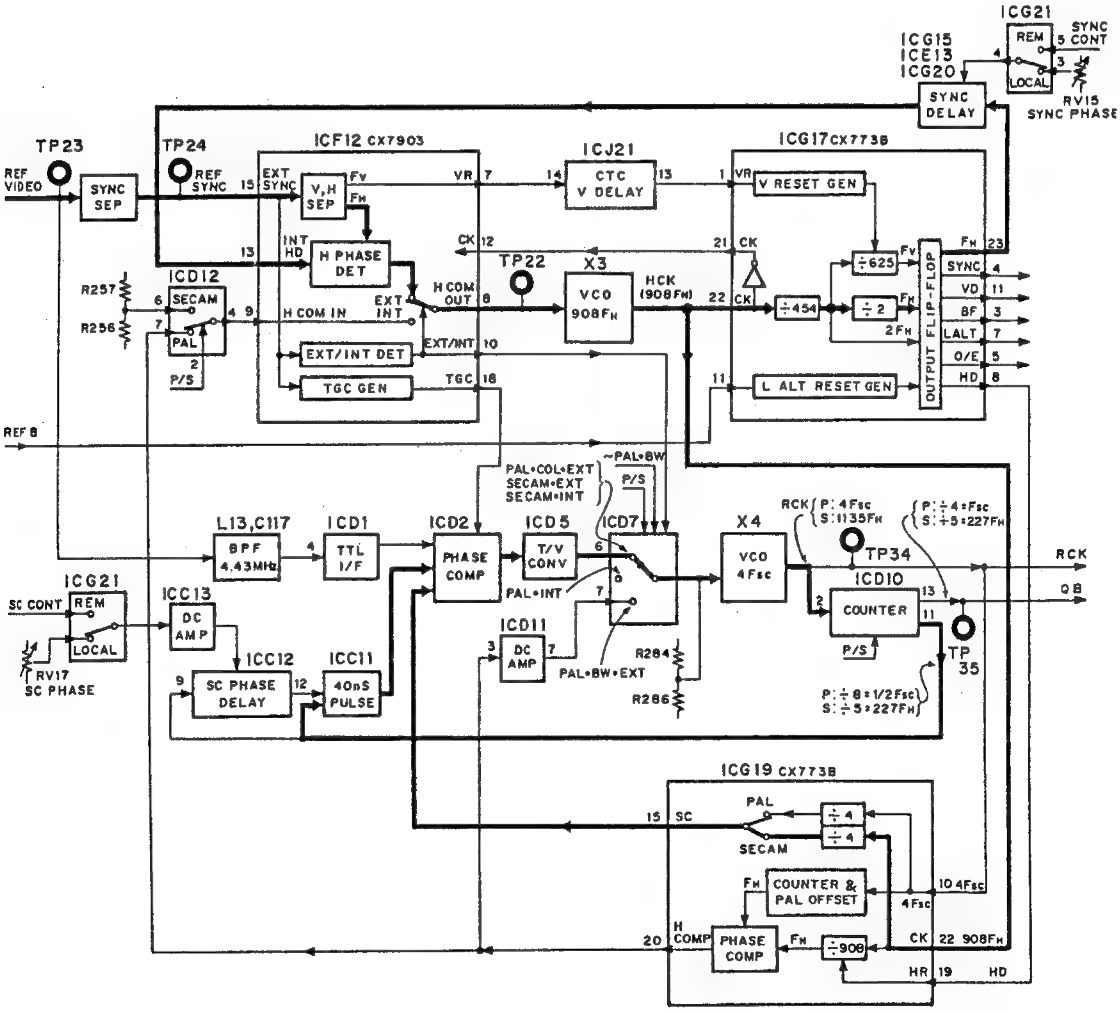


Fig. 4-4-42. Sync/Subcarrier Generators : SECAM • EXT Mode (RD-7)

(e) SECAM • INT mode

In this mode, the voltage produced by dividing +5V with R257 and R256 serves as the the 908FH VCO control voltage, and the 908FH VCO generates a fixed oscillation frequency. As with the SECAM•EXT mode, VCO X4 is synchronized with the 908FH signal.

$$RCK = \frac{5}{4} HCK$$

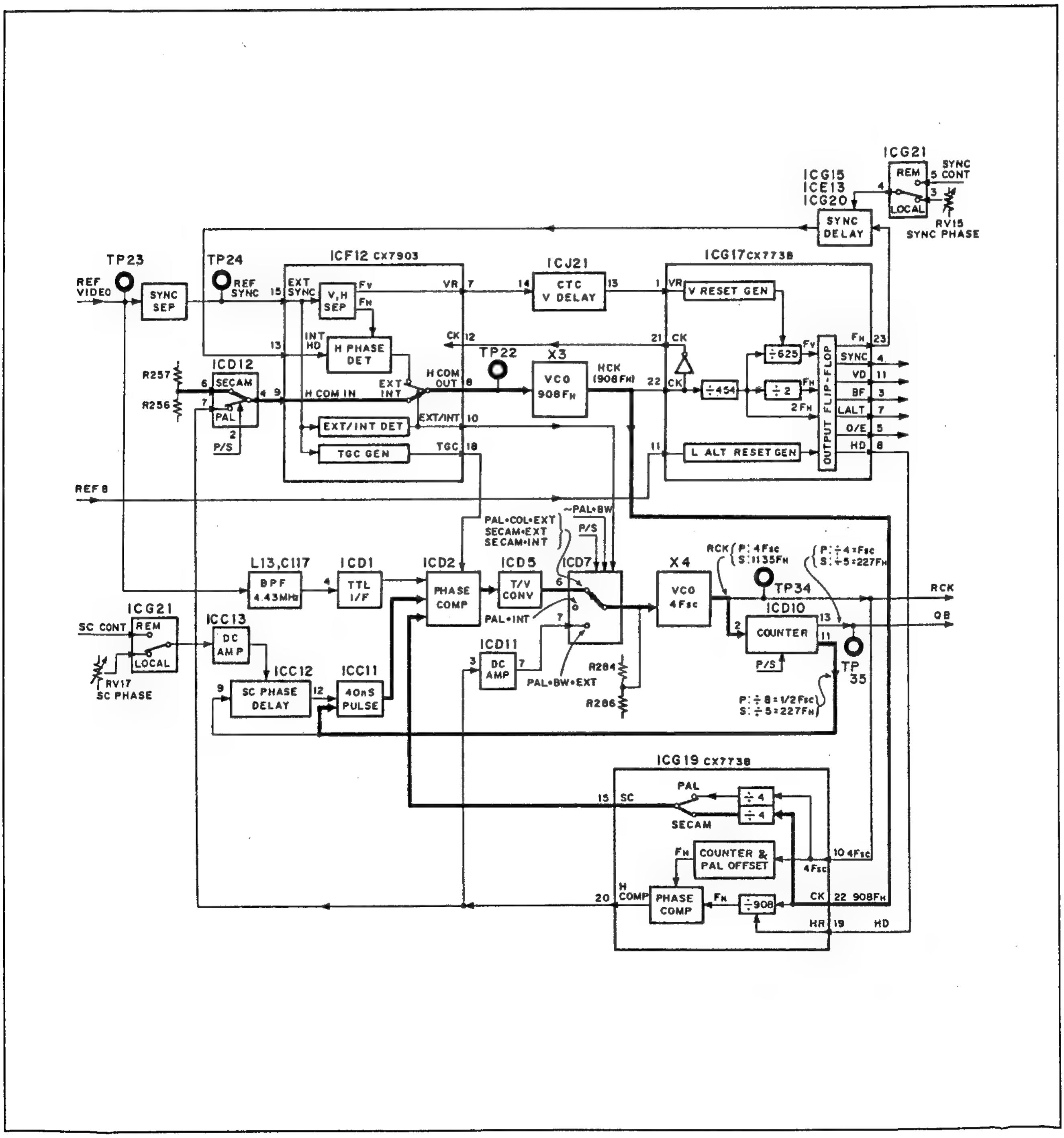


Fig. 4-4-43. Sync/Subcarrier Generators : SECAM • INT Mode (RD-7)

(4) V phase control (RD-7 board)

The TBC sync signal is synchronized to the reference sync signal by resetting the sync generator using the VR (V reset) signal generated from the reference sync signal by the ICF12 gen-lock driver. Depending on the mode, the VR signal is delayed by the CTC (ICJ21 : μ PD71054C) and, as a result, the vertical phase of the TBC sync signal is delayed. The 454FH pulse, which is produced by dividing down by 2 the 908FH VCO output is used for the CTC clock signal.

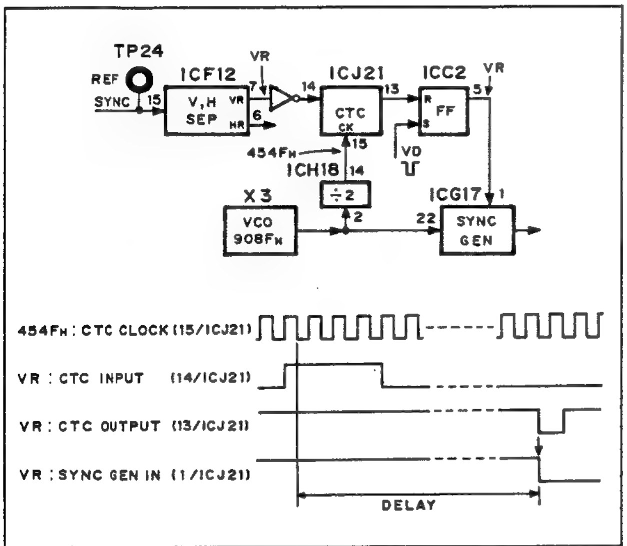


Fig. 4-4-44. V Reset Delay Circuit (RD-7)

The vertical phase of the video signal read from the main memory is determined by the REF VN signal. Depending on the mode, the VD pulse generated by the sync generator is delayed by the CTC (ICJ19 : μ PD71054C) to form the REF VN signal. The R ZERO signal is used as the H rate pulse with a timing delayed slightly from the VD pulse for the CTC clock signal.
The video signal which is read from the main memory is further delayed by the CK board and PR board. The following table lists the VR signal delays and video signal delays for each of the various modes.

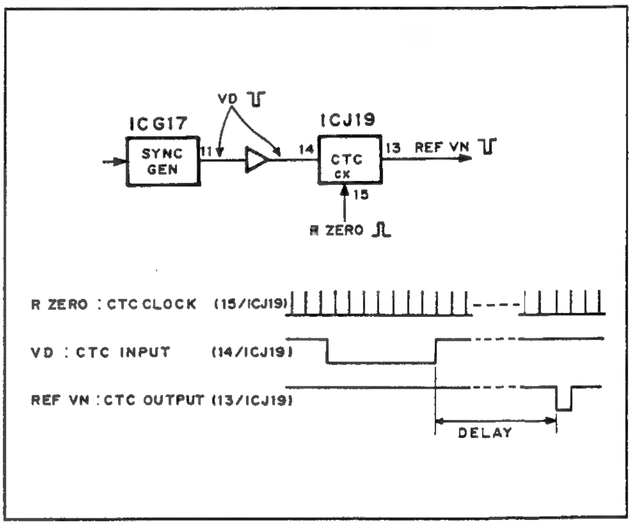


Fig. 4-4-45. REF VN Generator (RD-7)

VTR status			VR delay	Video signal delay		
Mode	PR board	PAL SECAM		REF VN	CK board	PR board
NORMAL	PR-92	×	0*5	0*5	0	0
	PR-98	×	0*5	0*5	0	2H
EE NON DELAY*1 or PREVIEW NON DELAY*2	PR-92	×	0	0	4H	0
	PR-98	PAL	0	2H	4H	2H
		SECAM	0	0	4H	2H
EE DELAY*3 or PREVIEW DELAY*4	PR-92	×	8H	8H	0	0
	PR-98	×	8H	6H	0	2H
CONFI DELAY	PR-92	×	1/3V+13H	1/3V+13H	0	0
	PR-98	×	1/3V+13H	1/3V+11H	0	2H

*1 : When [I10. EE SYNC DELAY] menu is set to [DISABLE]
*2 : When [I11. EDIT SYNC DELAY] menu is set to [DISABLE]
*3 : When [I10. EE SYNC DELAY] menu is set to [ENABLE]
*4 : When [I11. EDIT SYNC DELAY] menu is set to [ENABLE]
*5 : There is no need to delay the VR and REF VN signals since the drum servo is advanced by

(5) Y ADD GATE and UMSC signal (RD-7)

The Y ADD GATE signal is a pulse which prohibits Y signal line adding in the DT playback mode and it indicates the lines which do not have video components. Using the VD pulse provided by the sync generator as the input and the R ZERO signal as the clock pulse, the CTC (ICJ19 : μ PD71054C) generates the Y ADD GATE signal.

Normally, the Y ADD GATE signal is low for 25 lines of the vertical blanking period. In the case of zero advance (see note below), the video start point is delayed so that it comes after the sync signal in the output signal and so this delay is added and the Y ADD GATE signal is created. This means that this signal has an increased width equivalent to 8H with PAL • PR98 and equivalent to 4H for PAL • PR92.

Note : Zero advance

When the sync signal of the TBC output is not delayed in the EE mode or EDIT mode, the vertical sync signal of the TBC output will have the same phase as the reference video signal. This is known as zero advance.

In the case of SECAM signals, the video start point is delayed by 6H but the Y ADD GATE signal width is not increased because this signal acts as the reference pulse of the UMSC signal which is described below.

The SECAM signals are frequency-modulated signals and lines where the subcarrier is not superimposed are characterized by noise. For instance, in the EE • NON DELAY mode, the subcarrier is added to the 4 lines following the vertical blanking period and the lines are replaced with a black picture. The UMSC signal functions to indicate those lines which are to be replaced with the black picture.

The UMSC signals are produced from the Y ADD GATE signal, V ID signal and the signal generated by the two CTCs (ICJ18 : μ PD71054C) which use the VD pulse as the input and the R ZERO signal as the clock. The V ID signal serves to indicate the lines where the SECAM ID signal is to be superimposed.

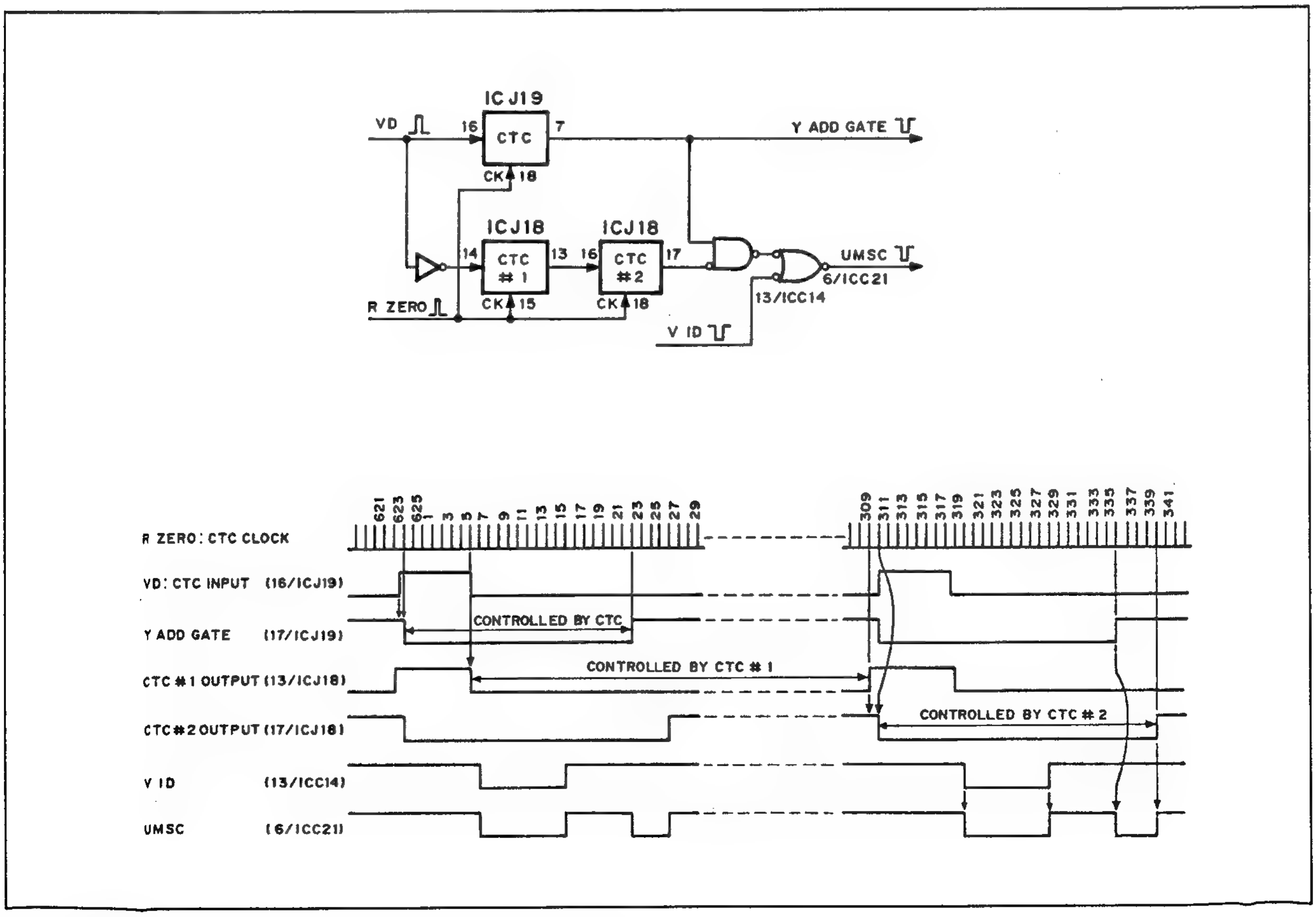


Fig. 4-4-46. Y ADD GATE/UMSC Generator (RD-7)

When the SECAM • PB COLOR • $\overline{\text{F BID}}$ mode is established, the UMSC signals are generated as shown in the figure below.

A. EE • DELAY EN
B. EE • DELAY DISABLE
C. PLAY STATUS • EDIT • DELAY DISABLE
D. PLAY STATUS • $\overline{\text{EDIT • DELAY DISABLE}}$
E. BID • EDIT • DELAY DISABLE
F. BID • $\overline{\text{EDIT • DELAY DISABLE}}$
G. DT • Y ADD OFF
H. DT • Y ADD ON

Note: The "PLAY STATUS" signifies the NORMAL FWD mode or EE mode in which the capstan servo is locked.

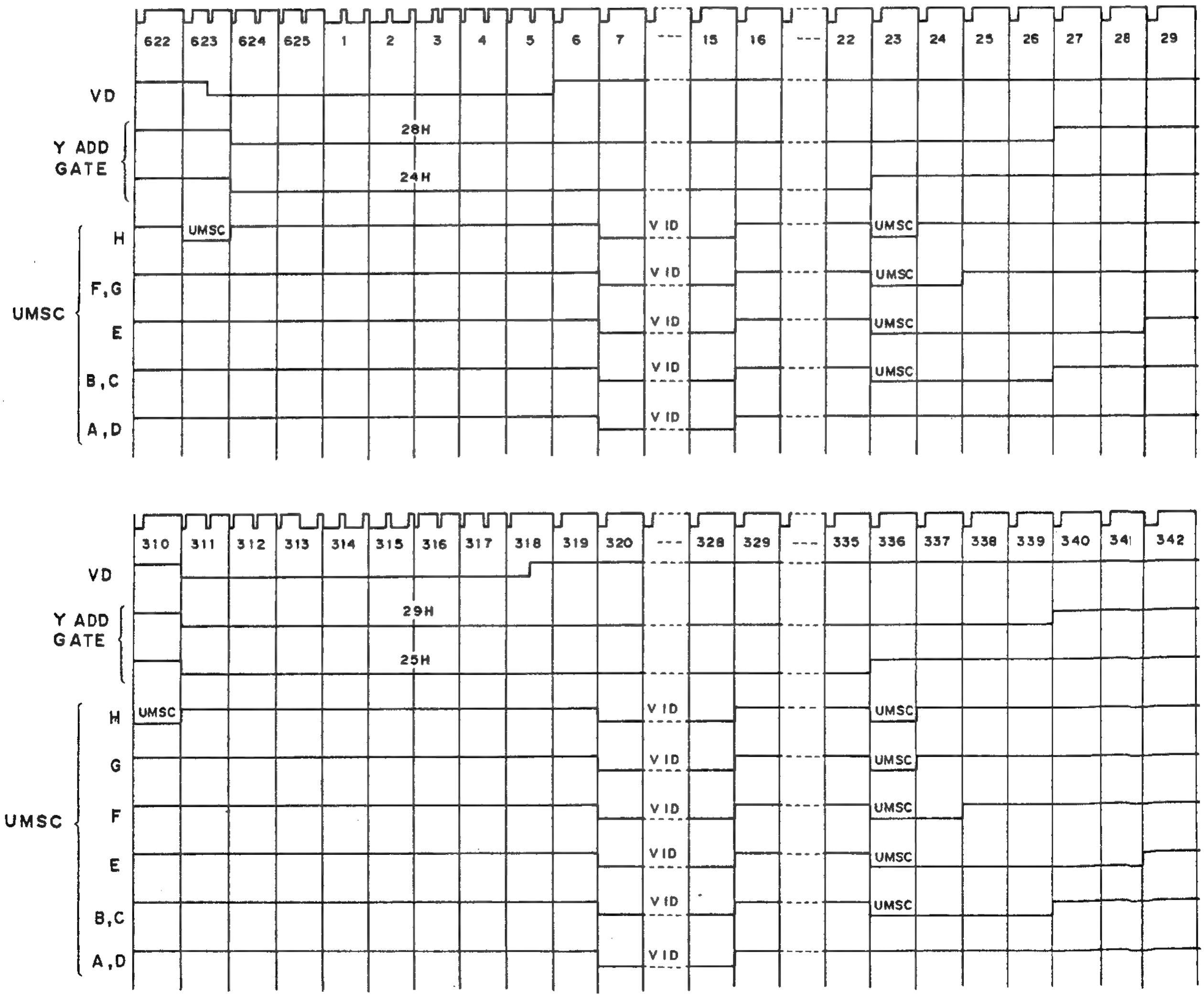


Fig. 4-4-47. UMSC Signals : SECAM • PB COLOR • $\overline{\text{F BID}}$ Mode

(6) SECAM B&W mode

In the PAL mode, the COL/B&W signal which is detected from the reference video signal determines whether the burst signal is to be added to the TBC output signal. The burst signal that is added is created from the reference video signal.
However, in the SECAM mode, the burst (line ID) signal read from the main memory is added to the TBC output signal without change or modification. If the burst signal is added again, discontinuity will result in the carrier and the color will be disturbed. Consequently, whether the picture is to be in color or B&W for the SECAM mode is determined not by the REF COL/B&W signal but by the PB COL/B&W signal. This PB COL/B&W signal also determines whether the SECAM ID (V ID) signal is to be added to the TBC output signal.
A description of each of the SECAM B&W modes is given below.

(a) BLACK BURST ENABLE (188 menu)
The TBC output signal forms a black picture or black-and-white striped picture, depending on what has been selected in the [188. BLACK BURST OUTPUT] menu. The PB COL/B&W signal is low (=B&W) at this time and so the TBC output signal does not have the V ID signal and line ID signal.

(b) PR TEST 1 ENABLE (T05 menu)
When the PB COL/B&W signal is high (=COL), the V ID signal is added to the TBC output signal; when it is low (=B&W), it is not added. Regardless of the status of the PB COL/B&W signal, the line ID signal is not added. If the monitor is the type which detects the V ID signal, noise will affect the whole screen in the PB COLOR mode, and a signal without the line ID and subcarrier will be output for use in the TEST mode.

(c) BVB ENABLE (S06 menu)
When the PB COL/B&W signal is high (=COL), the V ID signal is added to the TBC output signal; when it is low (=B&W), it is not added. The video lines of the TBC output have the line ID and subcarrier when the PB COL/B&W signal is high and a black picture is produced.

(7) Blanking pulse generator (RD-7 board)

The horizontal (H) blanking pulses are produced from the HD pulses by ICF20. Their width differs depending on whether the signals are SECAM or PAL (and SECAM B&W) and this means that the time constant of ICF20 is switched by ICH14. The pulses are supplied to ICJ13 and mixed with the vertical blanking pulses produced by ICJ13.

The vertical blanking pulses are created from the VD pulses by ICJ13 (CX20162). ICJ13 is provided with a pin which controls whether lines 7 through 22 (320 through 335) are to be blanked or not, and the control signal specified by the [180. BLANKING LINE] menu is input to this pin. The blanking width of line 23 is based on the half H pulse provided by ICJ6.
ICJ13 also creates the SECAM V ID pulses.

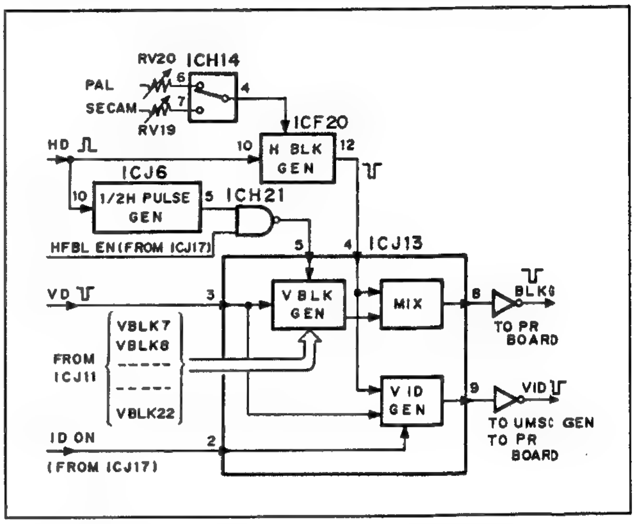


Fig. 4-4-48. Blanking Pulse Generator (RD-7)

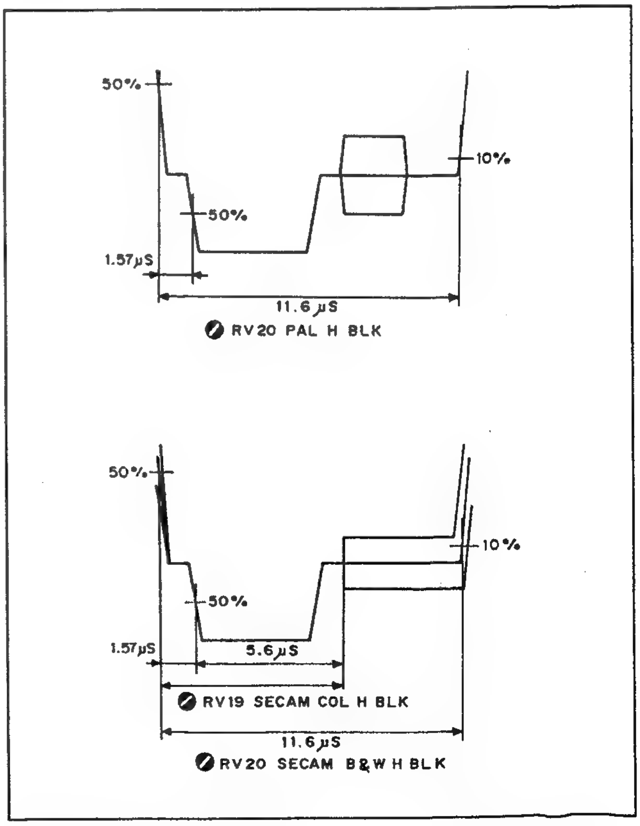


Fig. 4-4-49. H Blanking

4-4-7. Read Clock/Read Zero Generator (RD-7 Board)

(1) Burst-chroma phase controller (RD-7 board)

The Fsc pulse (QB) generated by the subcarrier generator is supplied to ICB10, and the RD Fsc signal whose phase is shifted 90° every other line is created. The RD Fsc signal is sent to the PR board to serve as the PAL burst signal.
Prior to its 90° shift, the Fsc pulse is supplied to pin 1 of the ICB1 monostable multivibrator, its phase is shifted by the BURST CHROMA control (RV23 or remote control), and the REF CK signal is produced. The phase of this REF CK signal is then shifted by ICB1/RV25 and modulated in the next stage by the velocity error voltage, after which the fourth-order harmonics are extracted to produce the read clock signal for the PAL mode.
The REF CK signal is also sent to the PR board where it is used to create the DECODE/ENCODE CARRIER.

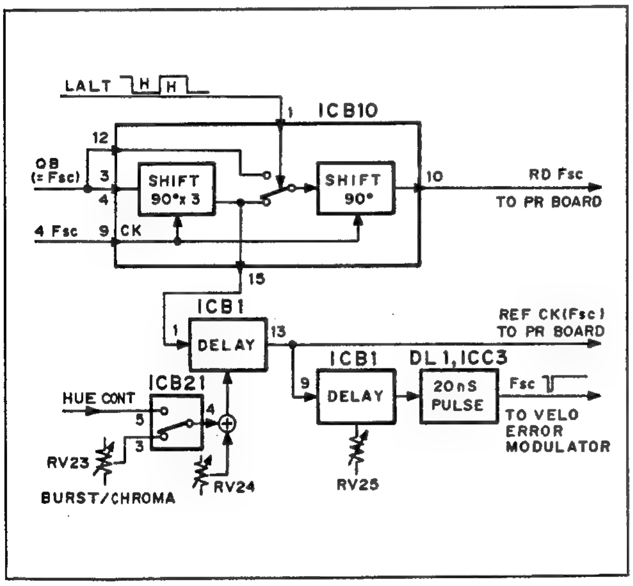


Fig. 4-4-50. Burst-Chroma Phase Controller (RD-7)

(2) Velocity error modulator and read clock generator (RD-7 board)

After the phase of the Fsc pulse has been adjusted by the burst-chroma phase controller, it is modulated by the velocity error voltage. The DP VIDEO signal (Y signal sent from the write side for differential phase compensation) is superimposed onto the velocity error voltage, and phase modulation conducted for differential phase compensation is carried out simultaneously. In the SECAM mode, the signals bypass this circuit.

The Fsc pulse is supplied to pin 13 of the RS flip-flop which is composed of the ICB9 NAND gate, ICB9 pin 3 is set low at the fall edge of the pulse, and the output voltage of the sawtooth wave generator composed of ICB7, Q10 and Q11 starts to rise. This ramp wave is supplied to pin 3 of the ICC10 voltage comparator and ICC10 pin 9 is set low when the velocity error voltage supplied to pin 4 is exceeded. The ICC10 pin 9 output enters pin 1 of the ICB9 flip-flop, the RS flip-flop output is reset high, and the ramp wave (TP25) is reset. When the next Fsc pulse is supplied to the RS flip-flop, the same operation is repeated. As a result, the phase of the pulse which is output from ICC10 pin 9 is shifted in accordance with the velocity error voltage.
The fourth-order harmonic components of the phase-modulated Fsc pulse are filtered out by the FL1 bandpass filter and the PAL read clock is created.
In the SECAM mode, both velocity error and differential phase compensation are not necessary and so the 1135FH pulse, which is created by the sync generator circuit, is used without change or modification as the read clock signal. ICC5 functions to select the PAL and SECAM read clock signals.

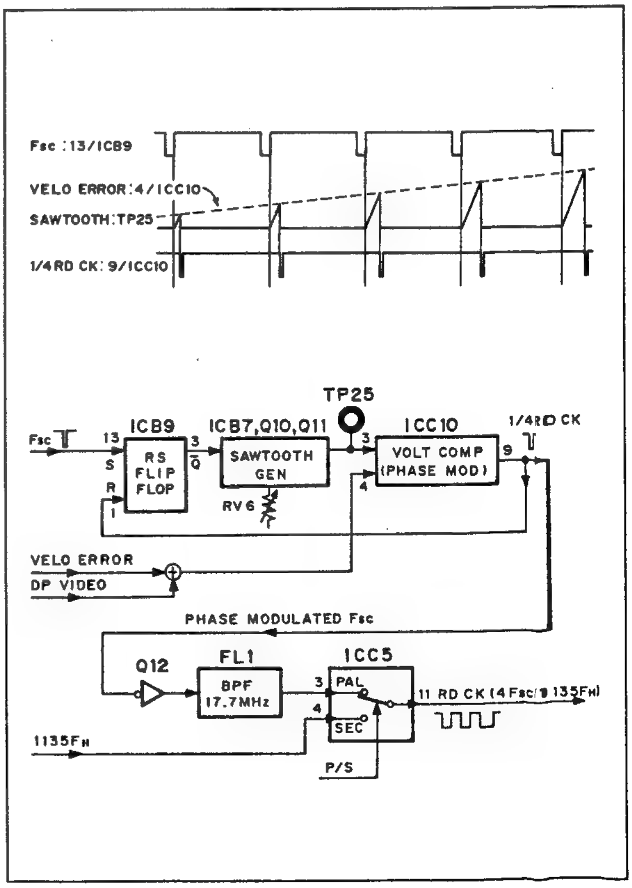


Fig. 4-4-51. Velocity Error Modulator and Read Clock Generator (RD-7)

(3) PAL H generator and REF SCH detector (RD-7 board)

The PAL H generator is composed of the V sawtooth wave generator, H sawtooth wave generator, voltage comparator and SC-H phase comparator. The PAL H pulse is the signal produced by removing the V/2 offset from the HD pulse created by the sync generator, and it serves as the reference signal for creating the PAL read zero signal.

The V sawtooth wave is produced from the VD pulse by the integrator (ICE19) and analog switch (ICF21). The H sawtooth wave is produced from the HD pulse by the switching transistor (Q13), constant-current source (ICE19, Q14) and capacitor (C153). By comparing the two voltages in ICD20, H pulse whose phase has been modulated by the V sawtooth wave is created. The ramp of the V sawtooth wave is adjusted so that the H pulse phase advances by an amount equivalent to half the subcarrier period per field. As a result, the PAL H pulses with phases of 0°, 270°, 180° and 90° with respect to the subcarrier are output in this sequence from ICD20. The 4Fsc (RD CK), Fsc (1/4 RD CK), N/I (LALT/2) and RD FLD (O/E) signals are supplied to ICE15, 1/Fsc interval pulse whose phase with respect to the subcarrier commences at 0°, 270°, 180° and 90° is created, and the phase of the pulse is compared with that of the PAL H pulse in ICD19 and ICC19. The phase difference is converted by ICC17 into a voltage, and a loop is configured by adding this phase difference voltage (TP36) to the V sawtooth wave and it is controlled so that the PAL H pulse phase will be made constant.

When the phase difference voltage (TP36 : TBC REC SCH signal) exceeds ±3V, the CF RESET signal is created by DT CPU (ICM18) and gated by the VD pulse in ICC15, and the phase difference voltage is reset during the vertical blanking period.

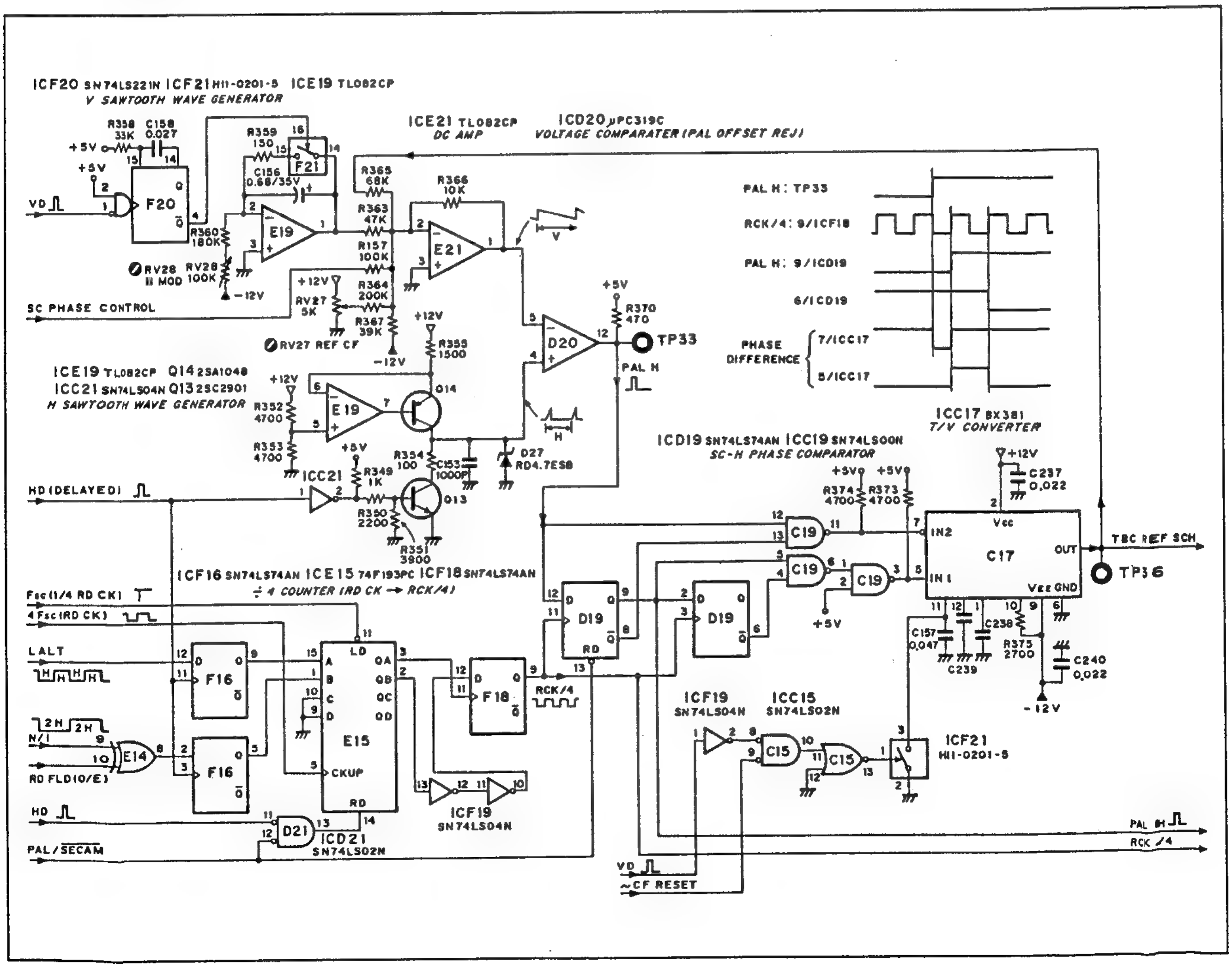


Fig. 4-4-52. PAL H Generator and REF SCH Detector (RD-7)

(4) READ ZERO generator (RD-7)

The READ ZERO generator is composed of the CTC (ICJ21 : μ PD71054C) and the counter (ICA12 and D14 : SN74LS163AN). In the PAL mode, the READ ZERO pulse is created based on the PAL H pulse ; in the SECAM mode, it is created based on the HD pulse. ICD21 functions to select the PAL H and HD pulses.

The READ ZERO pulse is created at a position which allows for the system delay from the WRITE ZERO pulse. The PAL H pulse is positioned between the READ ZERO 2 and READ ZERO 3 pulses, as shown in Fig. 4-4-53, and the CTC uses this PAL H pulse as its input and, with the RCK/4 pulse serving as the clock pulse, the counter (ICA12) load pulse is output in each mode. The RCK/4 pulse is created when the RD CK pulse is divided by 4 in ICE15 (Fig. 4-4-52). The ICE15 load data are latched by the HD pulse and so the RCK/4 pulse is characterized by discontinuity in the vicinity of the leading edge of the HD pulse. The RD CK pulse is a signal which has undergone velocity error compensation, which means that the RCK/4 pulse is discontinuous at the timing (1 to 2 μ sec from the leading edge of the H sync pulse) when the velocity error is reset. In order to prevent ICA12 from counting at these timings, the READ ZERO JUMP signal is set low for the READ ZERO 1 and READ ZERO 3 pulses.

The VPF1 and VPF2 signals provide the fine adjustment in each mode. The READ ZERO SHIFT signal is set high when the N/I signals of the write and read sides do not match. The READ ZERO pulse is shifted by 2 clocks at this time to prevent color reversal.

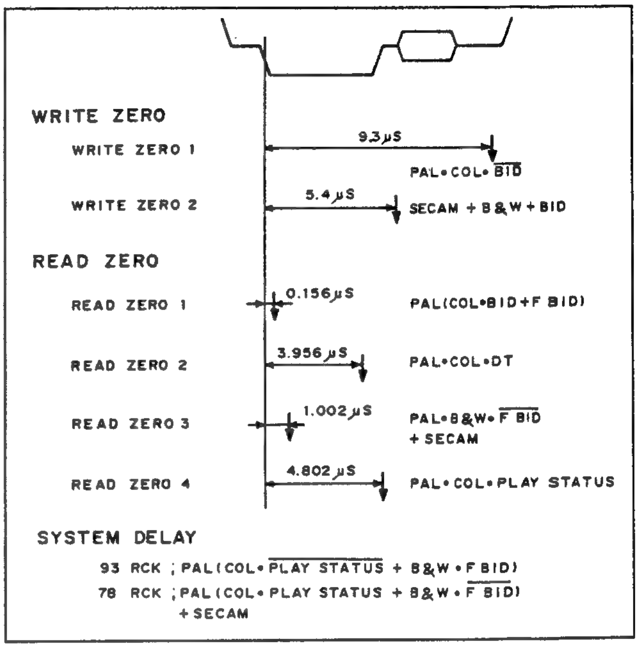


Fig. 4-4-53. READ ZERO Timing

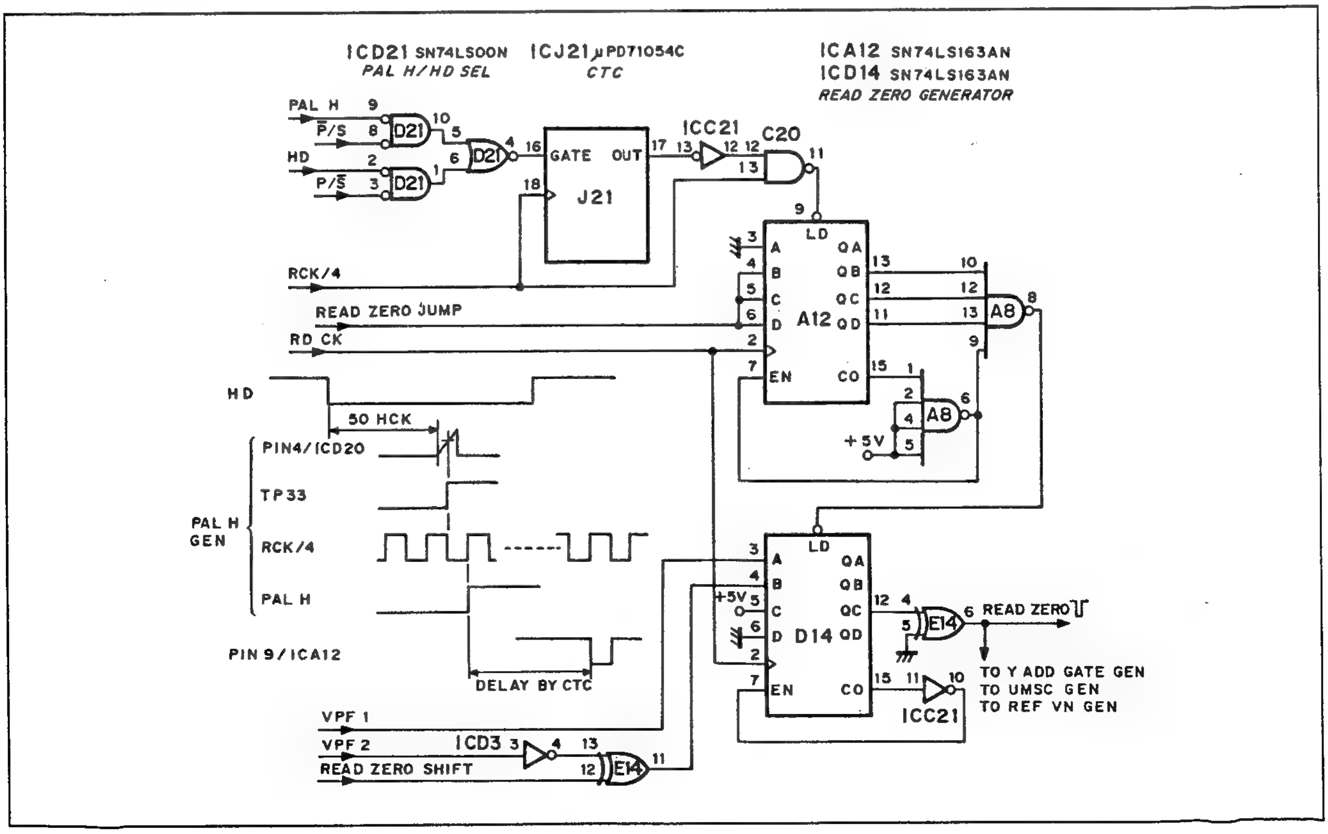


Fig. 4-4-54. READ ZERO Generator (RD-7)

4-4-8. Velocity Error Interpolator (RD-7 Board)

The velocity error voltage which has been decoded on the CK board is supplied to the velocity error interpolator on the RD-7 board. In the interpolator, it is interpolated by second order approximation so that it approaches a true velocity error.

The two-line adding of the velocity error voltage is conducted together with the line adding of the chroma signal.

The Y signal, which has been D/A converted, is first added to the interpolator output for DP compensation and it is then sent to the read clock generator so that the phase of the read clock will be modulated.

The principle of interpolation by the second order approximation is shown in Fig. 4-4-55. ϕ is the velocity error and t_H is the 64 μsec H period. $t=0$ is the timing at the W CK head (timing with APC applied to W CK). At this time, ϕ is equal to 0.

If it is assumed that the velocity error of a particular line L_0 is ϕ_0 and the velocity error of the line before L_{-1} is ϕ_{-1} then the second order approximation of the change in the velocity error at L_0 will be as follows :

$$\phi = \frac{1}{2t_H}\left\{\frac{1}{t_H}(\phi_0 - \phi_{-1})\,t^2 + (\phi_0 + \phi_{-1})\,t\right\} \cdots (1)$$

In the actual circuit, velocity errors ϕ_0 and ϕ_{-1} are ϕ-V converted and obtained as voltages V_0 and V_{-1}. The velocity error second order approximation interpolator is a circuit that generates the voltage below using V_0 and V_{-1} in correspondence with formula (1).

$$V = K\left\{\frac{1}{t_H}(V_0 - V_{-1})\,t^2 + (V_0 + V_{-1})\,t\right\} \cdots (2)$$

In Fig. 4-4-55, C144 holds V_{-1} and the voltage $C(V_0 - V_{-1})\,t$ produced by integrating $V_0 - V_{-1}$ is output to pin 1 of ICB14. V_0 and V_{-1} are then added to this voltage and when this is supplied to next-stage integrator ICB12, the voltage in the following formula is obtained at pin 1/ICB12 and formula (2) is realized.

$$K\left\{\frac{1}{t_H}(V_0 - V_{-1})\,t^2 + (V_0 + V_{-1})\,t\right\}$$

The voltage produced here is supplied to the velocity error moudlator, V-ϕ converted and, as a result, formula (1) is realized.

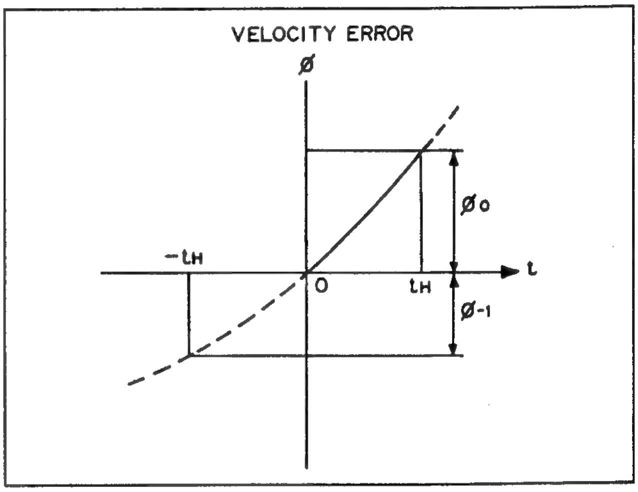


Fig. 4-4-55. Principle of Interpolation by 2nd-Order Approximation

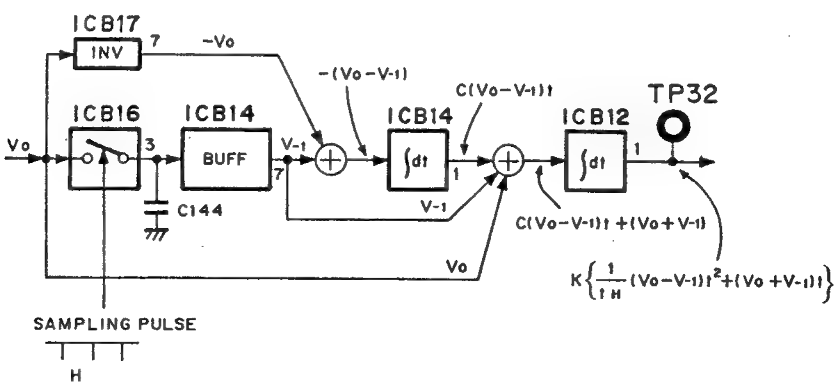


Fig. 4-4-56. 2-Line Adding and Interpolation by 2nd-Order Approximation (RD-7)

The integration capacitor in the interpolator is discharged by the HD pulse which is ahead of the read zero signal, and the velocity error voltage is reset. During the VD period, the resetting mode is established and the interpolator output is turned into a constant DC voltage.

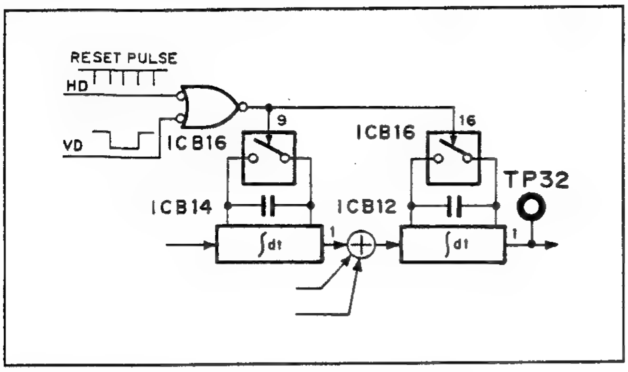


Fig. 4-4-57. Velocity Error Reset (RD-7)

4-4-9. DP Video Modulator (RD-7, PR-98/92 Boards)

DP (Differential Phase) is compensated, as outlined below, in the TBC block.
The 8-bit Y signal data supplied from the Y/C separator circuit is converted into an analog signal by ICJ9 (or by ICK5 on the PR-92 board). The offset and gain of this analog Y signal are then adjusted by RV1 and RV2, and the signal is further supplied to the RD-7 board for the purpose of DP compensation.
The DP VIDEO (analog Y) signal supplied to the RD-7 board is added to the velocity error and supplied to the phase modulator circuit of the read clock. DP is compensated by reading out the video data from the memory using the phase-modulated read clock signal.

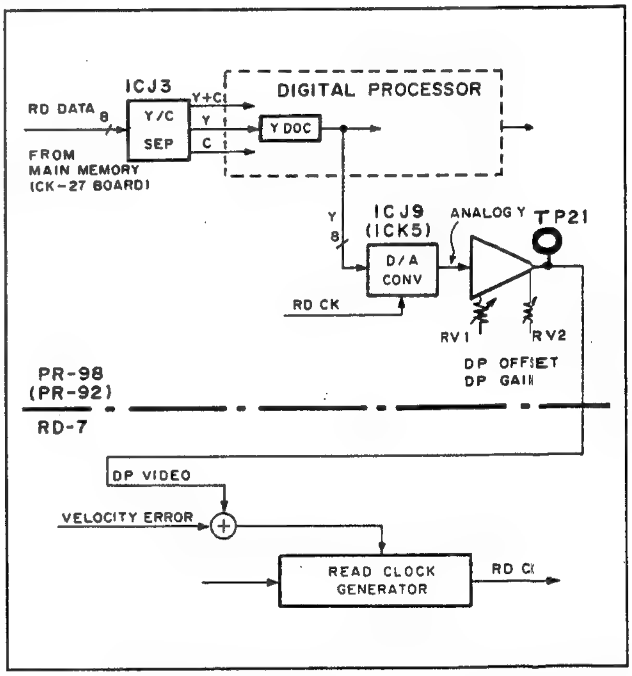


Fig. 4-4-58. DP Video Modulator (RD-7, PR-98/92)

4-4-10. Digital Processor/BKH-3020 (PR-92 Board)

Note : PR-92 board have currently three types respectively, having the part numbers' last two digits of "-11", "-12" and "-13". The same circuit components sometimes have the different reference numbers in the "-11" /-12" and "-13". In order to avoid confusion, the reference numbers for the PR-92 board ending by "-13", are omitted in the subsequent description.

During dropout compensation (DOC) and BIDIREX playback, this circuit serves to correct the digital video signals which have been read out from the main memory (and freeze memory) of the CK-27 board. Fig. 4-4-59 shows the basic configuration. The main memory output is separated into the Y signal and the chroma signal and each signal is then processed respectively. The Y signal and C signal system circuitry functions in combination in accordance with the various modes, and the signal processing route are thus all shown together in section (4) "processing by individual mode".

(1) Y/C separator (PR-92 board)

This circuit serves to separate the Y signal and chroma signal from the digital composite video signal which is output from the main memory, and the actual processing is done by ICJ3 CX23082.
The CX23082 IC is composed of a CMOS gate array with 8000 gates and its main functions are outlined below.

1. Main line delay circuit (adjustable) with 2 independent input systems (switchable)
2. 9-bit input, 10-bit maximum output
3. Chroma phase inversion function
4. Chroma inhibit function
5. Rounding in accordance with word length used
6. Selectable between straight binary (offset binary) and 2's complement
7. Maximum operating frequency of 20 MHz

Fig. 4-4-60 shows the configuration of the CX23082 circuit. The Y signal is taken out by subtracting the chroma signal from the input signal. Fig. 4-4-61 shows the frequency response of the chroma filter. The frequency response of the Y filter is complementary to the chroma filter.

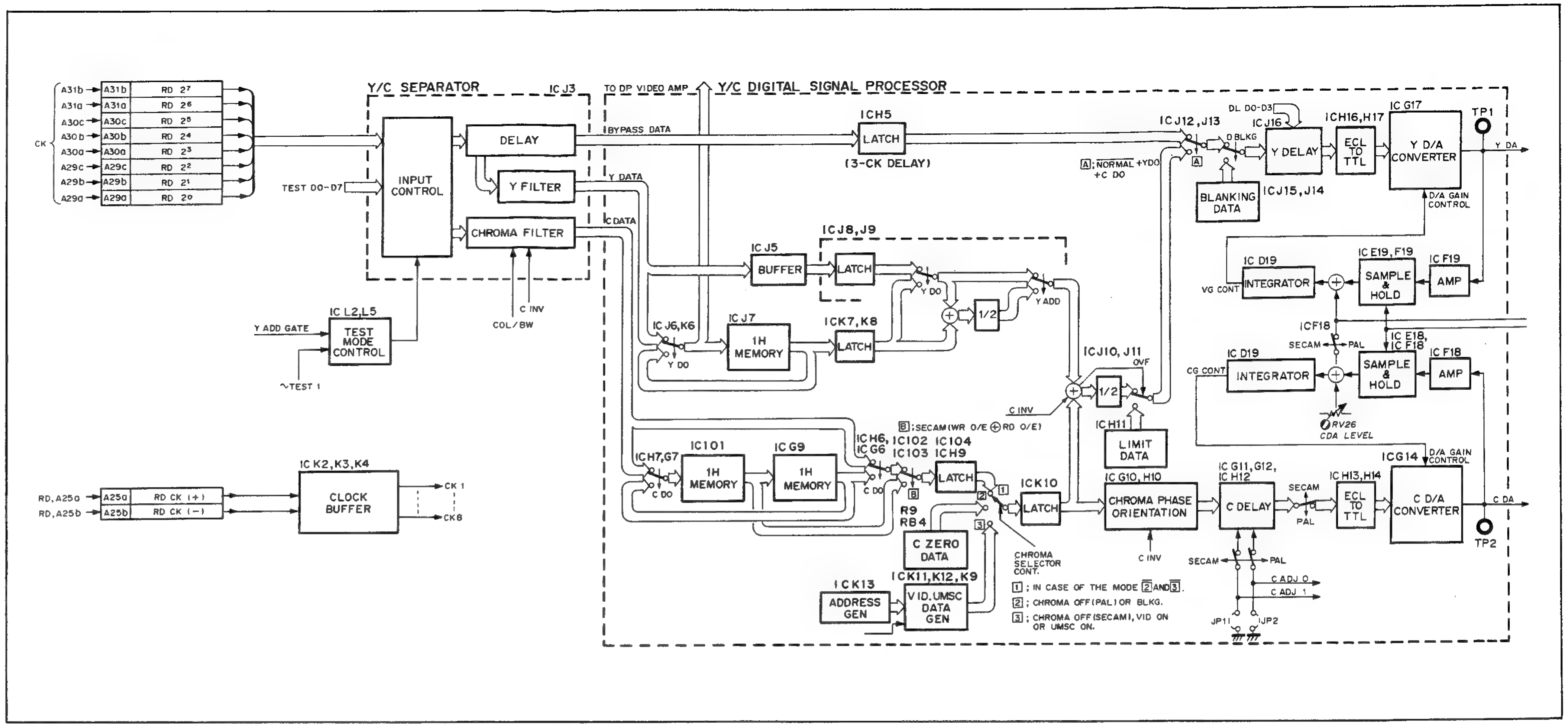


Fig. 4-4-59. Digital Processing Circuit/BKH-3020 (PR-92)

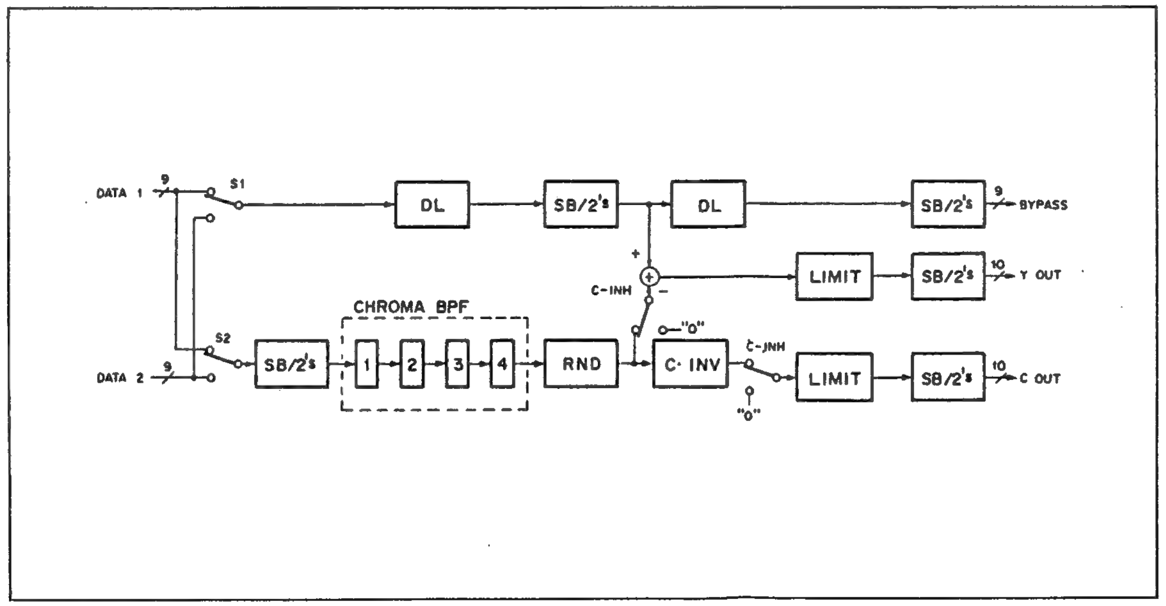


Fig. 4-4-60. Configuration of CX23082 (ICJ3/PR-92)

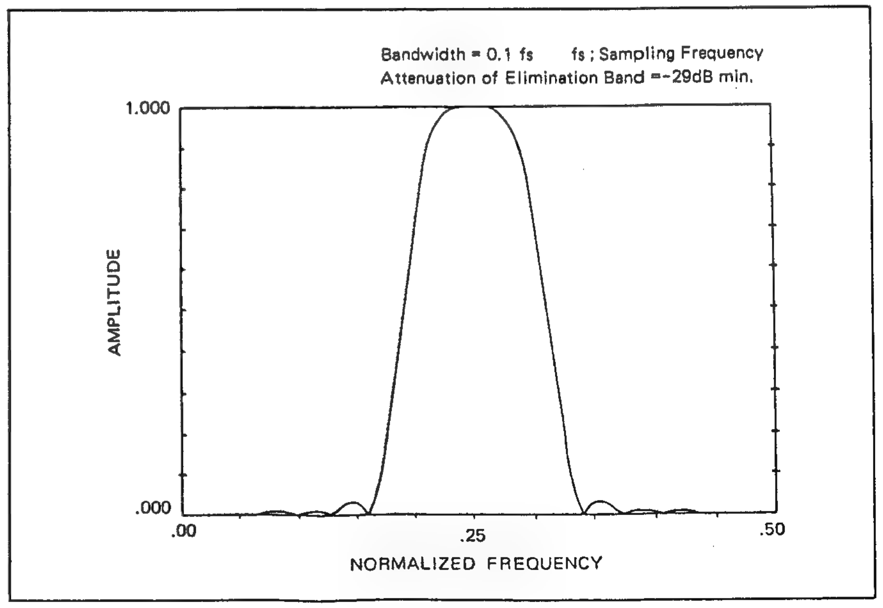


Fig. 4-4-61. Frequency Response of Chroma Filter (ICJ3/PR-92)

(2) Y signal digital processor (PR-92 board)

(a) Y signal dropout compensator (PR-92 board)

Dropouts in the Y signal are compensated for by "partial replacement using the Y signal of 1H before." The Y signal data which have been output from the ICJ3 Y/C separator are applied to terminal "1" of DO switcher ICJ6 and ICK6. The DO switcher output is delayed 1H by line memory ICJ7 and returned to terminal "0" of the DO switcher. The DO switcher normally selects terminal "1" but it is switched to "0" during the dropout period and the data of 1H before the dropouts are supplied to the line memory again.

The μPD41102C used for the memory devices is a FIFO (first-in, first-out) memory and so the memory addresses are created from the clock input.

(b) DOC control circuit (PR-92 board)

The DOC control circuit expands and delays the pulse width of the DO signal (Y DO) which has passed through the main memory and it outputs the DOC switching control signals which accord with the various modes.

The DOC control circuit employs a special-purpose IC (ICM9 : CX20219). Its main functions are outlined below.

1. Input DO pulse delay (38 to 50 clocks)
2. Pulse width expansion (±32 clocks)
3. DO processing switching of the previous line or the lines before and after
4. Line adding peripheral circuitry
5. RZ (READ ZERO) signal differential circuit
6. Maximum operating frequency of 20 MHz
7. Compatible with NTSC, PAL and SECAM systems

Fig. 4-4-62 shows the configuration of the CX20219 circuit.

(c) Y-ADD circuit (PR-92 board)

With variable speed playback such as in the DT/BIDIREX mode, the phenomenon inevitably occurs in which the field sequence of the playback video signal matches or fails to match the reference video signal. The matching/non-matching repeat period is long when the tape speed approaches ±1 times normal speed, but its length is reduced when the speed deviates from ±1 times normal speed.

When the field sequence does not match the reference video signal, it is made to match as far as appearances are concerned either by 1H delaying the even fields of the main memory output or by 1H advancing the odd fields. As a result, the picture in the mismatched field will shift downward by 0.5H. This is known as vertical (V) shift. Depending on the tape speed, the V shift phenomenon is perceived as flicker.

The Y-ADD ON mode is provided in order to smooth out the V shift to all appearances by line addition to the Y signal, and also to remove the flicker. Y signal line addition accompanies the delay and so, in the Y-ADD ON mode, the odd fields of write side are advanced by 1H.

The Y-ADD ON mode is specified by set up menu S84 : Y-ADD.

ICJ8 and J9 provide line addition for the ICJ5 output (Y signal) and ICK8 output (1H delayed Y signal). When dropouts occur in the Y-ADD ON mode, Y signal line addition is not provided and DOC is conducted.

The picture processed in the Y-ADD ON mode is natural and without flicker but when the tape speed approaches ±1 times normal speed, the picture will become defocused by the Y signal line adding and, depending on the design, an out-of-focus picture and a clear picture may appear alternately for long periods.

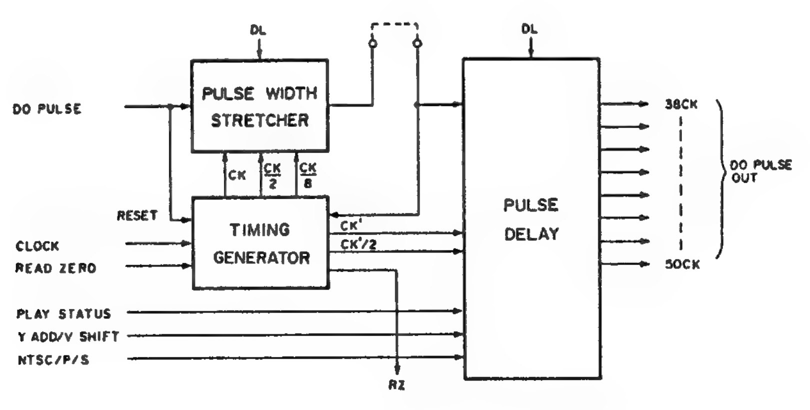


Fig. 4-4-62. Configuration of CX20219 (ICM9/PR-92)

(3) Chroma signal digital processor (PR-92 board)

(a) Chroma signal dropout compensator (PR-92 board)
Dropouts in the chroma signal are compensated for by the "partial replacement using the chroma signal of 2H before (line replacement when the dropouts occure in the burst signal)" in the PAL mode and by the "line replacement using the chroma signal of 2H before" in the SECAM mode.
Chroma signal DOC is performed by the 2H line memory (IC101 and ICG9). In other words, the data input into the 2H line memory are output immediately.
The data which are read out will be the data of 2H before and the dropout portion will be replaced by the chroma signal of 2H before.
The write line in the 2H line memory is determined by the W O/E (W D'R/D'B) signal.
The read line of the 2H line memory is the same line as the write line in the PAL mode.
In the SECAM mode, the 2H line read differs according to whether the playback mode is normal or BIDIREX. In the normal playback mode, it is the same line as the write line and in the BIDIREX mode, it is the same line as the write line or the line 1H after so as to provide line D'R/D'B alignment. When the W D'R/D'B and R D'R/D'B signals match, it is the same line as the write line and when they do not match, the line 1H after is the read line and the line D'R/D'B is aligned with the reference video signal.
In this way, the 2H line memory also functions to align the line D'R/D'B of the BIDIREX playback signal in the SECAM mode. This is in addition to its DOC function.

(b) Chroma off
When the S84 : CHROMA ON/OFF menu is set to OFF, the chroma signal is no longer output from the latch (ICK10) and the only the Y signal is output from the PR borad.
With CHROMA OFF, the chroma signal is not input to ICK10 from ICH9. In the SECAM mode, the unmodulated subcarrier provided by the SECAM ID generator (ICK9, K11, K12 and K13) is input to ICK10 and in the PAL mode, the chroma zero level data provided by the R4 and RB4 resistors are input to ICK10.

(4) Processing by individual mode (PR-92 board)

The operating modes of the TBC can be broadly classified into the NORMAL PLAY, DT, SLOW BIDIEX and FAST BIDIREX modes. The actual processing differs greatly depending on whether the playback video signal is a color signal or black-and-white signal and a PAL signal or SECAM signal.

• NORMAL PLAY mode
In this mode, the tape is played back at normal speed (+1×) and except when dropouts are present, the digital processor section is bypassed.
• DT mode
In this mode, the tape is played at any speed ranging between −1 and +3 times normal speed (except at the +1 times normal speed) using the PLAY head (DT head), and various processes are undertaken in order to yield playback which is free from guard band noise.
• SLOW BIDIREX mode
In this mode, the tape is played back at speeds up to ±8 times normal speed except in the NORMAL PLAY and variable play modes. The color is locked but guard band noise is produced.
• FAST BIDIREX mode
In this mode, the tape is played back at speeds exceeding ±8 times normal speed and the picture appears in black and white.

The signals are processed as follows in the NORMAL PLAY mode and DT/BIDIREX mode. Fig. 4-4-63 through 4-4-68 show the signal processing route in the various modes.

PAL or SECAM	NORMAL or BIDIREX	S83 CHROMA ON or OFF	S84 Y-ADD ON or OFF	Fig.
P/S	NORMAL	ON	×	4-4-63
P/S	NORMAL	OFF	×	4-4-64
PAL	BIDIREX	ON	ON	4-4-65
PAL	BIDIREX	ON	OFF	4-4-66
SECAM	BIDIREX	ON	ON	4-4-67
SECAM	BIDIREX	ON	OFF	4-4-68

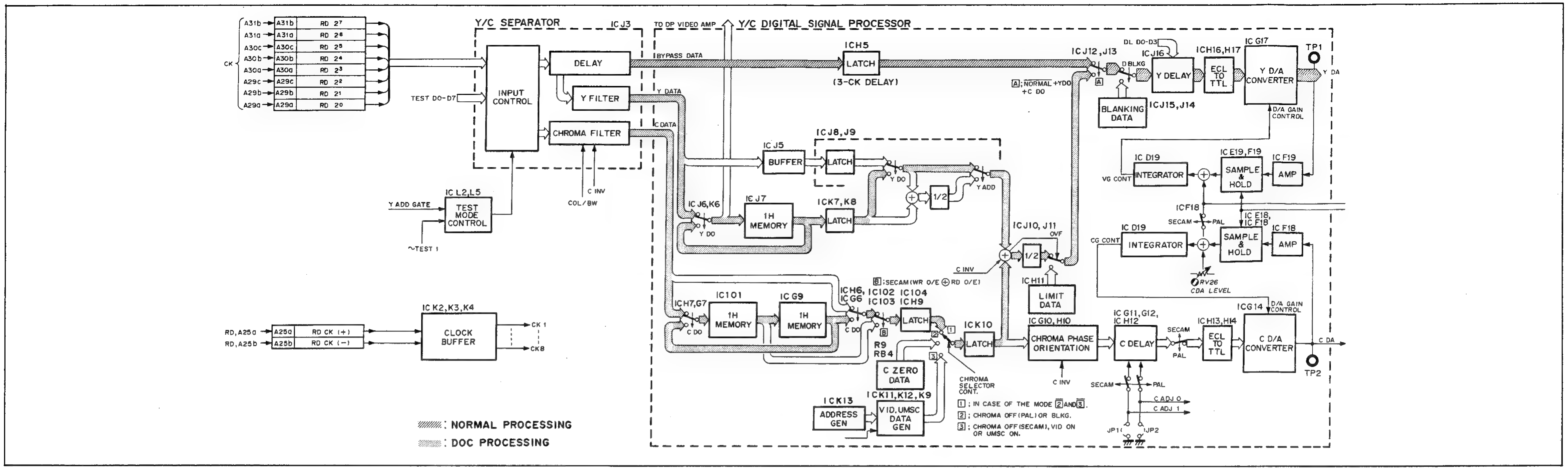


Fig. 4-4-63. [NORMAL · CHROMA ON] Processing (PR-92)

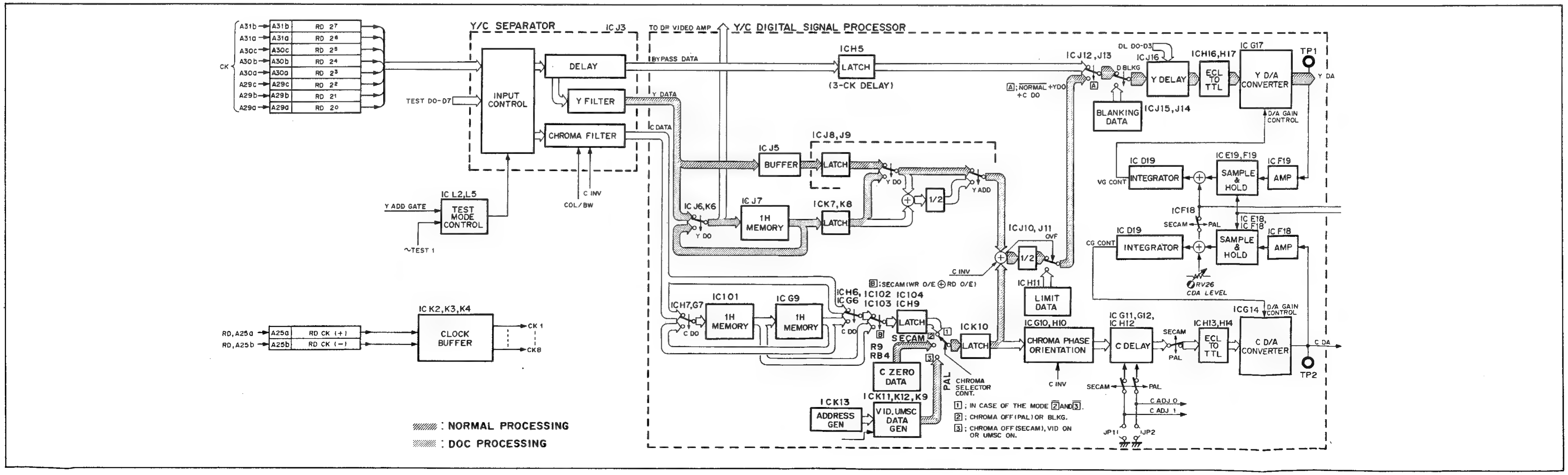


Fig. 4-4-64. [NORMAL · CHROMA OFF] Processing (PR-92)

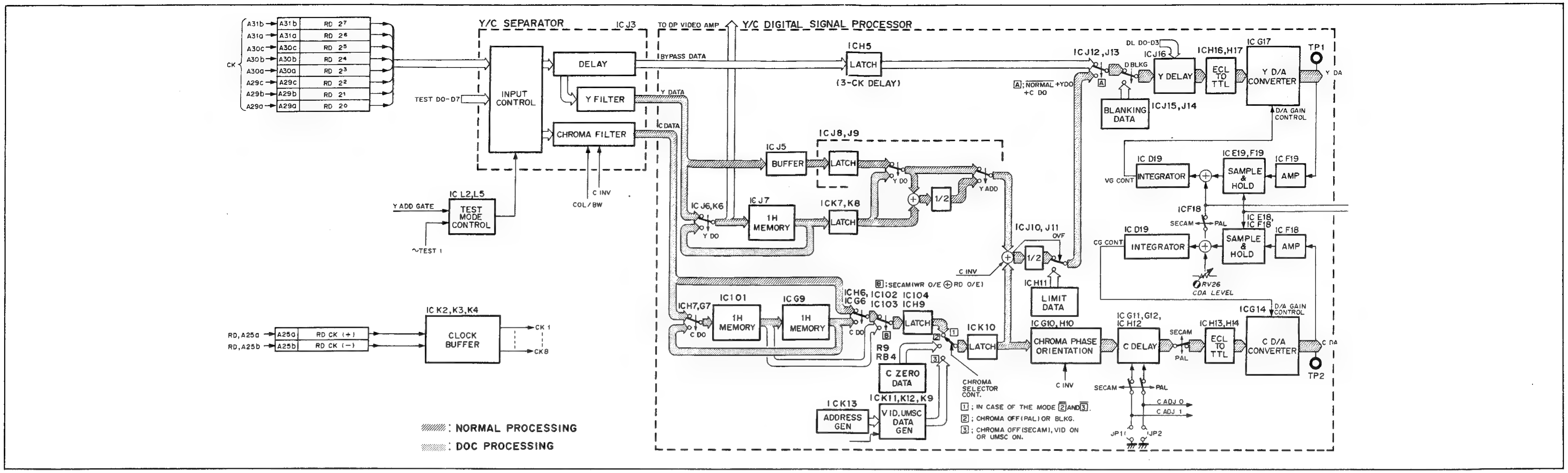


Fig. 4-4-65. [PAL・BIDIREX・CHROMA ON・Y ADD ON] Processing (PR-92)

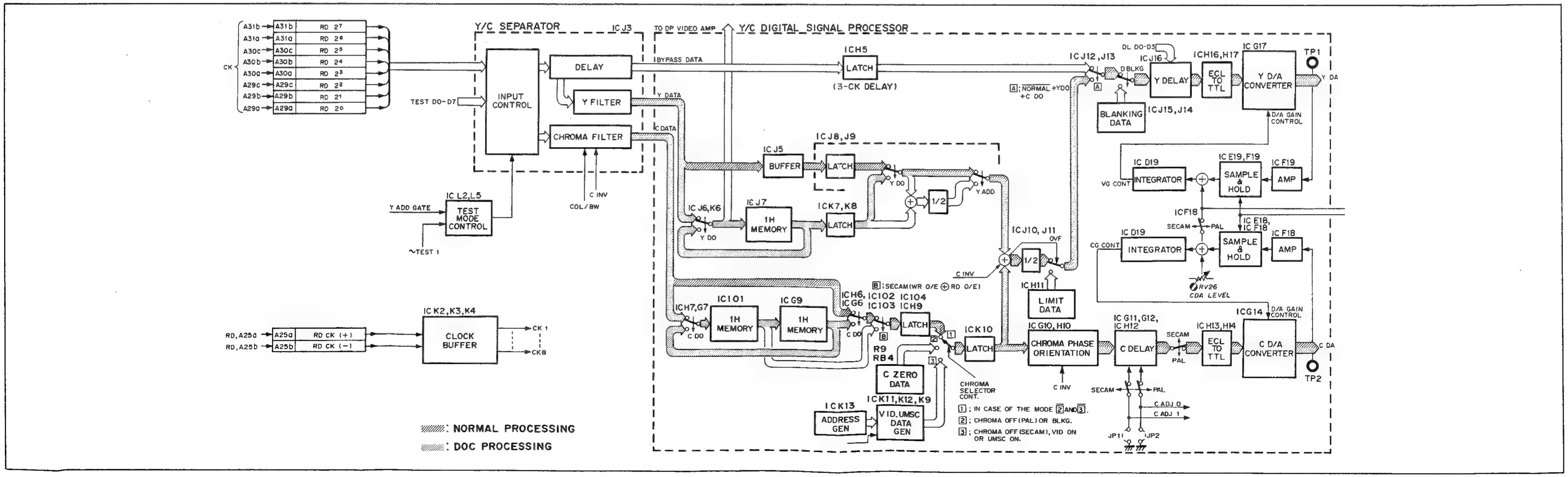


Fig. 4-4-66. [PAL・BIDIREX・CHROMA ON・Y ADD OFF] Processing (PR-92)

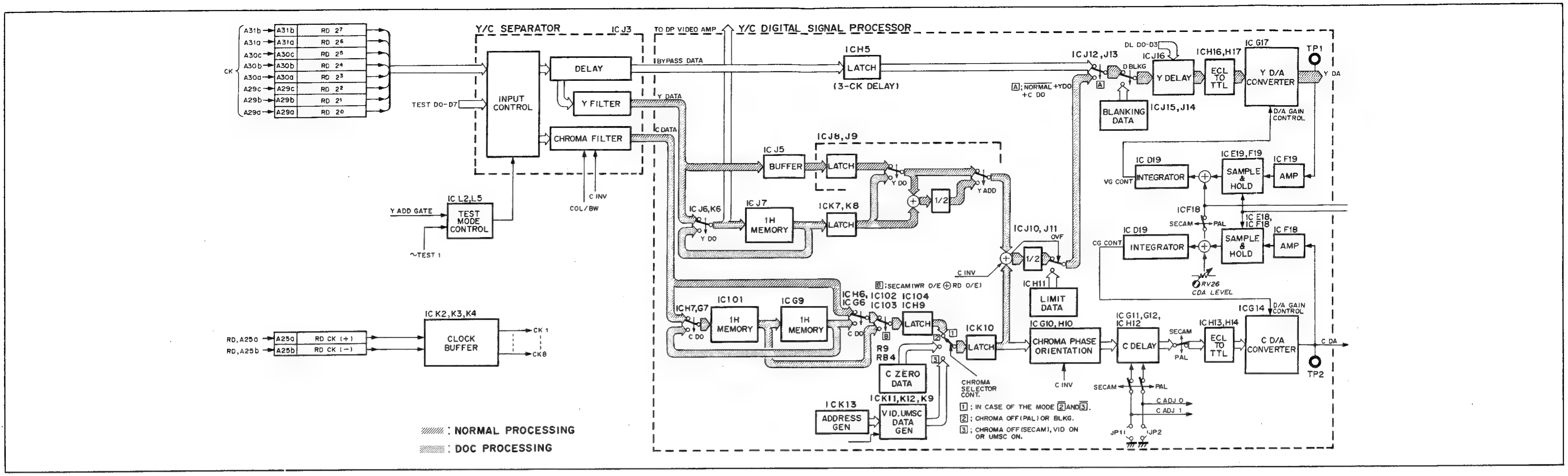


Fig. 4-4-67. [SECAM · BIDIREX · CHROMA ON · Y ADD ON] Processing (PR-92)

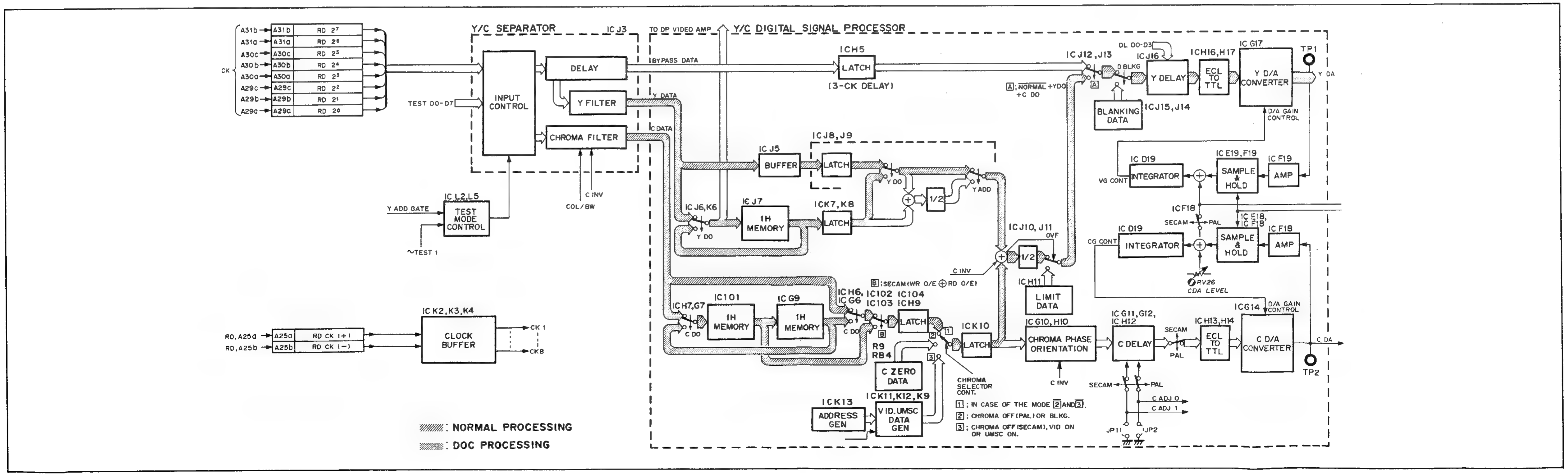


Fig. 4-4-68. [SECAM · BIDIREX · CHROMA ON · Y ADD OFF] Processing (PR-92)

4-4-11. Digital Processor/BKH-3060 (PR-98 Board)

The Y signal processing section is responsible for compensating for the dropouts in the Y components and providing field interpolation for the Y components.
The description for the chroma signal processing in the PR-98 board is omitted, because it is similar to that in the PR-92 board.

(1) Y/C separator (PR-98 board)

The 8-bit digital composite video signal which has been supplied from the CK board is first latched by ICJ2 and it is then applied to Y/C separator ICJ3 (CX23082) where the Y and chroma components are separated. The composite signal which has not been separated is also output from ICJ3 and sent to the bypass circuit. It is also possible to supply the test pattern data which are output from I/O expander ICM3 (CXD1095Q).
The test pattern mode, chroma signal inhibition and chroma signal inversion are controlled by the TEST 1 signal, COL/BW signal and WNI 1 signal, respectively, which are applied to Y/C separator ICJ3.
The composite video signal output to the bypass line is delayed so as to correspond with the delay in the other processing systems. A delay equivalent to 4 clocks are provided by ICH4, 1H each by ICH5, H6, and 1 clock each by ICG6 and H18. This makes a total delay of 2H+6 clocks.

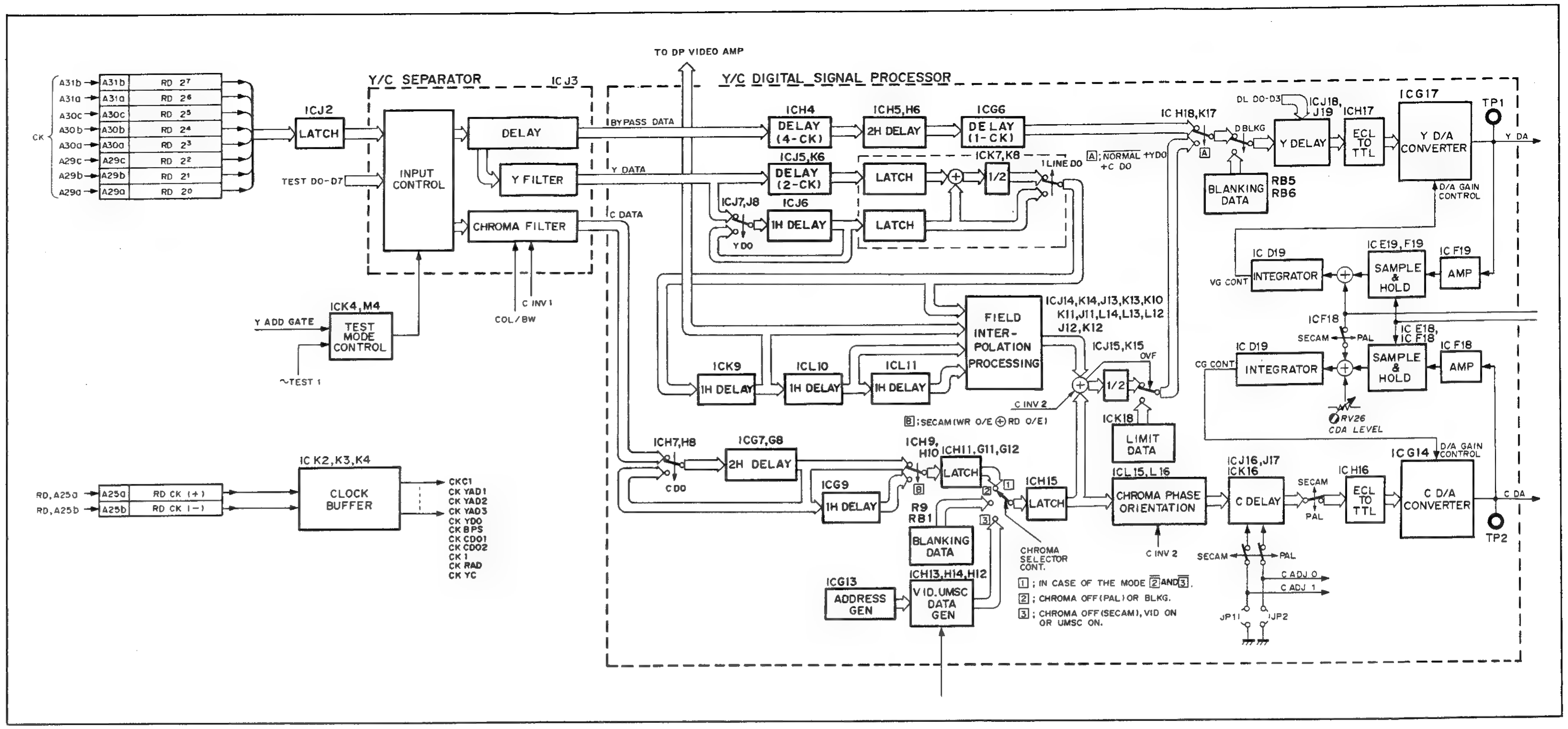
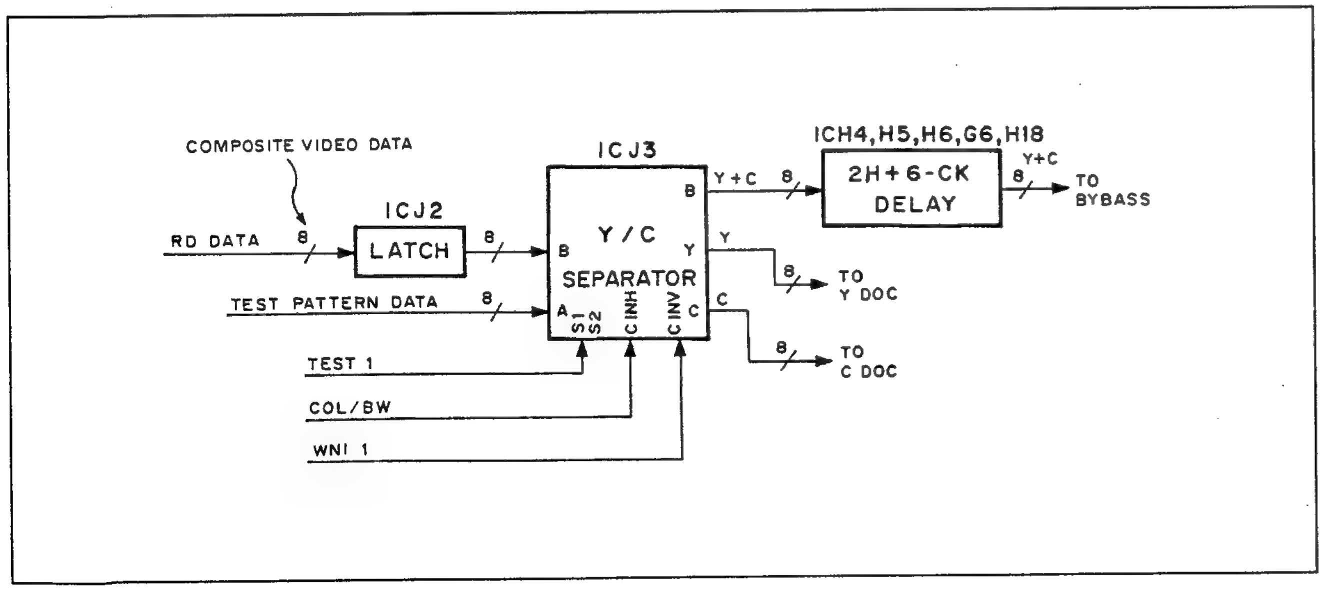


Fig. 4-4-69. Digital Processing Circuit/BKH-3060(PR-98)



Fi. 4-4-70. Y/C Separator and Bypass Line (PR-98)

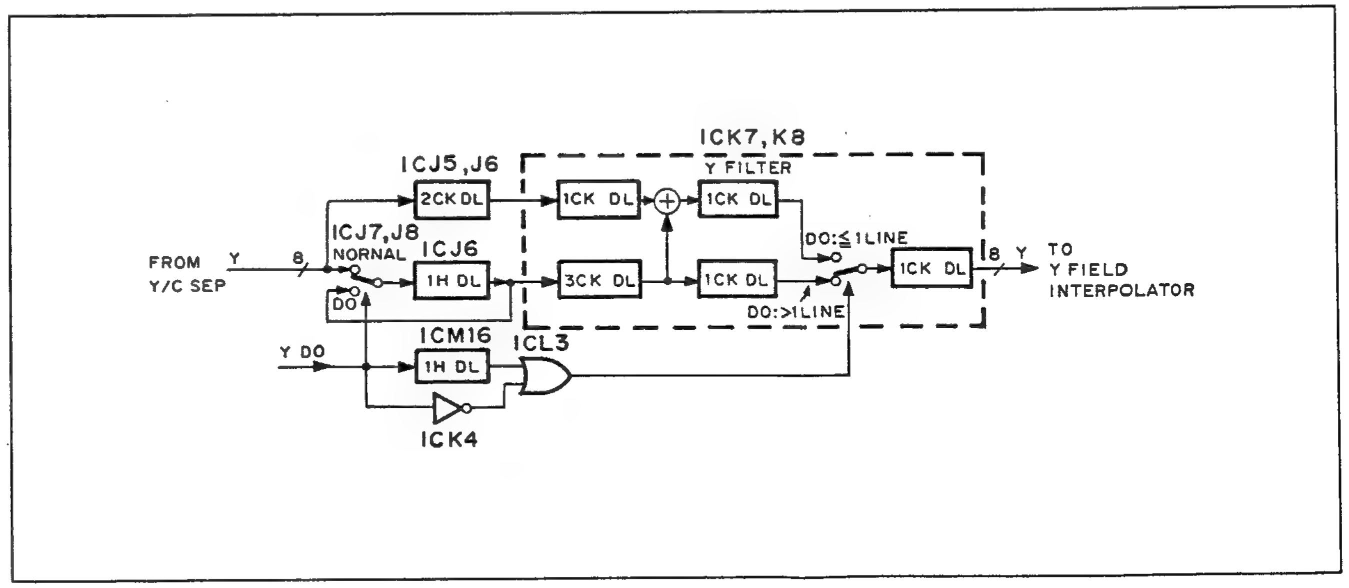


Fig. 4-4-71. Y DOC (PR-98)

(2) Y signal digital processor (PR-98 board)

(a) Y signal dropout compensator (PR-98 board)
This circuit compensates for the dropouts in the Y signal. When a dropout or dropouts have been detected, the separated Y signal is processed as follows. Dropouts are detected on the CK board and supplied to the PR board as the Y DO and C DO signals.
When dropouts occur, the Y signal which has been 1H delayed by ICJ6 is returned to selector ICJ7 and J8 so that it is further 1H delayed by ICJ6. The resulting 2H delayed Y signal is added by line adder ICK7 and K8 to the Y signal whose delay has been adjusted by ICJ5 and J6. As a result, the dropouts are compensated for.
The Y DO detection signal is applied to the select pin of selector ICJ7 and J8, while it is inverted by ICK4 and OR-ed with the signal which has been 1H delayed by ICM16. The OR-ed signal is supplied to the select pin of the line adder. When dropouts have occurred over a multiple number of lines, the interim lines and final line are respectively processed as follows in accordance with the processing of this detection signal. The interim dropout lines are replaced by the Y signal of the line before that in which the dropout has occurred. The final dropout line is replaced by the signal which is produced by adding the Y signal of the line before that in which the dropout has occurred to the normally returned line Y signal.
When no dropouts are detected, the Y signal is delayed by 1H+5 clocks and it is then output.

(b) Y field interpolator (PR-98 board)
Using the reference signal and playback signal field coincident/non-coincident information, this circuit conducts field interpolation from the Y signals equivalent to 4 lines and it improves the picture quality in the DT playback and STILL modes.
The Y signal is delayed 1H each by ICK9, L10 and L11. The factors corresponding to the amounts of the delay are applied by ROMs ICK10, J11, K11, L14, L13 and L12 to the delayed Y signal and, in accordance with the combinations shown in the figure, they are added by line adders ICJ12/K12, J13/K13 and J14/K14. As a result, field interpolation is conducted using the data of 4 lines each in all.
The Y ROM A9 and Y ROM A8 signals which switch the factors of the ROMs represent information relating to whether the reference signal and playback signal fields coincide or not and whether the fields should be interpolated.
[Y ROM A8] 0: Field coincident 1: Field non-coincident
[Y ROM A9] 0: No interpolation 1: Interpolation

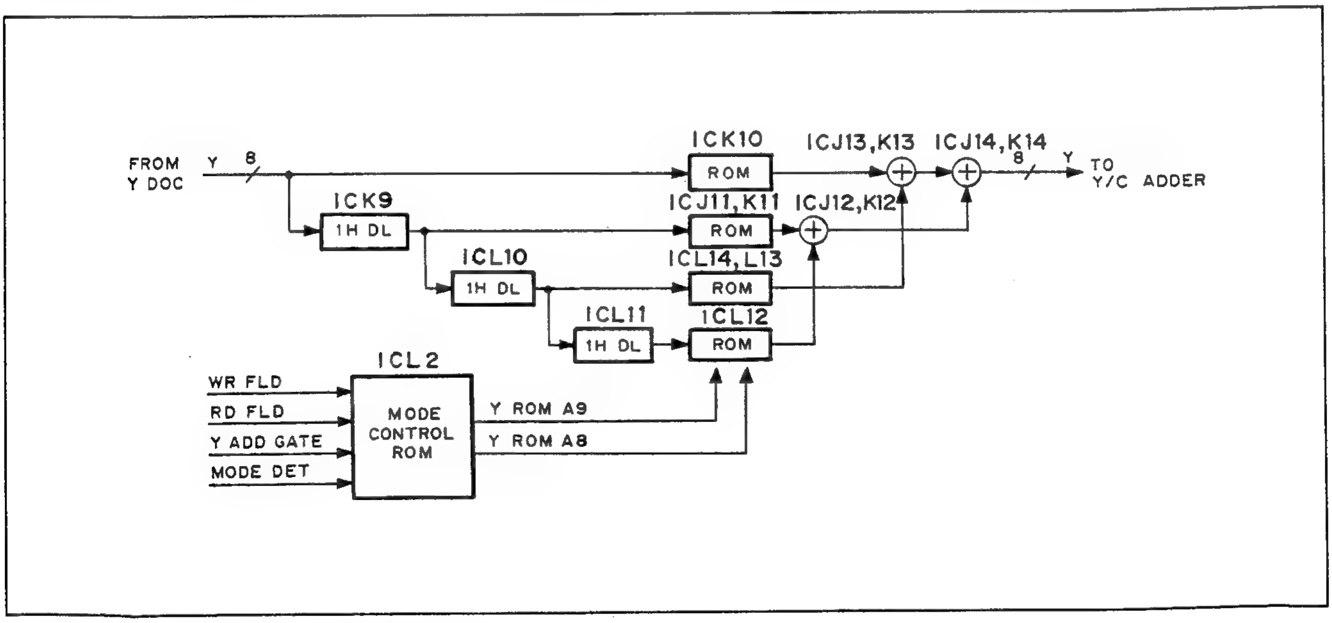


Fig. 4-4-72. Y Field Interpolator (PR-98)

4-4-12. Analog Processor (PR-98/92 Board)

The anfalog processor block contains a processor circuit, which controls the video level, chroma level and black level (PAL signals only) with the Y D/A converter and also which adds both the reference sync signal and the reference burst signal (PAL signal only) to these video signals.
In the FAST BIDIREX mode over ±8 times normal tape speed, the video signals in both the PAL and SECAM mode are restricted to a 2.5MHz band, the chroma signal is cut out and a monochrome signal is output.
The C phase corrector is a circuit which processes the chroma signals in the PAL BIDIREX mode.

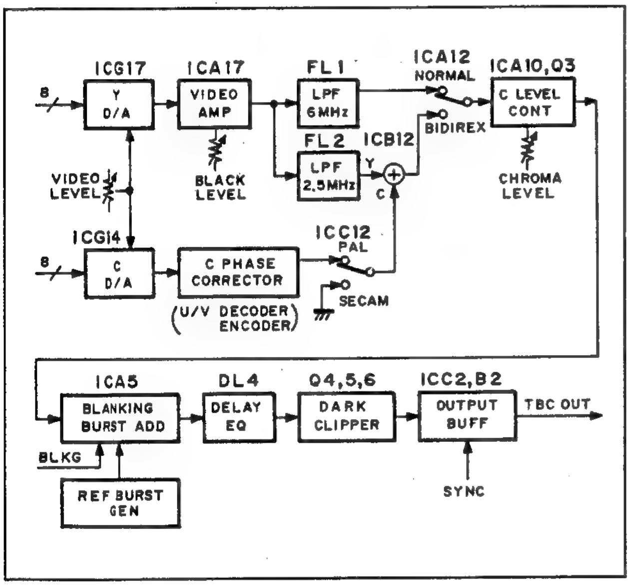


Fig. 4-4-73. Outline of Analog Processor (PR-98/92)

(1) D/A converter (PR-98/92 board)

The Y D/A converter converts the digital output of the digital processor circuit into an analog signal. The input of this converter is delayed by ICJ18 and J19 (or ICJ16 on the PR-92 board) in clock pulse units equivalent to the time required for chroma signal processing. The Y D/A output signal is a composite signal in both the PAL and SECAM modes.
The C D/A converter provides D/A conversion for only the Y/C separated chroma signal. The input of this converter is delayed in clock pulse units by ICK16 and J17 (ICG11 and H12) in order to align the Y/C delay of the PAL BIDIREX playback signal. The phase of the C D/A output signal is compensated in the PAL DT/BIDIREX playback mode.
Both output levels of the Y D/A and C D/A converters are adjusted by the VIDEO LEVEL control. The adjustment is made in order to adjust the video levels of TBC OUT and TBC NON COMP.

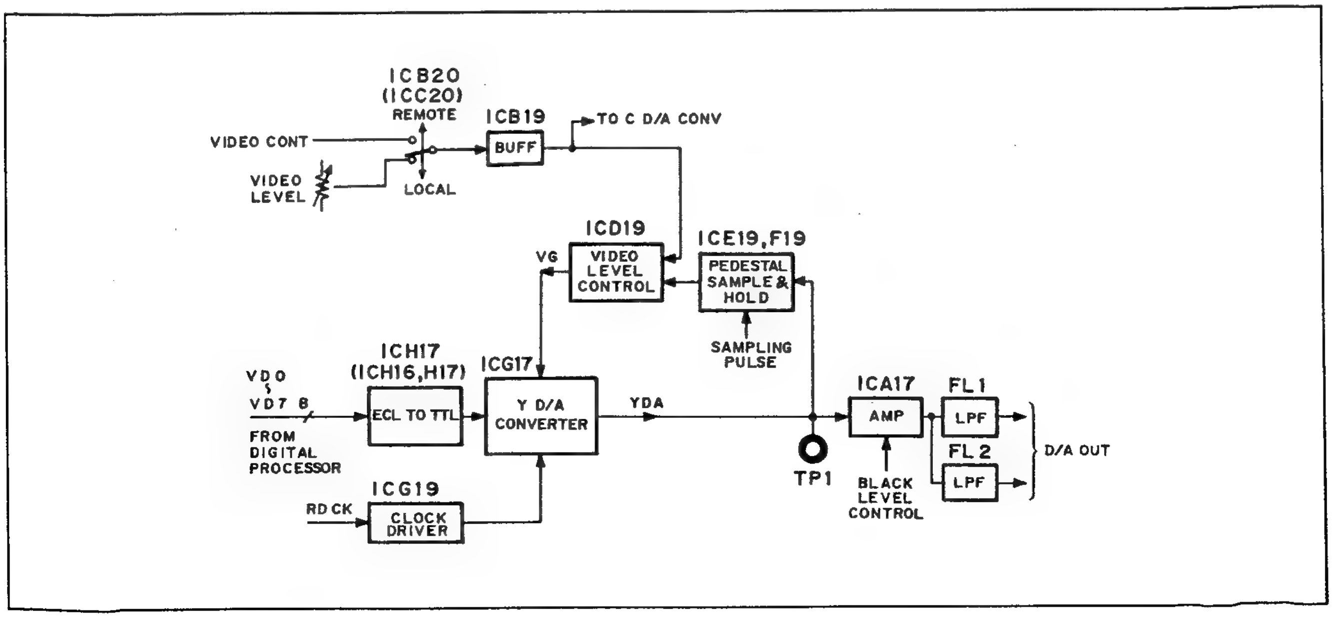


Fig. 4-4-74. Y D/A Converter (PR-98/92 board)

(2) LPF and mode switching circuit (PR-98/92 board)

In the normal playback mode, the frequency response of the Y D/A output signal is first compensated by ICA17, the signal is then interpolated by FL1 (6 MHz low-passfilter) and sent to the ICA12 switcher. Mode switching circuit ICA12 is set to NORMAL in the following modes ; in all other modes, it is set to BIDIREX.

PAL • COLOR • PLAY STATUS

+ (SECAM+B&W) • $\overline{\text{FAST BIDIREX}}$

In the PAL BIDIREX playback mode, the band of only the Y signal of the video signal output from ICA17 is restricted by FL2 (2.5 MHz low-pass filter), the chroma signal whose color field sequence has been corrected at the input side of ICB12 is then added to the resulting signal, and the signal is then sent to the ICA12 switcher.

In the FAST BIDIREX mode, the Y signal whose bandwidth is restricted by FL2 is sent to ICA12 without chroma signal adding,because the chroma signal is prohibited in the C phase corrector circuit.

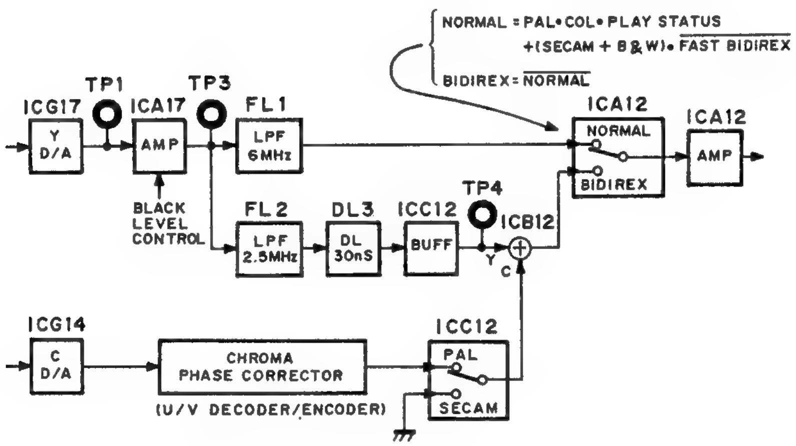


Fig. 4-4-75. LPF and Mode Switching Circuit (PR-98/92)

(3) Chroma level and black level control circuit (PR-98/92 board)

The chroma level control circuit is composed of delay line DL2, linear multiplier ICA10 and chroma component adder Q3. The amount of delay in the delay line is 1/2 fsc sec. This means that when the video signal which passes through the delay line is subtracted from the video signal containing the reflection component of the delay line, only the chroma components will be output from ICA10. The level of these chroma components depends on the voltage applied to pin 8/YIN (−) of ICA10. Consequently, when the ICA10 output is added to the video signal (FL3 output), the result will be a video signal whose chroma level has been adjusted by the CHROMA CONT voltage. Low-pass filter FL3 functions as a delay line for aligning the timing.
When changing the shorting plug position from JP10 to JP9, the chroma level control can be possible in the SECAM mode.
Fig. 4-4-77 shows the frequency response of the chroma level control circuit.
The black level control circuit comprises a feedback loop stretching from Q3 to ICA17. ICB18 controls the offset of ICA17 so that the pedestal level of the Q3 output will follow the SET UP CONT voltage applied to ICB18.

The respective remote/local control modes are selected using the "I83. CHROMA LEVEL" and "I82. BLACK LEVEL" initial set-up menus.
In the SECAM mode, the black level control voltage is switched off by ICD18 and black level control does not function.

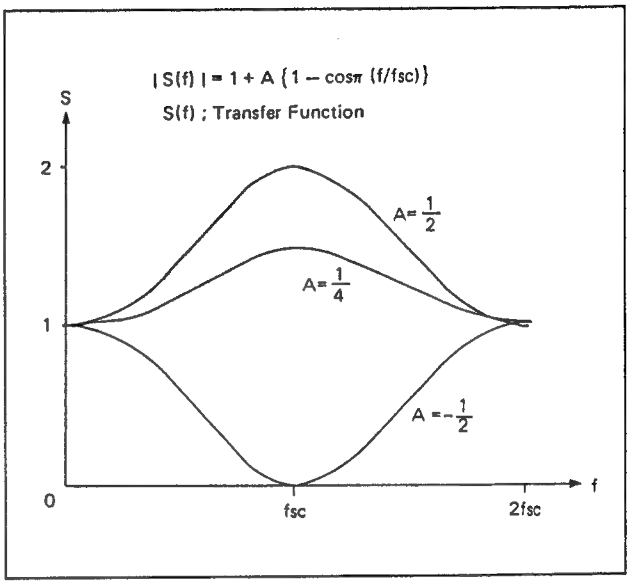


Fig. 4-4-77. Frequency Response of Chroma Level Control Circuit

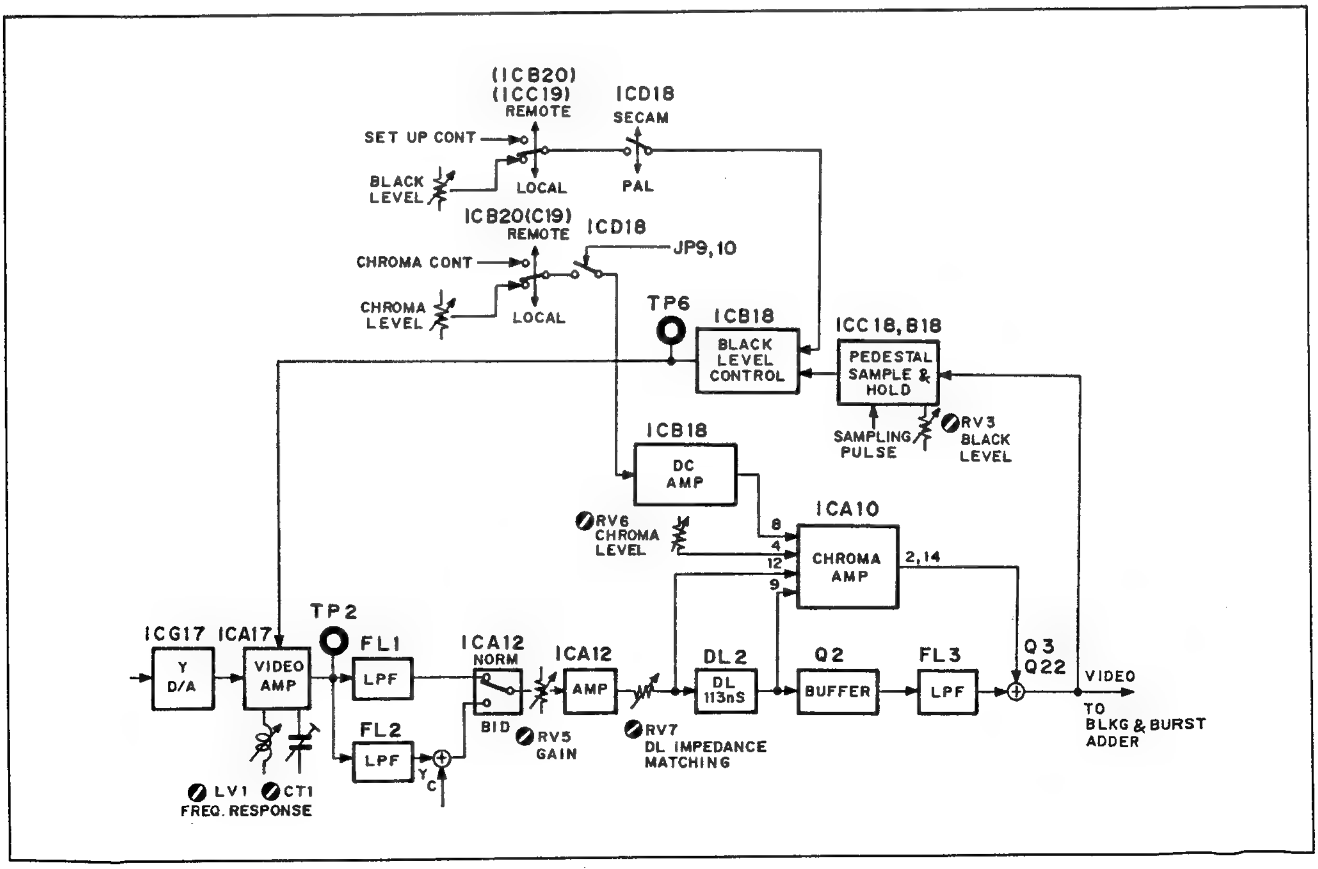


Fig. 4-4-76. Chroma Level and Black Level Control Circuit (PR-98/92)

(4) Blanking/burst adder, Y/C delay adjustment and dark clipper (PR-98/92 board)

The video signal, whose chroma level and set-up level have been controlled, is now supplied to switcher ICA5. The reference burst signal is supplied to the other input pin of the switchers. The reference burst signal is added at the same time as blanking is applied by selecting these switchers using the blanking signal.
The output of the blanking/burst adder circuit is fed to the Y/C delay adjusting circuit consisting of S1, S2 and DL4. The Y/C delay is adjusted by using group delay of the delay equalizer (DL4) so that the adjustment of 7 nsec per one step accuracy can be carried out by the selection of S1 and S2.
However, when Y/C adjustment will be performed using this circuit, the burst phase also varies, consequently, it is necessary to perform the SC/H phase adjustment again.
The dark clipper is a circuit consisting of Q4, 5 and 6 as well as bandpass filter BPF1. The video signal, to which the reference burst signal has been added, is applied to one base of Q4 and to the other base is applied only the chroma components which have passed through the bandpass filter. This means that the signal clipped below the pedestal level and excluding the chroma components is output to the emitter of Q4. Q5 and 6 function to stabilize the operating point of Q4, enabling the Q4 gain to be compensated during the clipping operation.
An example of how this circuit operates is shown in Fig. 4-4-79.

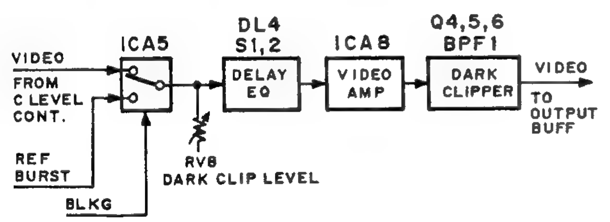


Fig. 4-4-78. Blanking/Burst Adder, Y/C Delay Adj. and Dark Clipper (PR-98/92)

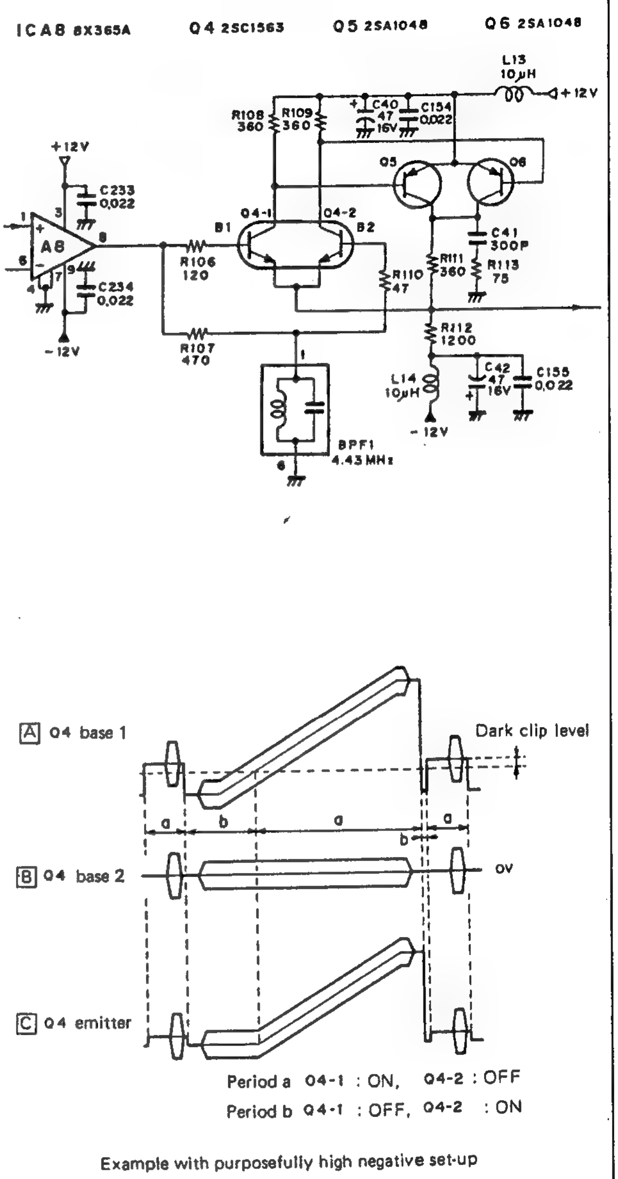


Fig. 4-4-79. Dark Clipper Operation (PR-98/92)

(5) Reference burst generator (PR-98/92 board)

The reference burst signal is generated from the RD Fsc signal which is gated by the burst gate signal created from the BURST FLAG signal. After its band has been limited by the bandpass filter, it becomes the reference burst signal.
Whether or not the burst signal is to be added to the VTR output depends on the setting of the "I89. BURST" initial set-up menu.
In the SECAM mode, the BF signal input is prohibited and the reference burst signal is not output.

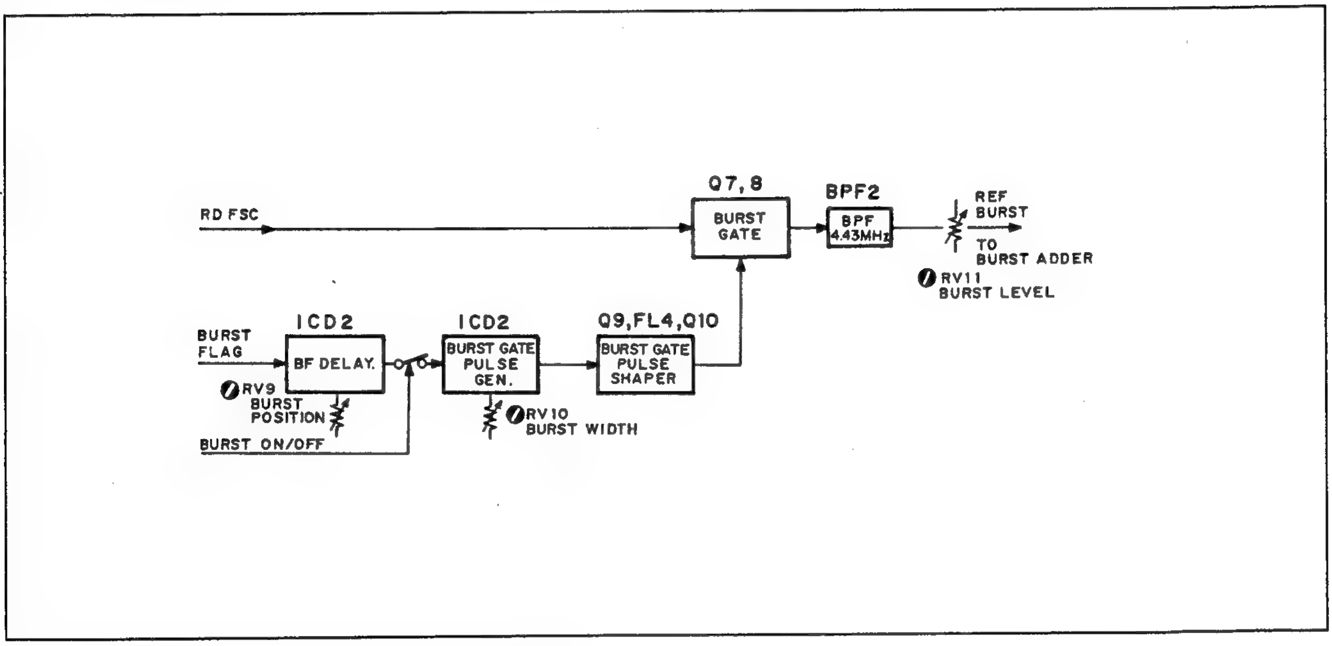


Fig. 4-4-80. Reference Burst Generator (PR-98/92)

(6) Output video buffer and sync adder (PR-98/92 board)

ICC2 and B2 are output buffers. At the output side of each buffer is added the sync signal which is generated from the TBC SYNC signal. The amplitude of the TBC SYNC signal which is applied to Q11 is adjusted by RV12, the waveform of the signal is then shaped by low-pass filter FL5, and then the signal is added to the respective buffer outputs by Q12, 13 and 14. The switching operation of Q13 and Q14 is turned on or off by the "S81. COMP/NON COMP" select menu, which enables the COMP or NON COMP mode for VIDEO OUT 3 to be selected.

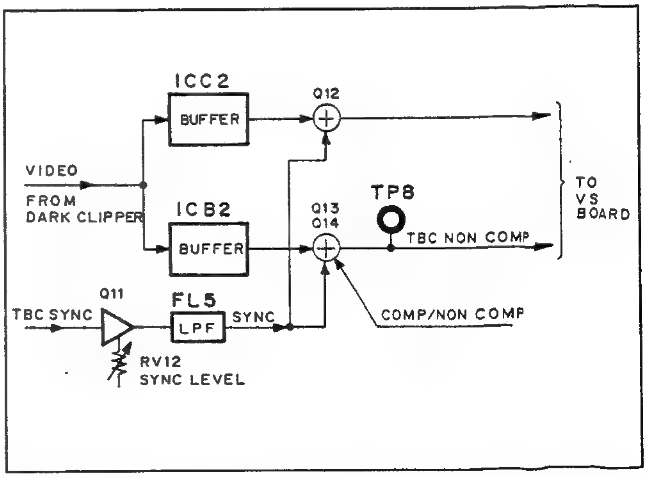


Fig. 4-4-81. Output Video Buffer and Sync Adder (PR-98/92)

(7) **Chroma signal phase corrector (PR-98/92 board) (PAL U/V decoder/encoder)**

The chroma signal phase corrector circuit is a circuit which processes the chroma signals in the PAL signal BIDIREX mode. Among other circuits, it consists of the PAL U/V separator circuit, decoder, encoder, and decode/encode carrier generator.
In the PAL BIDIREX mode, the phase of the chroma signal sent from the CK-27 board dose not match that of the reference signal.
In order to bring the chroma signal into alignment with the reference signal, the chroma signal phase corrector circuit generates a decode carrier synchronized to the C D/A output signal, and that decode carrier is used to decode the C D/A output signal. Next, the decoded signal is encoded using a carrier synchronized to the reference signal.
In the FAST BIDIREX mode, the encode carrier is not generated and the chroma signal is set off.

(8) **U/V separator (PR-98/92 board)**

BPF3 serves to filter out only the chroma components from the C D/A output signal. The level of the BPF3 output is adjusted by RV13 so that the level of the signal input into the decoder circuit is made uniform, and then its phase is adjusted by RV14 so that it coincides with the decode carrier in the DT mode.
The U components are obtained by adding the 1H delay signal delayed by DL1 and the signal which is not 1H delayed (ICD13 output) in the U/V separator circuit, and the V components are obtained by subtracting these two signals in the same circuit.

The phase inverter circuit composed of Q17 and ICD13 is designed to invert the chroma phase so that the U/V separation can be conducted properly even when the main memory output has jumped by 2H due to an excessive WINDOW in the main memory.

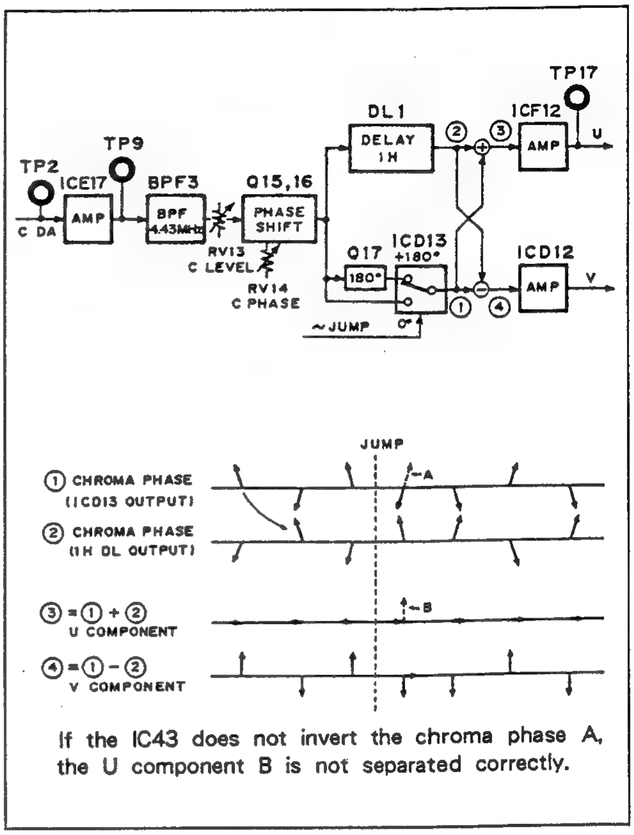


Fig. 4-4-83. U/V Separator (PR-98/92)

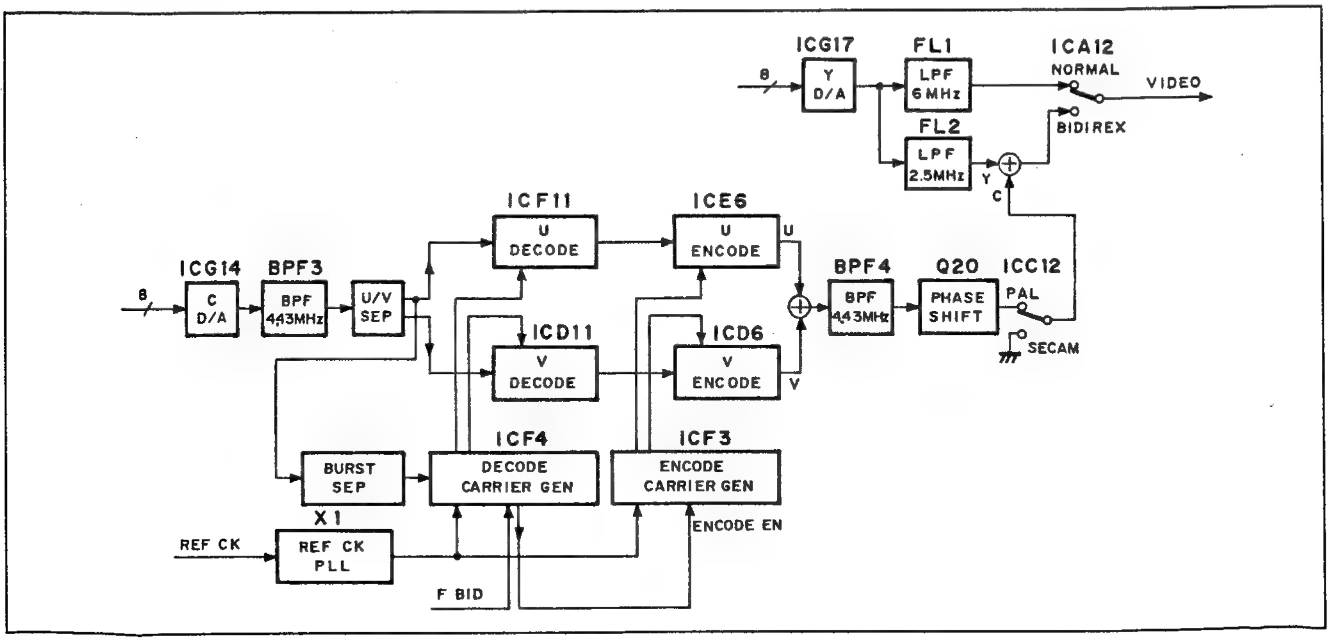


Fig. 4-4-82. Chroma Phase Corrector (PR-98/92) (PAL U/V Decoder/Encoder)

(9) U/V decoder (PR-98/92 board)

The U/V separated signals are decoded by the decode carriers in ICF11 and ICD11 respectively, the signals pass through the FL7 and FL6 low-pass filters, and base band chroma signals are obtained.
The decoded chroma signal is clamped to 0V, with the digital blanking section serving as the reference. ICE7 and ICE9 make up the clamp circuit for the V components while ICF7 and ICE9 make up the clamp circuit for the U components.

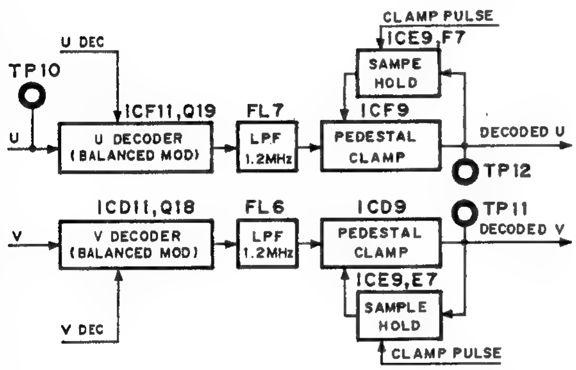


Fig. 4-4-84. U/V Decoder (PR-98/92)

(10) REF CK PLL (PR-98/92 board)

With the REF CK signal sent from RD-7 board serving as the reference, the REF CK PLL circuit provides an Fsc clock or 4Fsc clock signal which serves as the reference for the encode or decode carrier.
REF CK is the Fsc clock signal which is not subject to velocity error phase modulation but which is subjected to SC phase and Burst-Chroma phase control. The Y/C delay in the BIDIREX mode is adjusted by varying the amount of delay in the chroma signal system in single 4Fsc clock units by means of JP1 and JP2. This adjustment has the effect of varying the CDA signal phase in 90° steps, and ICH2 is a circuit for varying the phase reference of the decode carrier in accordance with these phase fluctuations.

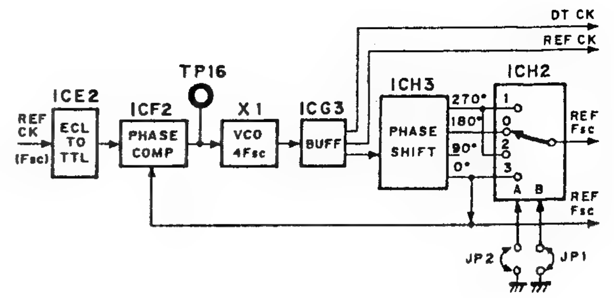


Fig. 4-4-85. REF CK PLL (PR-98/92)

(11) Decode carrier generator (PR-98/92 board)

The decode carrier is provided by ICF4 but the way in which it is provided differs depending on whether the mode is SLOW BIDIREX or DT.

SLOW BIDIREX mode

In the SLOW BIDIREX mode, the playback burst signal is written into the main memory. The decode carrier is provided using this burst signal.
The U/V separated U component signal passes through Q21, it is turned into a binary value by ICF5 and then input into ICF4 as the WSC signal. Using the WSC signal and clamp pulse (H SYNC), one cycle of the U component in the burst signal is taken out by ICF4.
This is called the RESET signal. The shuttle decode clock generator composed of ICE3 employs this RESET signal as the voltage-controlled oscillator (VCO) reset pulse, and the output phase of this VCO is locked to the phase of the U component in the burst signal. The frequency of the VCO output (4Fsc) is divided down by 4 in ICF4 and the U-axis decode carrier UDEC is created as a result.
ICG4 functions to control the phase in 90° steps when the frequency is divided down by 4, and the V-axis decode carrier is also produced by this control. The phase of the V-axis decode carrier is advanced by 90° over the phase of the U-axis decode carrier.
The frequency of the VCO in the shuttle decode clock generator is stabilized by first comparing the phases of the UDEC and REF FSC signals during the VD period by ICF4, passing the resulting error voltage through ICD5 to the D10 varicap diode and then locking the oscillation frequency of the VCO to a value equivalent to four times the REF FSC frequency.

DT mode

As with the normal playback signal, the DT playback signal is subject to the time base correction processing. Consequently, the video signal of the D/A output is time-base-corrected at a high degree of

precision even in the DT mode.
However, since any field is played back with DT playback, the color field sequence of the playback signal becomes discontinuous, the phase of the D/A output chroma signal is shifted by 90° with respect to the phase of the reference signal, and the V-axis swing sequence is reversed.
As a result, the decode carrier in the DT mode is produced not by a method that uses the playback burst signal as in the SLOW BIDIREX mode but by a method that modulates the phase of the REF FSC signal, which is the REFERENCE SC signal, in 90° steps in accordance with the state of the D/A output chroma phase.
The state of this phase is identified by comparing the W O/E and W N/I signals which indicate O/E and N/I of the playback signals with the R O/E and R N/I signals which indicate O/E and N/I of the reference signal. This comparison and the results are sent to the PR board as the OEDC and NIDC signals.
Based on these OEDC and NIDC signals, the phase control signals UOE, UNI, VOE and VNI for producing the U-axis and V-axis decode carriers are produced themselves by the O/E and N/I decoders composed of ICL4 and K5 (or ICL15 and M11 on the PR-92 board). These signals are sent to ICF4 for phase modulation with the REF Fsc signal produced by the REF CK PLL circuit. The REF Fsc signal whose phase is modulated by the UOE and UNI signals becomes the U-axis decode carrier while the REF FSC signal whose phase is modulated by the VOE and VNI signals becomes the V-axis decode carrier.

(12) Encoder (PR-98/92 board)

The decoded U and V components are first encoded by ICE6 and ICD6 and then added together to form the chroma signal whose color sequence is made to coincide with that of the reference video signal. The bandwidth of the added chroma signal is restricted by the BPF4 bandpass filter and it then enters the chroma phase shifter. The chroma phase shifter is a circuit for adjusting the chroma phase of the Burst-Chroma phase, and RV19 is used for the actual phase adjustment.
The chroma phase shifter output is added to the Y signal via ICC12. O/E detector ICD7 is a voltage comparator for detecting the direction (O/E) of the V axis in the shuttle mode.

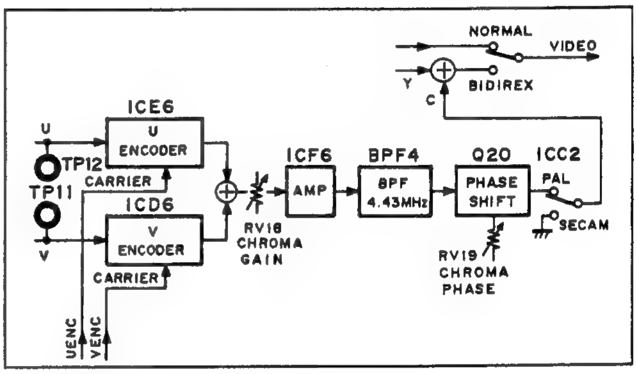


Fig. 4-4-87. Encoder (PR-98/92)

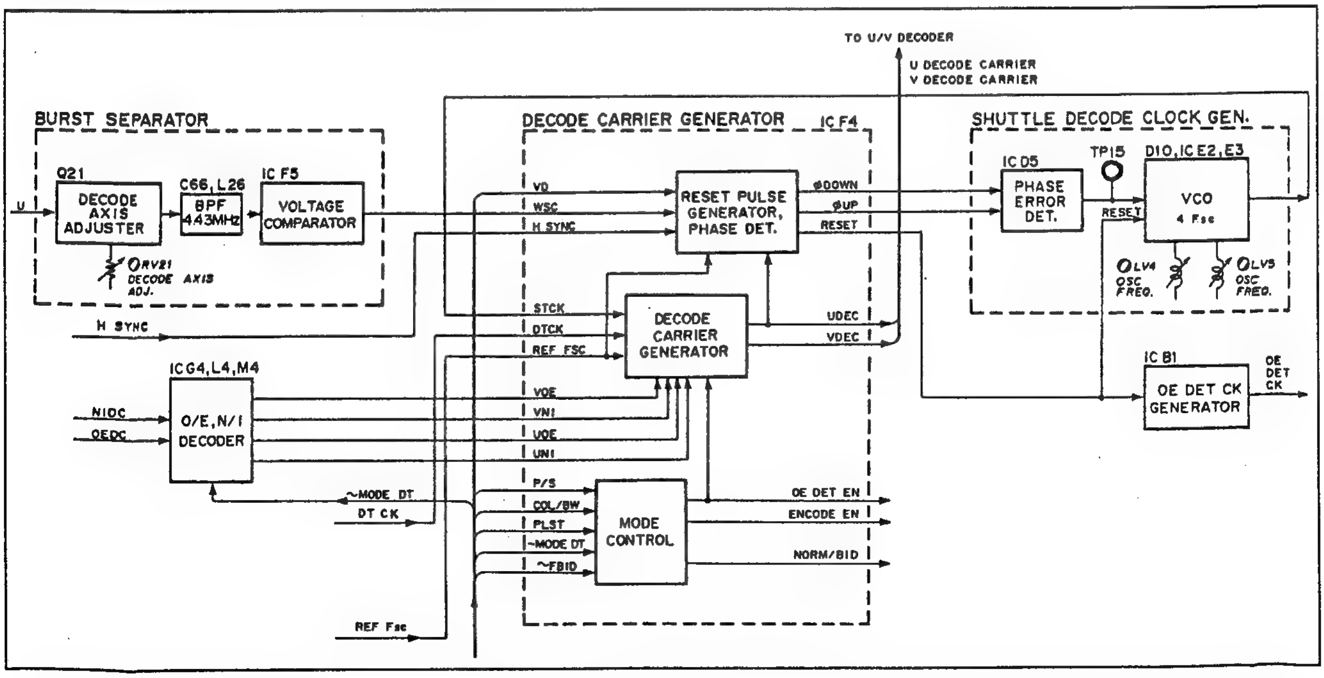


Fig. 4-4-86. Decode Carrier Generator (PR-98/92)

(13) Encode carrier generator (PR-98/92 board)

The encode carrier is produced by ICF3 using the REF Fsc signal as the reference, but the way in which it is produced differs depending on whether the mode is SLOW BIDIREX or DT.
The I/O3 and I/O4 signals of ICF3 are the mode switching signals of the encode carrier. The I/O3 signal is for switching between the DT and SLOW BIDIREX modes.
In the PAL•COLOR•SLOW BIDIREX mode, the SLOW BIDIREX encode carrier is produced ; in the other modes the DT encode carrier is produced.
The I/O4 signal is for stopping the encode carrier output. In the PAL • COLOR • (SLOW BIDIREX+DT) mode, the encode carrier is output; in any other mode, it is not output.

DT mode

In the DT mode, U-axis encode carrier UENC is produced by delaying the REF Fsc signal phase by 90° . V-axis encode carrier VENC is produced in-phase with the REF Fsc signal.
O/E conversion of the chroma phase in the DT mode is performed by inverting the phase of the V-axis decode carrier at the decode side. Consequently, the V-axis encode carrier phase is constant at all times.

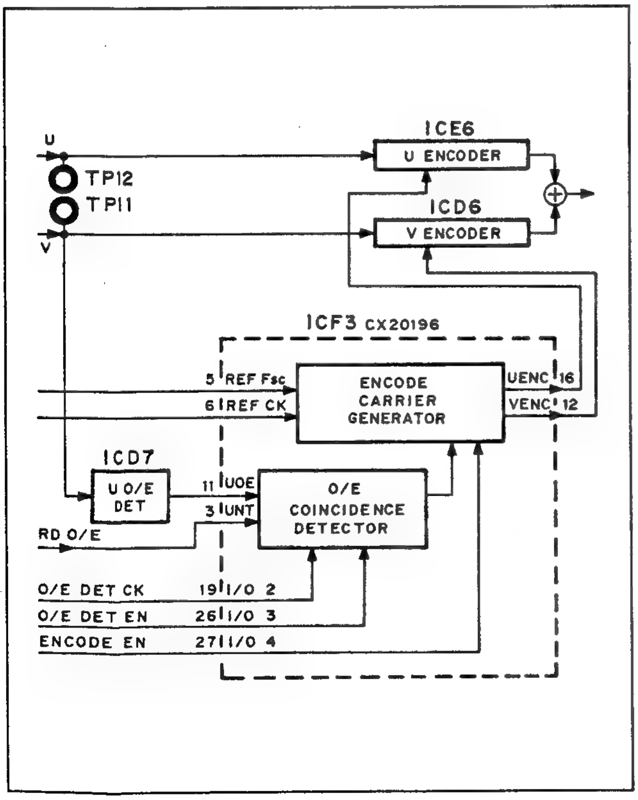


Fig. 4-4-88. Encode Carrier Generator (PR-98/92)

SLOW BIDIREX mode

In the SLOW BIDIREX mode, U-axis encode carrier UENC is produced in the same way as in the DT mode.
V-axis encode carrier VENC is produced in-phase with the REF Fsc signal when the UOE signal detected by the ICD7 voltage comparator coincides with the UNI signal which is the O/E information of the reference signal. If the signal does not coincide, it is produced by inverting the REF Fsc signal phase. By inverting the phase, the color field sequence of the playback signal is made to coincide with that of the reference video signal.
Fig. 4-4-89 gives an example of O/E conversion in the SLOW BIDIREX mode.

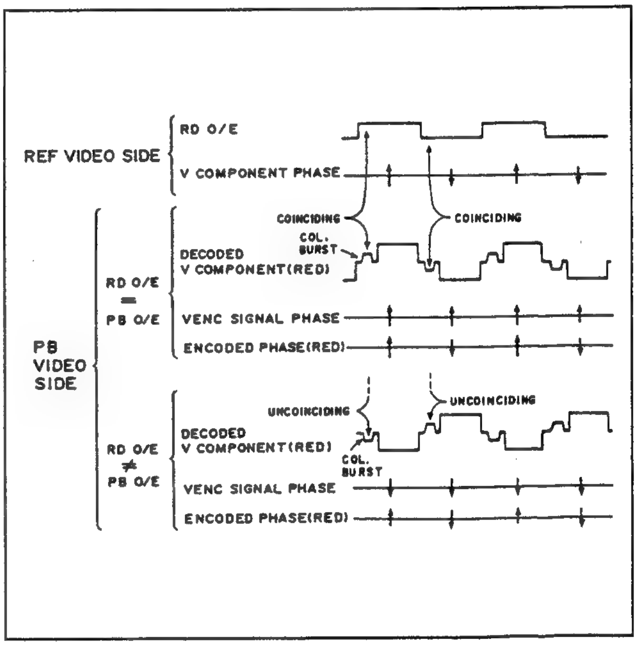


Fig 4-4-89. O/E Conversion : SLOW BIDIREX Mode

4-5. DT SYSTEM

4-5-1. Outline of DT System (RD-6/RD-7 Board)

Note 1 :
The DT system of BVH-3000/3100 employs the RD-6 board for NTSC model and the RD-7 board for PS model. The reference numbers that are given to respective parts and components are different in the RD-6 board and in the RD-7 board. Therefore, the reference numbers for the RD-6 board/NTSC model are shown first and those for the RD-7 board/PS model are shown in parentheses.

Note 2 :
RD-6 board and RD-7 board have currently three types respectively, having the part numbers' last two digits of "-11", "-12" and "-13". The same circuit components sometimes have the different reference numbers in the "-11/-12" and "-13". In order to avoid confusion, the reference numbers for the RD-6 board and the RD-7 board ending by "-13", are omitted in the subsequent description.

Note 3 :
The circuit compositions of the "-11" version and the "-12" version of the RD-6 board and the RD-7 board, are mostly same. The "-13" version has the following additional functions that are not found in the "-11, -12" versions.
- Ringing amount detector
- Wobbling phase shifter
- Filter during DT OFF period
- Feedback gain suppressor during INTEG OFF period

The DT system of BVH-3000/3100 has the most distinguished point in its microprocessor system where most of DT system controls are performed by the microprocessor. The changes in the DT head characteristics and the changes in tape properties are automatically compensated by the microprocessor. Amount of jump that has been frequently adjusted in the conventional type, becomes automatic control and the optimum control for the DT head transient response becomes possible.
The signals that are supplied from other circuit boards for DT head control, are listed as follows.

From VO board
- PB V : PB V signal
- PB H : PB H signal
- RF ENV : PB RF envelope signal

From CK board
- FHX : PB H signal (AFC output)

From DD board
- ST GAUGE : DT head operation information

From SV board
- ~RD INT 2 : 32×V signal
- ~RESET : Reset signal for CPU
- PB WINDOW : Window of the PB V signal
- REF ADV V : Phase information of the REF V signal
- SV A0-SV A5 :
- SV D0-SV D7 :
- ~RD CS :
- ~SV RD :
- ~SV WR :

(SV A0-SV A5, SV D0-SV D7, ~RD CS, ~SV RD, ~SV WR): CPU control information

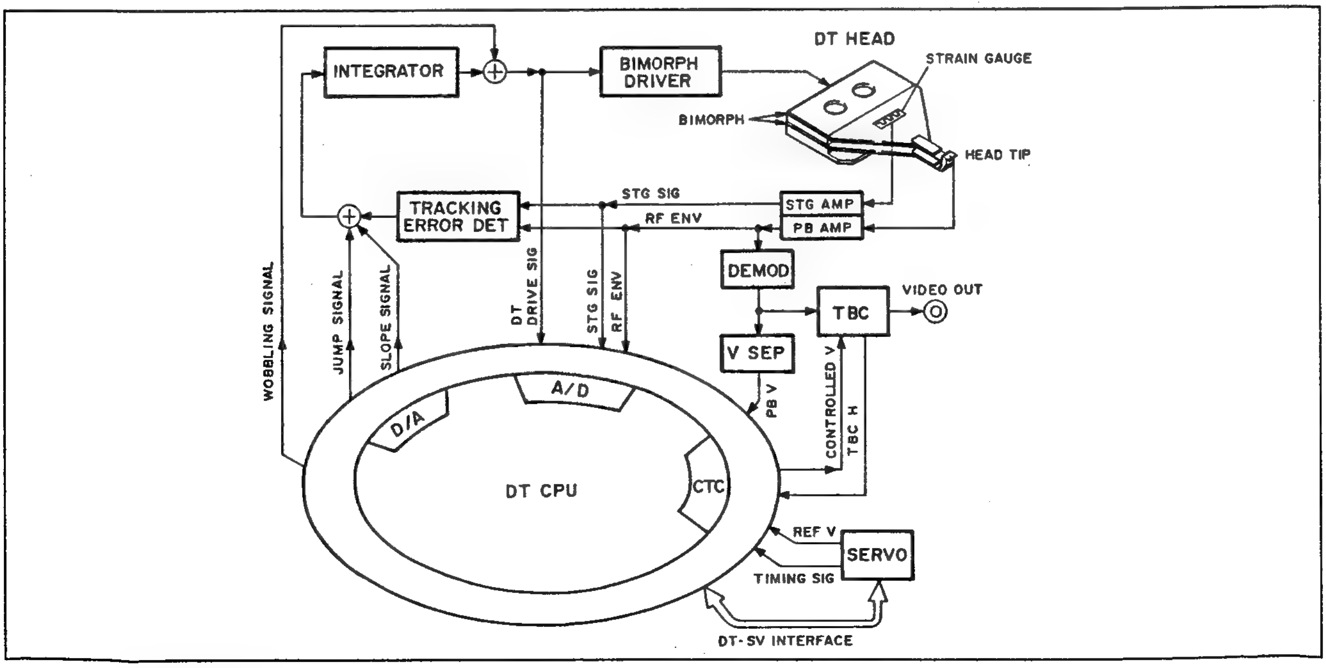


Fig. 4-5-1. BVH-3000/3100 DT System

4-5-2. DT CPU (RD-6/RD-7 Board)

(1) Outline of CPU (RD-6/RD-7 board)

ICL20 (ICM18) μPD78C10G is the CMOS 8-bit CPU that has built-in 16-bit ALU, 256 bytes RAM, 8-bit A/D converter, multi-function 16-bit timer/event counter, two 8-bit timers and general purpose serial interface. This CPU is also capable to make direct addressing to external memories of maximum 64k bytes.
The clock signal is the 12 MHz that is generated by the ceramic resonator (X1), realizing the minimum command execution time of 1 μsec. As its external memories, the ICL15 (ICM14) 8k bytes EPROM and ICM16 (ICN15) 2k bytes SRAM are employed. The power voltage of SRAM is backed up by ICN22 (ICM21) and battery so that the data can be kept memorized even while the power is turned off.

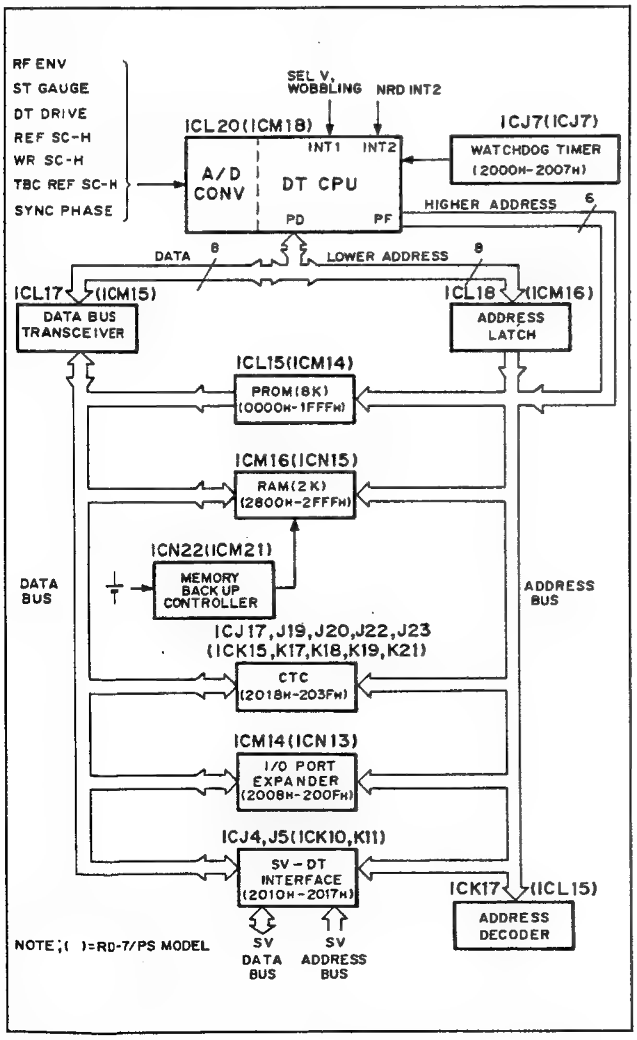


Fig. 4-5-2. CPU Peripheral Circuit (RD-6/RD-7)

The ICM14 (ICN13) I/O port expander is securing the ports equivalent to 4.5 bytes. Various measurements are performed by five CTC (programmable timer counter) ICJ17, J19, J20, J22, J23 (ICK15, K17, K18, K19, K21). These programmable timer counters are those of 3×16 bits, capable to measure in six modes of operation that are controlled by CPU. Clock frequency of up to 8 MHz can be used. The vertical information and wobbling information are input to pin 26 (INT1 terminal) of CPU while the "~RD INT2" signal is sent from the SV board to its pin 20 (INT2 terminal), as the external interrupt signal to the CPU. The "~RESET" signal that is supplied from SV board, is passing through ICL14 (ICL12), and is input to its pin 28 (RESET terminal) as CPU reset signal. By this reset signal, if the power supply voltage becomes lower than approximately 4.5V or when the power is turned on/off, the CPU is automatically reset. The DT CPU is interfaced to the SV CPU on the SV-90 board through ICJ4 and J5 (ICK10 and K11) 4×4-bit memories.
The DT CPU is functioning not only as the DT head controller but also controlling the detection of the servo reference SC-H phase, tape SC-H phase, SV CF detection.

(2) Address/data separator (RD-6/RD-7 board)

Because the transmission and reception of data D0 through D7 and the output of lower addresses A0 through A7 are commonly sharing the port D (PD0 through PD7) in the ICL20 (ICM18) CPU, data and address are separated by the ICL18 (ICM16) address latch and the ICL17 (ICM15) bus transceiver. The lower addresses that are output from the address latch, are added to the upper addresses (A8 through A13) that are output from port F (PF0 through PF7), becoming the 14-bit address bus. At the same time, the signal that has passed through bus transceiver, becomes the 8-bit data bus. The ICK17 (ICL15) is the address decoder that is generating the write address.

(3) Watch dog timer (RD-6/RD-7 board)

The ICJ7 (ICJ7) monostable multivibrator is functioning as a watch dog timer that generates approximately 2 msec pulse by the write pulse. The write pulse is input to the watch dog timer in every 1/32 field (approximately 520 μsec in NTSC model, and 625 μsec for the PAL/SECAM model). The Q output of ICJ7 is kept to "H" level normally, but it will go into "L" level if the CPU should run-away, so that the CPU should be reset.

(4) Memory back-up circuit (RD-6/RD-7 board)

The ICN22 (ICM21) is the back-up controller for the ICM16 (ICN15) SRAM, that is monitoring the +5V power supply voltage at all times. If the power supply voltage becomes approximately 4.5V or less, the chip enable terminal of ICM16 (ICN15) is set to "H" level so that write operation is inhibited, and at the same time the power supply to the SRAM is switched to the battery. The ICN22 (ICM21) detects the battery output voltage when the power is turned on. When the battery output voltage is lower than 2.0V, the second memory cycle is prohibited so that check becomes possible.
The lithium battery of 180 mAH is employed. When the TC5517AFL SRAM consumes the maximum consumption current of 1 μA in standby mode, and the DS1210 back-up controller consumes 1 μA, the battery life is calculated as approximately 10 years. If two times tolerance is considered, it becomes approximately 5 years.

(5) I/O port expander (RD-6/RD-7 board)

The ICM14 (ICN13) I/O port expander is equipped with the four sets of 8-bit I/O port where input and output can be assigned in 4-bit unit, and one set of 4-bit I/O port where input and output can be assigned in 1-bit unit. The following signals are assigned to the CPU and I/O port expander.

CPU port assignment : ICL20 (ICM18)

PIN	I/O	SIGNAL
1 : PA0	I	REF FRAME
2 : PA1	O	Δf GATE
3 : PA2	I	IN-PHASE DETECTOR (H : IN-PHASE)
4 : PA3	O	PB V SELECTOR (H : PB V)
5 : PA4	O	SG OFF (H : ON)
6 : PA5	O	INTEG OFF (H : OFF)
7 : PA6	O	DT DRIVE SELECTOR (H : ON)
8 : PA7	I	PB V
9 : PBO	I	BURST DETECTOR············RD-7/PS
10 : PB1	O	RINGING OFF (H : OFF) ····13 board
11 : PB2	O	SC-H/RING (H : SC-H) ·······13 board
12 : PB3	O	INT1 SG SELECT (H : ON) ····13 board
13 : PB4	O	DT FILTER (H : OFF)········13 board
17 : PCO	O	GREEN LED : DARK (H : ON)
18 : PC1	O	GREEN LED (H : ON)
19 : PC2	O	RED LED (H : ON)
20 : PC3	I	INT2 INTERRUPT
21 : PC4	O	CPU MONITOR
22 : PC5	O	INTERRUPT MONITOR
23 : PC6	I	WOBBLING TIMING (H : OFF)
24 : PC7	O	DT RESET (L : RESET)

I/O port expander port assignment : ICM14 (ICN13)

PIN	I/O	SIGNAL
54 : PA0	O	12-BIT D/A CONVERTER
55 : PA1	O	
56 : PA2	O	
59 : PA3	O	
60 : PA4	O	
61 : PA5	O	
62 : PA6	O	
63 : PA7	O	
64 : PB0	O	
3 : PB1	O	
4 : PB2	O	
5 : PB3	O	
11 : PC0	O	8-BIT D/A CONVERTER
| |	O	
18 : PC7	O	
20 : PD0	O	JUMP STATUS 1
21 : PD1	O	JUMP STATUS 2
22 : PD2	O	JUMP STATUS 3
49 : PX0	O	SV CF
50 : PX1	O	CF RESET
52 : PX2	I	TEST SWITCH
53 : PX3	O	OUT SC-H (L : ON)·······RD-6/NTSC 3-FIELD RESET (H : EVEN)RD-7/PS

(6) Interrupt process (RD-6/RD-7 board)

Most of the data processing by the CPU, is carried out by interrupt using the "~RD INT2" signal that is supplied from the SV-90 board. The "~RD INT2" signal is the signal that is obtained by dividing one field into 32. It means that interrupt takes place every approximately 520 μsec for the NTSC model and every approximately 625 μsec for the PAL/SECAM model. The CPU performs the Δf detection and outputting of the signal to the ICL12 (ICL11) 8-bit D/A converter at every interrupt, and performs other processing during the rest of time.
The V interrupt signal and wobbling interrupt signal are input to the INT1 terminal of the CPU. The CPU determines the amount of DT head jump by detecting the amount of Δf and Δϕ, at the timing of V interrupt. The calculated amount of DT head jump is converted into analog signal by the ICM12 (ICM11) 12-bit D/A converter, and is sent to the DT head driver. The interrupt by wobbling can provide the detection whether DT head is displacing normally or not, from the strain gauge output, and makes judgment to turn on or off the integrator of the DT head driver. Interface between SV board and RD board, is carried out by the ICJ4/ICJ5 (ICK10/ICK11) 4×4-bit register file. Data transmission/reception that are periodically done, are shown as follows. Now, in the EPROM with version 1, write and read are done once in every vertical timing. In the EPROM with version 2, they are done twice in

every vertical timing, and not only the periodic data transmission／reception but also arbitrary data transmission／reception in accordance with requesting address from the CPU, is possible.

<u>SV board→RD board</u>

DSR0 bit5 : STILL (version 2 and later)
bit4 : PHASE LOCK (version 2 and later)
bit3 : CONFI
bit2 : FIELD／FRAME
bit1 : CAPSTAN LOCK
bit0 : DT ENABLE

DSR1 bit3 : OUTPUT SC-H (1 : EVEN)
bit2 : PINCH OFF
bit1, bit0 :
SC-H SHIFT
00 : SC-H 0
01 : SC-H +
10 : SC-H −

DSR2 bit3 : VIDEO LACK
bit2, bit1 :
TV SIG
00 : NTSC
01 : PAL-M
10 : PAL
11 : SECAM
bit0 : AUTO JUMP

<u>RD board→SV board</u>

DSW0 bit3 : INTEG ON
bit2 : CF DETECT
bit1 : BAT ERROR
bit0 : DT CPU ERROR

DSW1 bit3 : TAPE／REF SC-H SEL
bit2, bit1, bit0 :
REF SC-H DATA
000 : BLANK
001 : SC-H<−70°
010 : −70° <SC-H<−40°
011 : −40° <SC-H<−20°
100 : −20° <SC-H<+20°
101 : +20° <SC-H<+40°
110 : +40° <SC-H<+70°
111 : +70° <SC-H

DSW2 bit3 : TAPE／REF SC-H SEL
bit2, bit1, bit0 :
TAPE SC-H DATA
000 : BLANK
001 : SC-H<−70°
010 : −70° <SC-H<−40°
011 : −40° <SC-H<−20°
100 : −20° <SC-H<+20°
101 : +20° <SC-H<+40°
110 : +40° <SC-H<+70°
111 : +70° <SC-H

4-5-3. ADV PB V Generator (RD-6／RD-7 Board)

The PB V signal is input to the RD board from the VO board as a jump timing signal. The PB V signal has the timing of negative going of the second equalizing pulse of the playback video signal. In order to prevent from the effect of dropout, etc., an AFC loop using PB signal, is formed in RD board that generates ADV PB V signal. The ADV PB V signal is used as the jump timing signal. The ADV PB V signal is the signal that is advancing to the PB V signal phase by 2H (3H for EPROM with version 2). This phase difference is provided considering the operation time of the CPU required to calculate the jump amount after detection of V signal. Jump timing is normally using the ADV PB V signal, but when the relation between ADV PB V signal phase and PB V signal phase is changed, it is reset immediately by PB V signal timing. Also the 16th line of playback signal is detected at the same time, and is sent to the TBC system (CK board) as the DT V signal.
The PB V signal that is input to "A20b" terminal of the RD board, is gated by the PB WINDOW signal that is input to "B4c" terminal, and is input to the ICK12 (ICK12) V selector. The PB WINDOW signal generated by the SV board is the window pulse of −6H／+4H width against the PB V signal. Because the PB WINDOW signal is generated from the PG pulse, when drum is not rotating, it may be input to the RD board with erroneous timing. To prevent this, the PB WINDOW gate is inhibited during DT OFF period in such mode as EE mode, by the PA6 (pin 7) output of the CPU.
The FHX signal that is input to B11c terminal of the RD board, is the playback H signal which is stabilized by AFC, and is supplied from the TBC (CK board). The FHX signal is frequency-doubled by ICH15 (ICJ7, J8) and becomes 2FHX signal. The CTC counts the 2FHX signal and generates the ADV PB V signal.
The ADV PB V signal is generated by the three counters (CTC32, CTC31, CTC30) that are built-in CTC ICJ20 (ICK17). The clock signal for each counters is the 2FHX signal. The GATE terminal (pin 16) of CTC32 receives the SEL V signal from the V selector. The GATE terminal (pin 14) of CTC31 receives the jump status signal from the output terminal(pin 17) of CTC32. The CTC30 GATE terminal (pin 11) of CTC30 receives the DT V signal from the output terminal (pin 13) of CTC31. The V selector(ICK12) selects first the PB V signal as the SEL V signal. After the ADV PB V signal and the PB V signal establish the specified phase relationship, it selects the ADV PB V signal as the SEL V signal. CTC32 performs three counts of 2FHX signal during when the SEL V signal remains "LOW" level, and produces its output. The CPU performs calculation to determine the jump amount during this period. The counted

data according as the jump amount, are written into CTC31. Thus, the output of CTC31 becomes always at the timing of 16th line of playback signal. Since the playback video signal length is made longer or shorter at every one track pitch jump for the amount of 2.5H (3.5H in the PAL/SECAM model), the counted data must be changed in accordance with the amount of jump. The CTC31 output is the DT V signal that is sent to TBC (CK board). CTC30 performs counting of fixed value after the DT V signal, and produces ADV PB V signal at the timing of 2H (3H for EPROM with version 2) before the PB V signal phase.

Counter 0 (CTC40) of CTC ICJ22 (ICK18) generates the one clock (1/2H) width pulse at the timing of 2H (3H for EPROM with version 2) after the ADV PB V signal. This pulse is input to ICK13 (ICK14) as the window of the PB V signal. ICK13 (ICK14) detects whether leading edge of PB V signal is located within the window pulse or not. The detected phase information is input to the PA2 terminal (pin 3) of the CPU. The CPU controls the V selector based on this phase information. The PB V signal is also input to the AN4 terminal (pin 38) of the CPU, so that the information from ICK13 (ICK14) is neglected if the PB V signal is not detected.

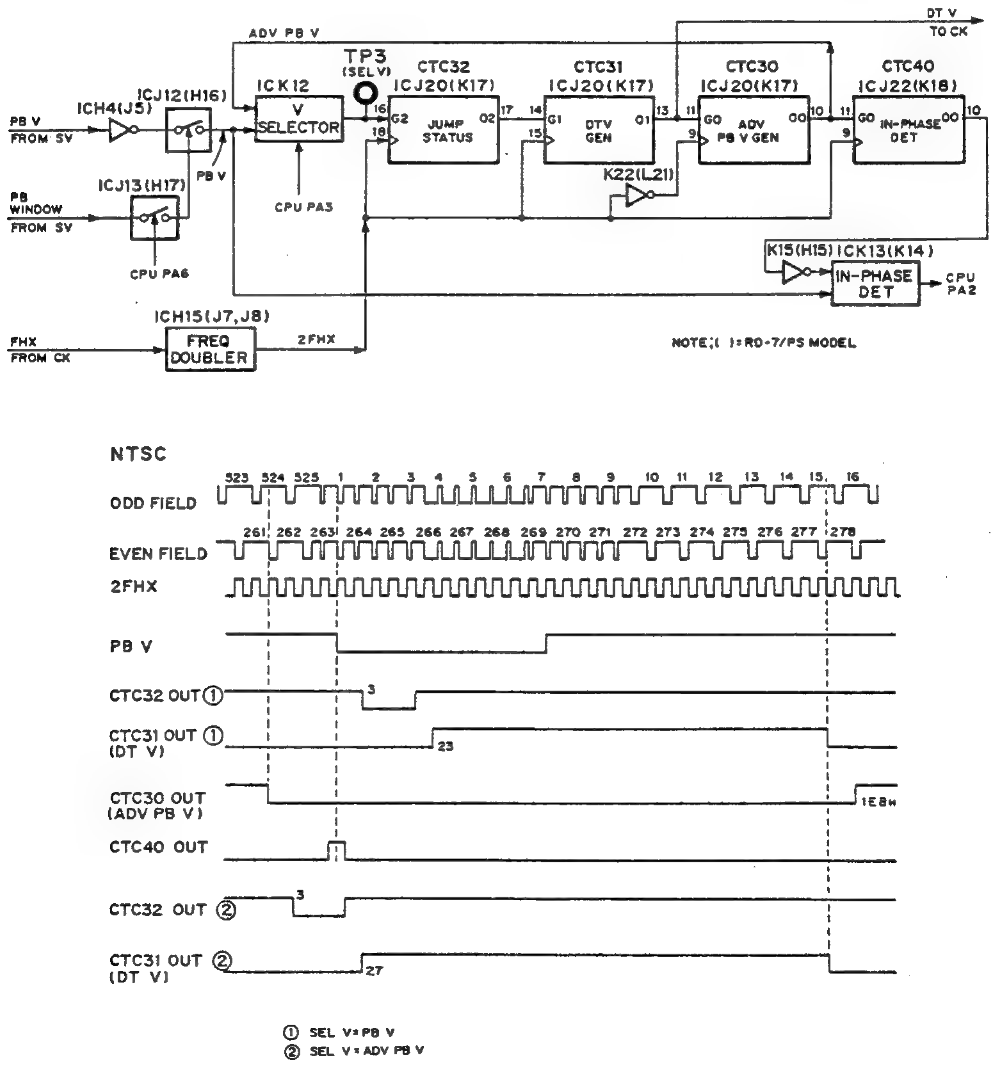


Fig. 4-5-3. ADV PB V Generator (RD-6/RD-7)

4-5-4. Δf Detector, Δφ Detector and Wobbling Signal Generator (RD-6/RD-7 Board)

When a recorded tape is played back in the different tape speed other than that used in the recording mode, the playback head will have different head angle other than that of recorded track. The Δf correction is to control the the DT head displacement until the trace angle of DT head becomes equal to the recorded track angle. When tape speed is changed, the trace angle of the DT head is also changed so that the length of playback video signal in a unit time period is also changed. By measuring the H sync pulse period of the playback signal, the Δf can be detected. In the other words, the Δf is the relative speed information of head against tape.

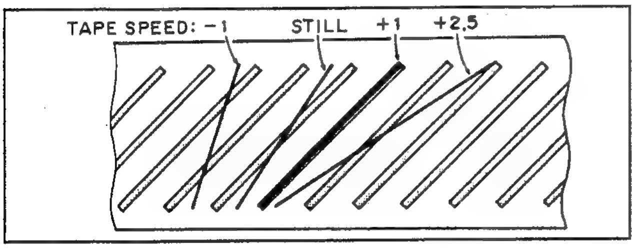


Fig. 4-5-4. Δf Correction

Because of difference in the track linearity between the recorded track and DT head, etc., the Δf alone cannot correct all the the tracking error so that some tracking error still remains. In order to remove the tracking error, the DT head is wobbled at a certain frequency (720Hz for the NTSC model, 700Hz for the PAL/SECAM model) in the direction parallel to the head gap. The playback RF signal is amplitude modulated by this wobbling where the amplitude modulation component is extracted from the playback RF signal, in order to detect tracking error component. Feedback is applied to the DT head controller until the tracking error is kept to constant value. Thus the DT head displacement is controlled.

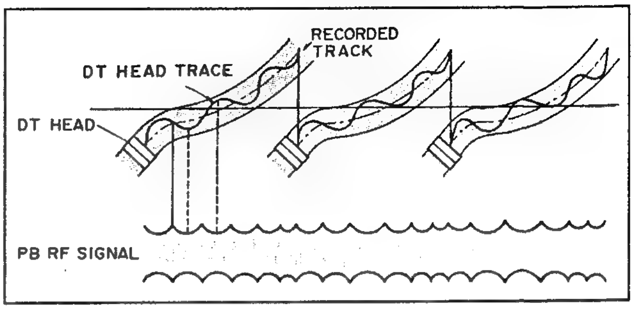


Fig. 4-5-5. Wobbling

When playback head reaches the end of a recorded track by tracing, it must determine which track should be traced next. When slow playback is carried out, the same video track must be repeatedly traced. When playback of faster than ×1 speed is carried out, skip tracing must be performed.
For an example, the case when DT playback at 1.2 times normal speed, is explained as follows.
The recorded track is shown in solid line and tracing of fixed playback head against the recorded track is shown in dotted line. In order for tracking to be conducted correctly, the DT head must be displaced from the dotted line to solid line. In this example, the 4th and 10th tracks are skipped. When the DT head is jumped, the jump position and jump amount are determined and controlled by the Δφ and aforementioned Δf. The Δφ is the phase information of the playback signal against the reference signal, that is detected by measuring the phase difference between the REF V signal and PB V signal.

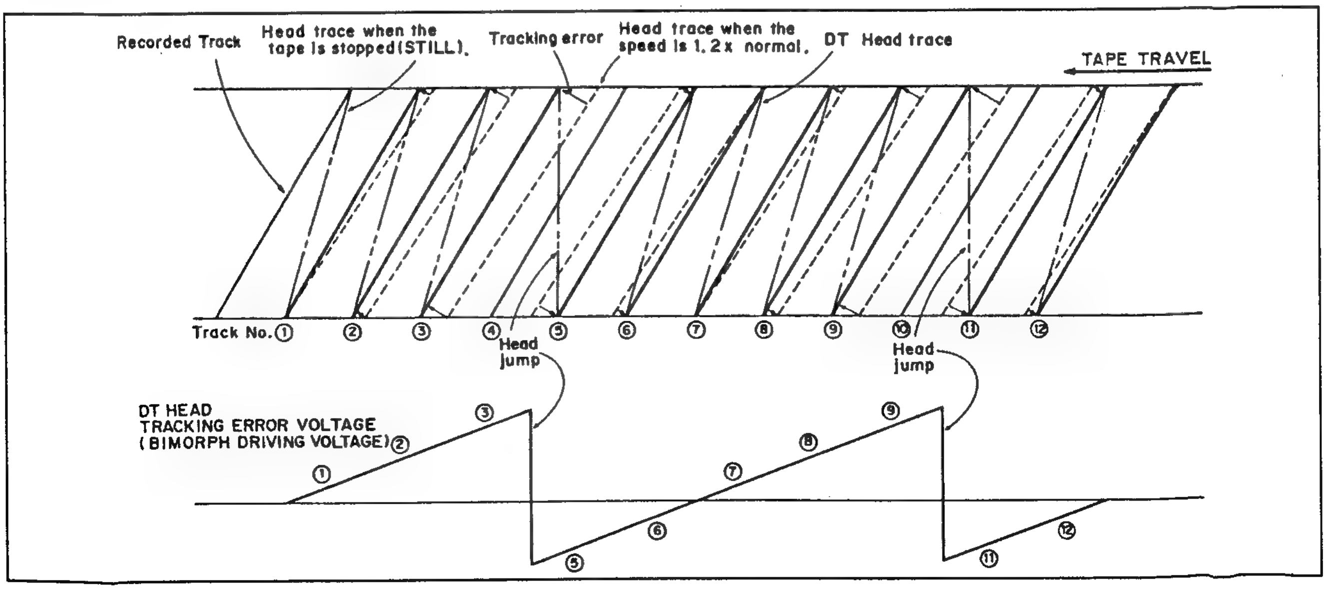


Fig. 4-5-6. Head Jump

(1) Δf detector (RD-6/RD-7 board)

The GATE terminal of CTC12 (pins 16, 17, 18 of ICJ17/K19) receives pulse from the PA1 terminal of the CPU at every interrupt event of "~RD INT2". CTC12 performs three counting of FHX that is the playback H signal, as triggered by the aforementioned pulse, so that the pulse that is equivalent to 3H width of playback signal, is output. CTC22 (pins 16, 17, 18 of ICJ19/K21) is a down counter that works only when its GATE terminal is "H" level, and is preset to "1417" in the NTSC model and "2374" in the PAL/SECAM model. When 3H width pulse is input to CTC22 from CTC12, CTC22 starts counting and the counted data are held after input pulse is ended. The clock pulse for CTC22 is 2fsc in the NTSC model and is 908fH/2 in the PAL/SECAM model. The memorized data in CTC22, is written by the CPU at the timing of next "~RD INT2" interrupt, so that the counter is preset again, and the PA1 terminal of the CPU output the pulse. This operation is repeated. The data that is written by the CPU is output from 8-bit D/A converter as the slope information of the head.

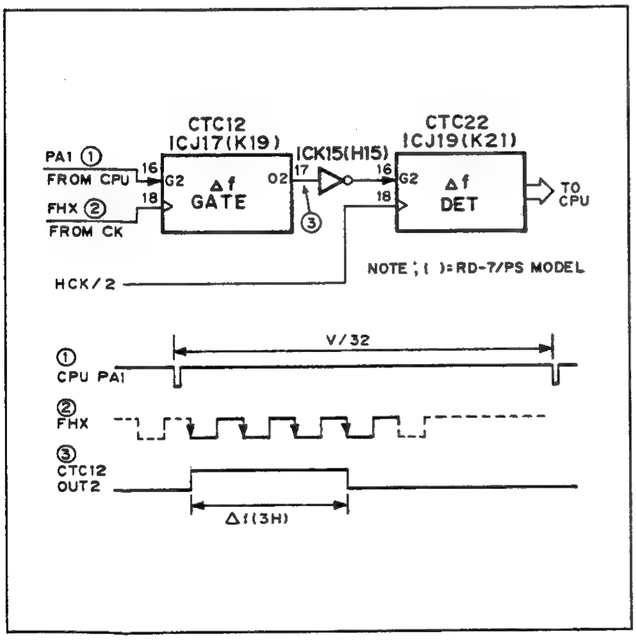


Fig. 4-5-7. Δf Detector (RD-6/RD-7)

(2) $\Delta \phi$ detector (RD-6/RD-7 board)

The REF ADV V signal is the signal of ±6H width centering around the PB V signal timing. This timing does not change due to tape speed nor phase. So, phase difference between the reference signal and playback signal can be known by measuring the SEL V signal phase against the REF ADV V signal phase. Because BVH-3000/3100 is using the ADV PB V signal as the V signal where the ADV PB V signal advances by 2H (after version 2, it is 3H) to PB V signal, the PRE REF ADV V signal whose phase is advancing 2H (or 3H) to REF ADV V signal, is generated by CTC41 (pins 13, 14, 15 of ICJ22/K18). The phase difference between the PRE REF ADV V signal and SEL V signal is compared by ICK13 (K14) and the phase difference is converted to a pulse width. CTC10 measures the pulse width of ICK13 (K14), that is in other words, $\Delta \phi$. The measured $\Delta \phi$ data are read by the CPU at the SEL V signal timing, and are used for jump judgment. The 2fsc clock is divided by 25 with CTC11, and it is used as the clock pulse for CTC10 in the NTSC model. The 908fH/2 clock is divided by 34 with CTC11, and it is used as clock pulse for CTC10 in the PAL/SECAM model.

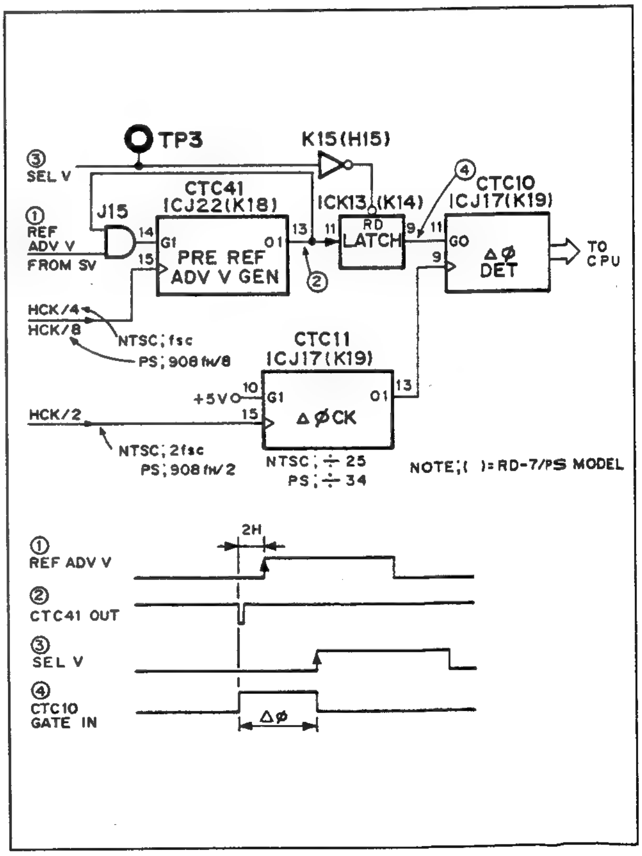


Fig. 4-5-8. $\Delta \phi$ Detector (RD-6/RD-7)

(3) Wobbling signal generator (RD-6/RD-7 board)

[When the suffix No. of the RD board is -11 or -12]
CTC20 (pins 9, 10, 11 of ICJ19/K21) divides the clock signal to 720Hz (700Hz in the PAL/SECAM model) during when the GATE terminal is "H" level. PA6 is the signal that goes to "H" level when DT is ON. So, the GATE terminal of CTC20 receives the REF ADV V signal only when DT is ON so that the signal that has wobbling repetition cycle is output from pin 10 (OUT0). CTC21 (pins 13, 14, 15 of ICJ19/K21) outputs the pulse of approximately 1100 μsec width from the SEL V signal, and during this period, the wobbling is stopped to OFF. The output signal thus obtained, is passed through the ICL9 low-pass filter to be shaped to sine wave, and becomes the wobbling signal.

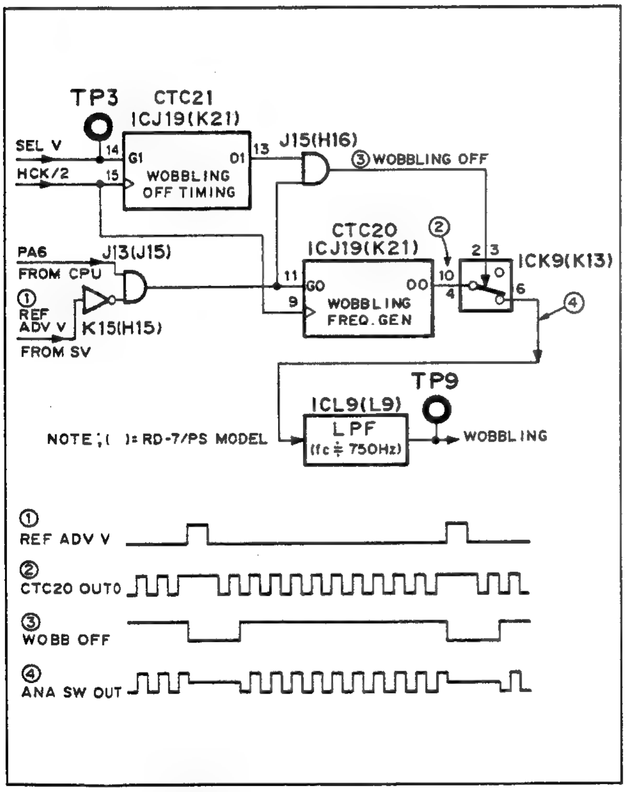


Fig. 4-5-9. Wobbling Signal Generator (RD-6/-7 : -11, -12)

[When the suffix No. of the RD board is -13]
CTC21 (pin 13, 14, 15 of ICJ19/K21) counts the clock constantly from the REF ADV V signal only during DT ON, and outputs "L" level at the last clock timing. CTC20 (pins 9, 10, 11 of ICJ19/K21) divides the clock into 720Hz in the NTSC model (700Hz in the PAL/SECAM model). CTC20 starts counting at the rising edge of the GATE input pulse so that the wobbling phase can be changed by the counting numbers of CTC21. In the circuit on the RD board with "suffix-13", the wobbling off period is not set. The output pulse thus obtained, is shaped into sine wave by a low-pass filter, and becomes the wobbling signal.
Because the negative going of CTC20 output signal corresponds to the peak of wobbling signal, this signal is input to INT1 terminal of CPU so that the level of strain gauge signal is measured at the moment of interrupt, in order to detect the wobbling of DT head and is used to judge the generation of INTEG OFF (integrator stop to off) signal. The wobbling timing signal is input to PC6 terminal of CPU so that the SEL V signal and wobbling are discriminated when INT1 terminal is interrupted.

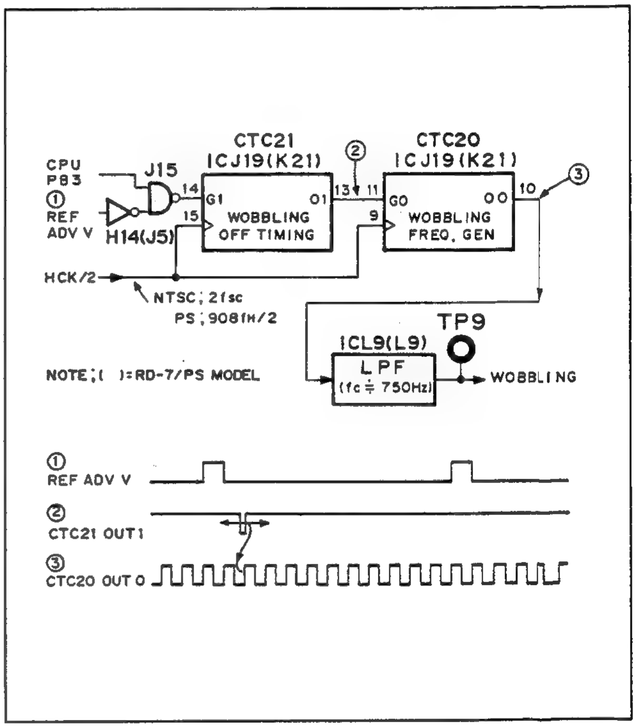


Fig. 4-5-10. Wobbling Signal Generator (RD-6/-7 : -13)

4-5-5. Tracking Error Detector (RD-6/RD-7 Board)

Displacement condition of the DT head can be detected from the ST GAUGE (strain gauge) signal. The strain gauge is a resistive material (approximately 120 Ω) that is attached on top of the bimorph plate of the DT head, whose resistance value changes depending upon physical stretch and shrinkage of the bimorph plate. Motion of DT head can be detected from the change of resistance value of the strain gauge.
Trace condition of the DT head with reference to the recorded track can be detected from the RF envelope signal. Since the DT head is tracing the recorded track while it is wobbling, the RF envelope of upper portion and lower portion will become symmetrical when the recorded track is straight. If the recorded track is curved, it will lose symmetry.

Only the AC component that is included in the RF envelope and strain gauge signals are amplified, and passed through approximately 500 Hz low-pass filter and are input to the ICM3 (ICN3) multiplier. The wobbling frequency component and its doubled frequency component that are included in the multiplier output signal, are removed by the notch filter (band eliminating filter) at the next stage so that only the tracking error information is extracted. The extracted tracking error information is input to the integrator (DT drive signal generator) at the next stage. The integrator output signal is fed back to the input of the strain gauge amplifier so that the slope signal component included in the strain gauge information can be removed.

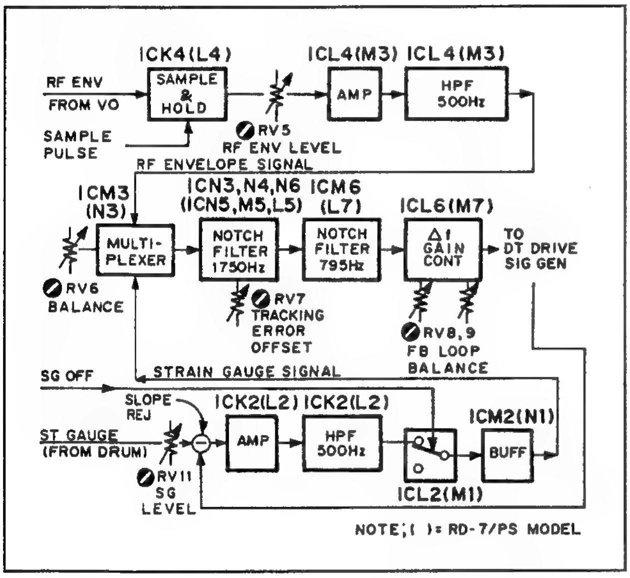


Fig. 4-5-11. Tracking Error Detector (RD-6/RD-7)

4-5-6. DT Drive Signal Generator (RD-6/RD-7 Board)

When a recorded tape whose track is outside the type-C format, is played back, or when sensitivity of the DT head is changed after long period of use, the jumped position (contact starting position) of a track can be off-track of the recorded tape. In this case, the playback RF signal level remains low until the DT head follows the recorded track by wobbling, so that streakings on the top of monitor screen can appear.

In the BVH-3000/3100, the RF envelope level at the beginning of playing back of a track, is detected and the jump amount is always changed for the maximum RF envelope level. This control is called as "AUTO JUMP". This jump amount data are memorized in each modes of every jump pitch (in field mode, −3, −2, −1, 0, +1, +2, +3 pitches, and in frame mode, −2, 0, +2 pitches respectively). This memorized data are backed up even during power is turned off.

The signal such as the jump signal from the ICM12 (ICM11) 12-bit D/A converter, Δf signal from the ICL12 (ICL11) 8-bit D/A converter and the tracking error information are added and are input to the ICL6 (ICM7) integrator. The integrator generates the slope wave from the Δf and tracking error information in proportional to the bending of recorded track, and converts the jump signal into the jump wave. The jump wave and the wobbling signal are superimposed and the the DT drive signal is generated. DT ON/OFF is controlled by PA6 (pin 7 of CPU). The RV10 is used when the DT head motion is visually checked and becomes active as the jumper plug is changed from JP3 to JP4.

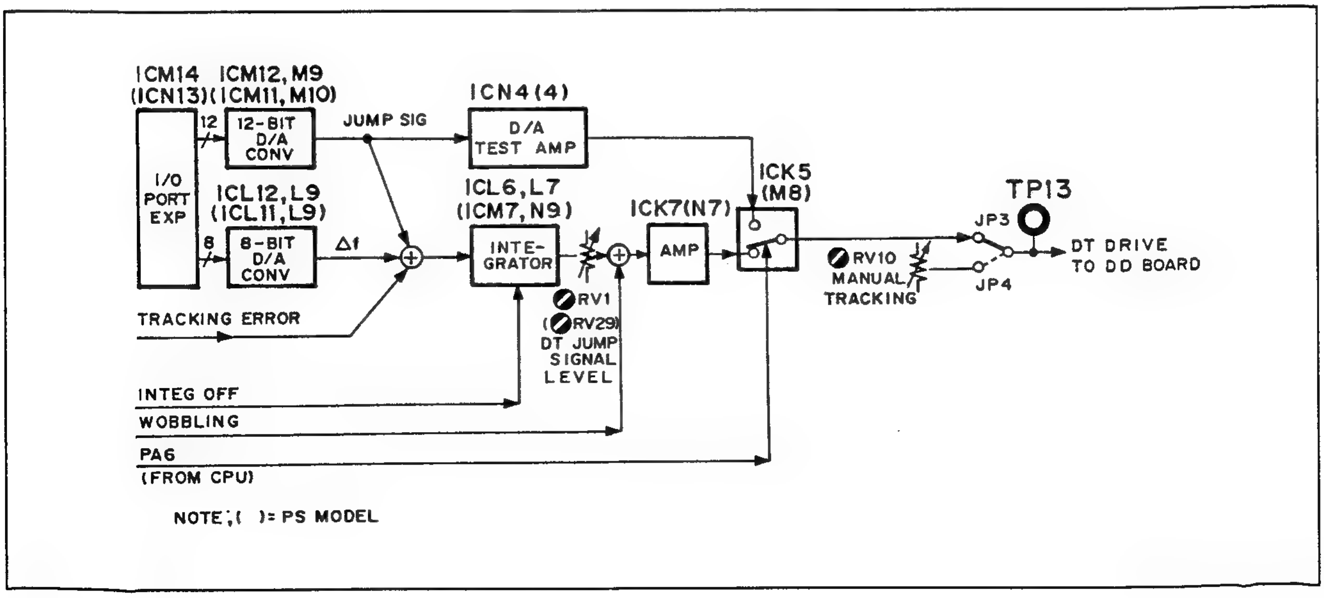


Fig. 4-5-12. DT Drive Signal Generator (RD-6/RD-7)

4-5-7. Additional Function for Board No."-13" (RD-6/RD-7 Board)

(1) Ringing level detector (RD-6/RD-7 board)

Ringing is the unwanted vibration that is generated when the DT head is moved quickly. The ringing is generated immediately after head jump, resulting in the poor RF waveform during playback at the beginning portion of track by the DT head.
BVH-3000/3100 employs the two-step jump system in order to decrease the ringing. In this system, steep slope is used first to drive the DT head and this slope is made slow in its middle in order to suppress ringing so that the DT head is driven.

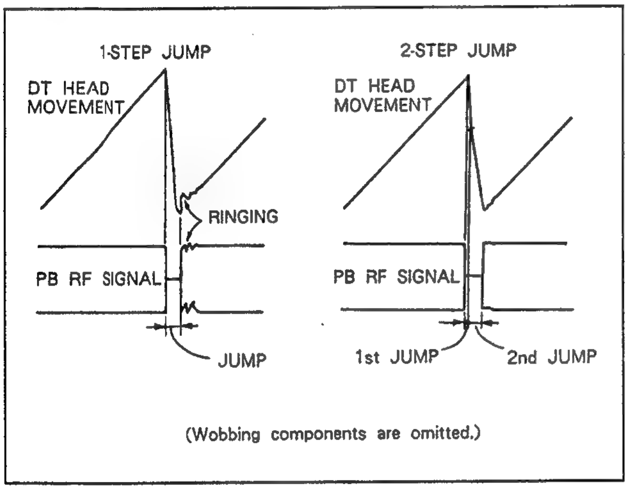


Fig. 4-5-13. Two-Step Jump System

But, the time that can be used for jump is fixed, the adverse effect from non-uniform performance of DT heads cannot be completely removed. Then, in the RD board having suffix-13 and later, the function that can control the jump time so that the ringing detection level becomes minimum, is added. The primary resonant frequency of bimorph that is the major component of the ringing, is extracted from the strain gauge signal, and input to the CPU. The CPU adjusts the ratio of jump at the first period and second period so that the ringing is minimized. This adjustment is started by pressing the TEST switch (S1) on the RD board for approximately two seconds during VAR −1 speed mode (CTL lock mode). During this adjustment, the "READY" LED blinks and when it is adjusted for optimum value, the LED is turned off and the adjustment is automatically finished. This adjustment should be done when upper drum is replaced so that the DT head can be jumped optimum track.
The strain gauge signal is passed through ICK2 (IC5) high-pass filter of 500 Hz center frequency so that the slope component is removed. It is input to the ICM1 and ICM2 ringing level detector. Out of this input signal, the notch filter having center frequency of 720 Hz is used to remove the wobbling component, and then the bandpass filter having center frequency of 1350 Hz is used to separate the ringing component. The separated the ringing component is input to the ICN1 analog switcher where the beginning portion alone is extracted to be peak-held by ICM1 and ICM2. The ringing signal is mixed with the REF SCH signal by the ICN2 analog switcher and is input to the analog port of the CPU.

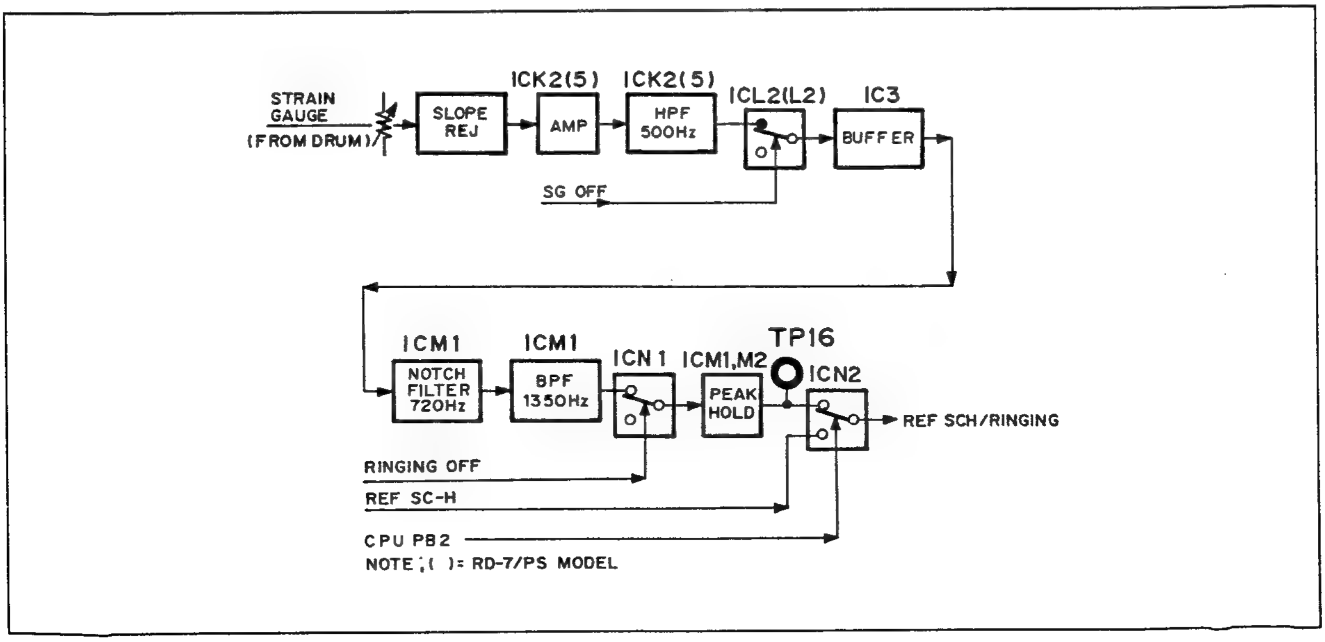


Fig. 4-5-14. Ringing Level Detector (RD-6/RD-7)

(2) Filter during DT OFF (RD-6/RD-7 board)

DT ON/OFF is controlled by the ICL5 analog switcher. When DT is OFF, output is set to 0V. But, depending upon the positions of the DT head, click noise can occur due to quick displacement. In the RD board having suffix-13 and later, the output is passed through a low-pass filter having center frequency of 500 Hz when the DT is turned OFF and then main line is released. Then the signal is smoothly set to 0V when DT is turned off and click noise is prevented.

(3) Feedback gain suppressor during INTEG OFF (RD-6/RD-7 board)

INTEG OFF is to stop the integrator that is generating slope signal, when the DT head happens to stop wobbling, or the DT head is not tracing the recorded track correctly. In this case, DT DRIVE signal is reset to the value near the center value and waits until the the DT head starts to follow the recorded track again. But, because tracking error detection gain is high, DT DRIVE signal comprises DC offset so that it takes time until the DT head starts following the recorded track again. Then in the RD board having suffix-13 and later, the tracking error detection gain is decreased during INTEG OFF period so that the time required to start following again, is shortened.

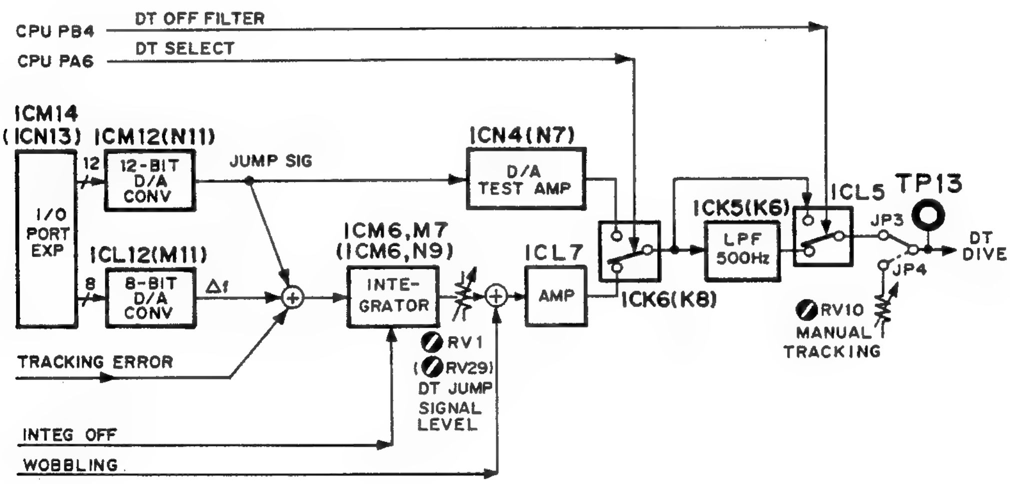


Fig. 4-5-15. Filter during DT OFF (RD-6/RD-7)

4-6. SERVO SYSTEM

4-6-1. Outline of Servo System

The servo system of the BVH-3000/3100 consists of the following boards.

SV-90 board : Main CPU
Address decoder
Video logic controller
Reference pulse generator
Sub CPU, motor servo
Tape transport interface

RD-6 (NTSC) /RD-7 (PS model) board :
Servo reference signal generator

CD-36 board : Capstan motor driver
Drum motor driver

RM-43 board : S reel motor driver
T reel motor driver

DS-19 board : Solenoid driver
Moving guide motor driver
IP roller motor driver
Sensor output level converter

(1) SV-90 board

The SV-90 board controls all operations after the mode controller, communication with the parallel remote (REMOTE 3), and logic processing of the video system, audio system, and TBC system.
Control signals for the tape transport system and video logic signals generated in this board are supplied directly as parallel data, and other control signals are supplied via a common bus, to the AU, VO, PR, CK, RD, SY and PA boards.
The SV-90 board has a main CPU (ICK19, V20 : μPD70108D) and a sub CPU (ICB15, μPD78C10G) which contains an A/D converter. The main CPU performs motor servo processing, CTL processing and timer processing. The RAM (ICE16) connected to the sub CPU is used for communication with the main CPU.
Most of the data in the servo system are processed by software. The processed data are latched in the respective boards, and used as control signals.
Each motor used in the BVH-3000/3100 is controlled by the CPU servo. An analog damping loop operates for transient responses which the arithmetic section of the CPU cannot follow, and the analog control voltage obtained is superimposed on the CPU servo control voltage.

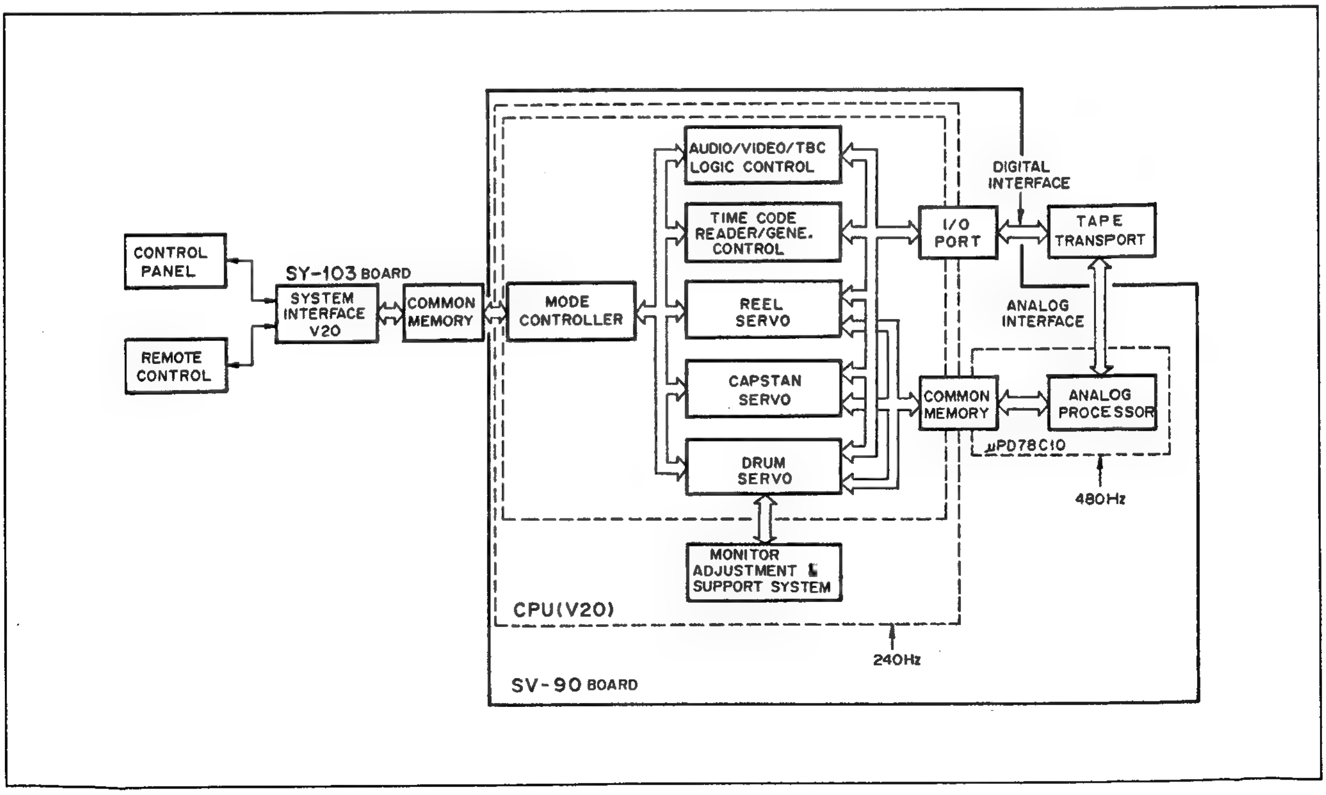


Fig. 4-6-1. SV-90 Board

In the CPU servo, the FG pulses and PG pulses generated according to the rotation of each motor are wave-shaped, and the outputs are input to the PTC (Programmable Timer Counter) and the PFC (Phase and Frequency Counter) where the phase and speed are measured.
The main and sub CPUs on the SV-90 board calculate the optimum control voltage for each motor based on the input data, and supply these voltages to D/A converter ICA16. The output of the D/A converter is time-sharing processed in an analog switcher, then passes through a sample hold circuit to be supplied to each motor as a motor control voltage for a digital servo.
The value of the potentiometer installed on the supply side (S) tension arm shaft (S-REEL TEN), capstan FG (CPADT, CPBDT, CPADD, CPBDD), T reel FG (T-REEL FG A, T-REEL F G B), S reel FG (S-REEL FG A, S-REEL FG B), the drum motor control voltage (DMVLD), and the capstan motor control voltage (CPVLD) are multiplexed by ICF9, ICF10 and ICF11, and supplied to the sub CPU ICB15 analog input (A-SIG0 to A-SIG3) terminals.
In the analog velocity loops of the drum system and capstan system, the time difference between the FG A pulse and the FG B pulse is measured for each pulse and converted into a voltage. The analog velocity loop is effective for the drum motor within ±6% of the regular speed, and for the capstan motor within ±6% of the velocity deviation in the normal PLAY mode. Consequently, in the variable mode, the capstan motor is controlled only by a digital servo which is controlled by the CPU.
Torque adjustment of each motor and drum PG adjustment, etc., can be performed from the control panel by using the setup menu. The adjustment values are stored in a non-volatile memory IC1 on the MB-140 board (mother board). Consequently, there is no need to adjust the servo system even if the SV-90 board is replaced.

(2) RD-6/RD-7 board

The RD-6 board (or RD-7 board for PAL/SECAM) consists of a servo reference signal generator circuit, TBC reference signal generator circuit, and DT control circuit.
The main functions of the servo reference signal generator circuit are as follows.

- REF SYNC generation
- REF V and REF H detection
- REF SC-H phase detection
- SEL FRAME and SEL CF generation

For details of the TBC reference signal generator circuit, refer to section 4-4 ; for details of the DT control circuit, see section 4-5.

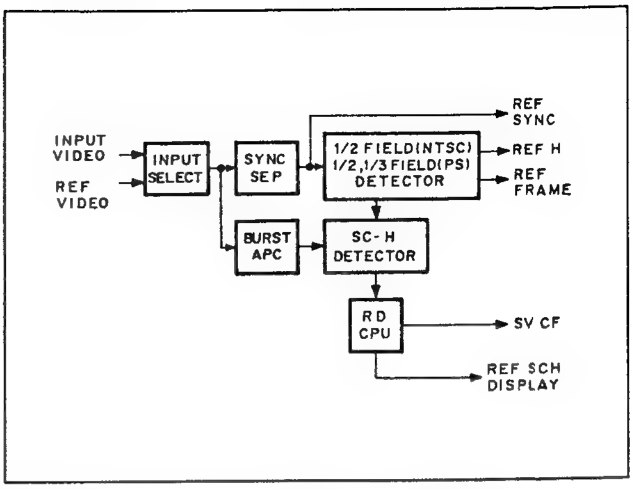


Fig. 4-6-2. Servo Reference Signal Generator (RD-6/RD-7)

(3) CD-36 board

The CD-36 board consists of the capstan motor and drum motor drive amplifiers. Each motor is driven by current control and voltage control by the MDA signal (analog signal) from the SV-90 board. The voltage is controlled by the MDA signal which varies the power supply voltage of the motor drive circuit up to a maximum of 40V. The variable voltage power supply is on the SP-02 board in the UR-20 power supply unit.
Three-phase DC motors are used for the capstan motor and the drum motor, hence it is necessary to switch the polarity on the drive circuit side. The signal which performs this polarity switching is generated inside each motor. The CD-36 board also detects the drum FG and capstan FG output and the drum PG.

(4) RM-43 board

In the RM-43 board, the analog control voltages (T REEL, MDA, S REEL MDA) and also the TRTCW signal and SRTCW signal which indicate the direction of torque generation are supplied from the SV-90 board in order to control the S reel motor and T reel motor drive voltage and current. Like the drum motor, the drive voltage controls the variable power supply voltage of the power supply unit. This voltage is set to a maximum of 80V.
The reel motor is a 3-phase DC motor, hence it is necessary to switch the polarity at the drive circuit side. The polarity switching signal is generated inside the motor. The RM-43 board also detects the reel motor FG output and the direction of rotation.

4-6-2. Servo Control System (SV-90 and MB-140 Boards)

(1) Clock pulse generator (SV-90 board)

This circuit consists of ICM19 and crystal X2. 14.7456 MHz clock pulses are output from pin 12 (OSC terminal) of ICM19. This frequency is divided into the specified frequencies by a circuit at a later stage, then used to measure the speed and phase of the motor servo system. Also, 50% duty 7.3728 MHz clock pulses are output from pin 8 (CLK terminal) of ICM19, and used in the main CPU and reference pulse generator circuit.

(2) Main CPU (SV-90 board)

The main CPU ICK19 (V20 : μPD70108D) is operated by 7.3728 MHz clock pulses from the clock pulse generator ICM19.
The main CPU uses interrupt control unit (hereafter called ICU) ICL16 as an external device. This device assigns a priority sequence to interrupts and then processes them. The following signals are input to the ICU.

- Pin 25 INTR7 : $\overline{\text{NVWR}}$ (When S2=ON)
- Pin 24 INTR6 : CPU INT (V/4 interval signal)
- Pin 23 INTR5 : TC INT (TC read timing signal)

EPROMs ICN5 and ICN3, each of which has a capacity of 256k bits, are used as external ROMs for the main CPU ICK19, providing a total memory capacity of 64k bytes. In addition, a 64k bit (8k byte) SRAM ICN7 is used as an external RAM.
In the main CPU ICK19, the lower 8 bits of the address bus are used both for addresses A7 to A0 and data D7 to D0. Consequently, it is necessary to separate data from addresses according to the respective timing. Addresses and data are separated by the ASTB (Address Strobe) signal output from pin 25 of the ICK19 main CPU. ICL2 and ICL1 are used as latches to extract only the lower 8 bits of the address. ICL2 operates as a latch for the internal bus, and ICL1 as a latch for the external main bus. Both of these ICs latch the lower 8 bits of the address at the rise timing of the ASTB signal. Data D7 to D0 which is separated from the address bus is interfaced to the data bus by bi-directional buffers ICM2 and ICM1.

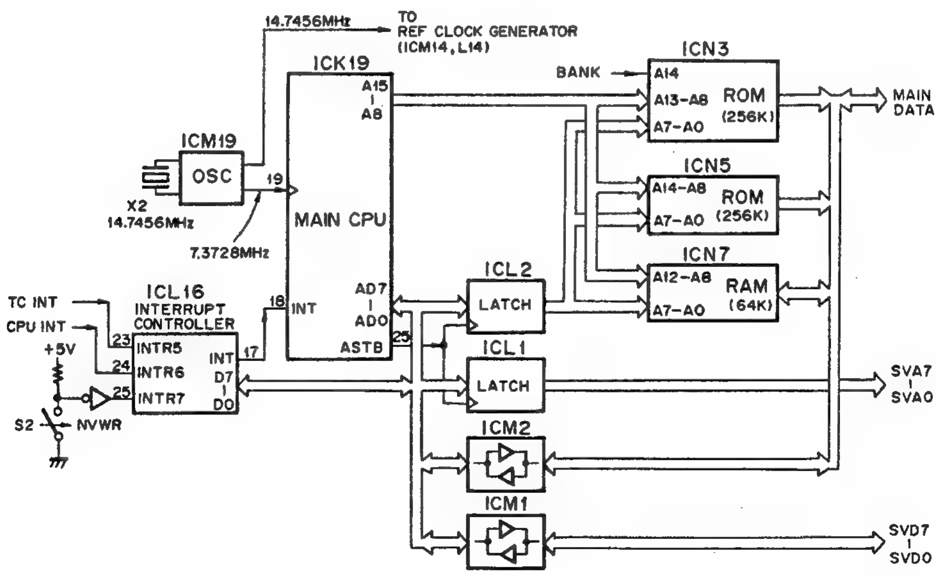


Fig. 4-6-3. Main CPU (SV-90)

(3) Main CPU memory (SV-90 board)

A 64k byte ROM (ICN5/ICN3) and an 8k byte RAM (ICN7) are used as the memory of the main CPU (ICK19). ROM ICN3 uses a bank select method in order to create a blank space in the address area. ROM ICN5 is assigned to addresses "0000H" to "3FFFH" and "C000H to "FFFFH". Also, ROM ICN3 is used as a bank method in which two kinds of data exist in addresses "4000H" to "7FFFH". Of these two kinds, the data to be output is selected by the BANK signal which is output from pin 20 of I/O expander ICG15. SRAM ICN7 is assigned to addresses "8000H" to "9FFFH".

(4) Address decoder (SV-90 board)

The main buses "SVA7 to SVA0" and "SVD7 to SVD0" are connected to each board in the amplifier chassis. They are also connected to various devices including PFC (Phase and Frequency Counter) and PTC (Programmable Timer Counter) as internal buses, and communicate with the main CPU (ICK19).
The chip select signal which specifies the opposite party for communication is generated by decoding the addresses output from the main CPU.
Chip selection of ROMs ICN5 and ICN3, and RAM ICN7 is performed by ICM4 and ICM5. The selection between an external port (AxxxH) and an internal port (BxxxH) is performed by ICM3. The chip select signal for the external port is generated by ICK1 and ICM6, and the chip select signal for an internal port is generated by ICM4, ICK3, ICK4, ICK5, and ICK6.

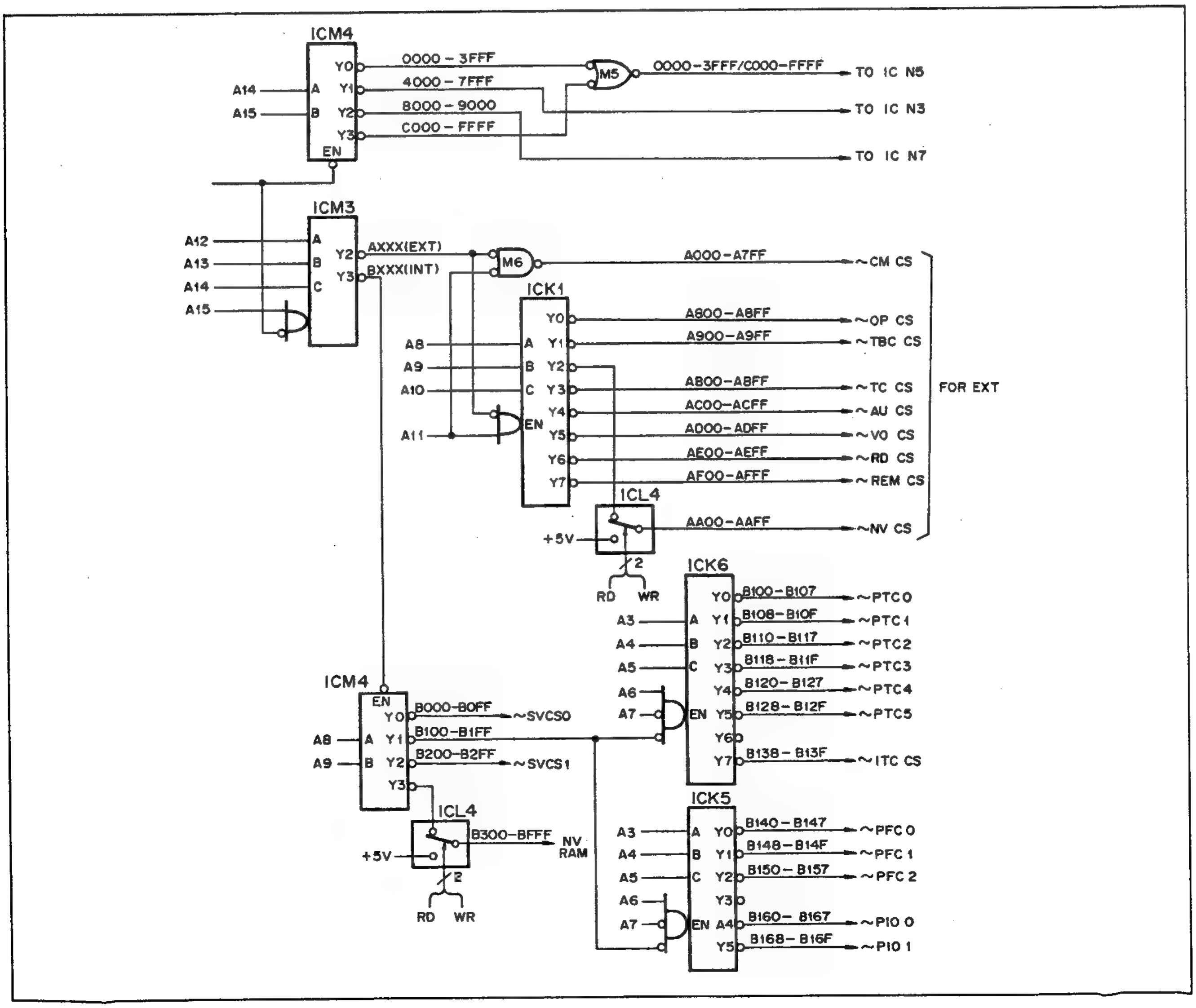


Fig. 4-6-4. Address Decoder (SV-90)

(5) Non-volatile memory (SV-90 and MB-140 boards)

A non-volatile memory (NOV RAM) is a special SRAM which can retain memorized data even after the power is switched off. The SV-90 board and the MB-140 board (mother board) each has a non-volatile memory containing the setup data.
The non-volatile memory (ICL3) on the SV-90 board contains mainly operating mode data such as remote select and the freeze mode. Non-volatile memory (IC1) on the mother board contains data related to the tape transport characteristics such as adjustment data for each motor which is necessary for processing data in the servo system. Consequently, there is no need to readjust the servo system in the event that the SV-90 board is replaced.

(6) Clock counters (SV-90 board)

Clock counters ICN8, N9 and N11 uses CMOS IC CF77074N each of which contains two 16-bit counters. These 16-bit counters count the period from the rising edge of the signal input to the START terminal to the rising edge of the signal input to the LATCH terminal, as the number of clock pulses input to the clock terminal. The count value at the timing of the rising edge at the LATCH terminal becomes 8-bit parallel data which is output from terminals D7 to D0.
Because the data output is in 8-bit parallel form and the counter and latch in the IC are 16 bit devices, the data is divided into 8 upper bits and 8 lower bits before being output. In addition, one IC contains counters for two channels, hence it selects one of four kinds of data and outputs it from the data output terminal. This selection is performed by the control logic circuit in the IC.

The functions of the input/output terminals of the clock counter are as follows.

Pin 23 CS1 : Chip select input
Pin 21 CS2 : Chip select input
Pin 22 OE : Output enable input
Pin 20 A/B : Data latch A/B select input

INPUTS					OUTPUTS
CS1	CS2	OE	A/B	L/H	D7−D0
0	X	X	X	X	HI−Z
1	0	0	0	0	CH−A LOWER BYTE
1	0	0	0	1	CH−A UPPER BYTE
1	0	0	1	0	CH−B LOWER BYTE
1	0	0	1	1	CH−B UPPER BYTE
X	1	X	X	X	HI−Z
X	X	1	X	X	HI−Z

Pin 19 L/H : Lower/upper data latch select input
Pin 10 OUT 16 : 1/16 frequency divided clock output
Pin 11 OUT 256 : 1/256 frequency divided clock output

(7) Timer counters (SV-90 board)

Timer counters ICN12, N14, N15, N17, and N19 use CMOS IC μPD71054. These timer counters are used for measuring speed and phase in the servo system. Each timer counter consists of the internal control circuit and three 16-bit counters. The 16-bit counter's functions, such as data presetting, data read-out, and operating mode assignment, are controlled by the CPU.
Each timer counter can operate in one of six modes, modes 0 to mode 5. In this unit, modes 0, 1, 2, 3, and 5 are used to perform the following eight measurements.

① Capstan FG count
(PTC-4 ICN15 : Channel 0/mode 0)
Here, the tape travel distance is measured. The condition of the channel 0/mode 0 input/output terminals of ICN15 is as follows.

GATE0 input (pin 11) : Level "H"
CLK0 input (pin 9) : Capstan 4FG (from pin 5 of ICA5)
OUT0 output (pin 10) : Not connected
Preset value : FFH

② Capstan prescaler
(PTC-4 ICN15 : Channel 1/mode 1)
The capstan speed which varies between −1 and +3 times normal speed, that is, the period of capstan FG, is measured at channel 2 of ICN14. At the capstan prescaler, a window which is equivalent to an integral multiple wavelength of capstan FG is applied to channel 2 of ICN14 to prevent overflow when measuring capstan FG and also to improve the measuring accuracy. The condition of the ICN15 channel 1/mode 1 input/output terminals is as follows.

GATE1 input (pin 14) : $\overline{\text{HCPRTR}}$ (speed measuring request signal)
CLK1 input (pin 15) : Capstan 2 FG (from pin 9 of ICA5)
OUT1 output (pin 13) : To pin 15 (LATCH B) and pin 16 (START B) of ICN8, and pin 16 (GATE 2) of ICN14

③ Capstan FG period measurement
(PTC-2 ICN14 : Channel 2/mode 0)
Here, the width of the window from the capstan prescaler is measured and the period of capstan FG calculated. The condition of the channel 2/mode 0 input/output terminals of ICN14 is as follows.

GATE2 input (pin 16) :	Capstan prescaler (from pin 13 of ICN15)
CLK2 input (pin 18) :	230.4 kHz clock (from pin 4 of ICM14)
OUT2 output (pin 17) :	Connected to ground
Preset value :	FFFFH

④ Capstan 2FG monostable multivibrator
(PTC-4 ICN15 : Channel 2/mode 1)
The output from pin 17 (OUT2) of ICN15 is used as a constant current supply control signal for the trapezoidal wave generator circuit of the capstan analog velocity loop. Pin 17 is triggered by capstan 2FG which is input to pin 16 (GATE2), and outputs pulses of approx. 96% (approx. 270 μsec) of the width of normal speed pulses. The condition of the channel 2/mode 1 input and output terminals of ICN15 is as follows.

GATE2 input (pin 16) :	Capstan 2FG (from pin 9 of ICA5)
CLK2 input (pin 18) :	7.3728 MHz clock (from pin 11 of ICM14)
OUT2 output (pin 17) :	Capstan analog velocity loop (to pin 4 of ICB5)
Preset value :	Depends on the adjustment value of the capstan velocity loop.

⑤ PG delay 1 (PTC-3 ICN12 : Channel 0/mode 5)
The delay of drum PG (preset value) is varied in steps of one wavelength of drum FG-B (approx. 220 μsec at the regular speed). The condition of the channel 0/mode 5 input and output terminals of INC12 is as follows.

GATE0 input (pin 11) :	Drum PG (from the CD-36 board)
CLK0 input (pin 9) :	Drum FG-B (from pin 12 of ICC4)
OUT0 output (pin 10) :	PG delay 2 (to pin 14 of ICN12)
Preset value :	Depends on the PG delay adjustment

⑥ PG delay 2 (PTC-3 ICN12 : Channel 1/mode 1)
The delay of drum PG which has been adjusted by the previously output PG delay 1 is accurately adjusted in 271 nsec steps. The condition of the channel 1/mode 1 input and output terminals of ICN12 is as follows.

GATE1 input (pin 14) :	PG delay 2 (from pin 10 of ICN12)
CLK1 input (pin 15) :	3.6864 MHz clock (from pin 10 of ICM14)
OUT1 output (pin 13) :	PG pulse (to pin 13 of ICN9 and pin 24 of ICG13)
Preset value :	Depends on PG delay adjustment

⑦ Tracking delay (PTC-2 ICN14 : Channel 0/mode 5)
The REF V signal is delayed in order to adjust the phase of the CTL signal. In the playback mode when the tracking control is pushed in (fixed), or in the recording mode, the delay is fixed at 1/2V. In the playback mode when the tracking control is pulled out (variable condition), the delay varies within the range 1/2V±1/4V according to the condition of the tracking control. The condition of the channel 0/mode 5 input and output terminals for ICN14 is as follows.

GATE0 input (pin 11) :	REF V (from pin 5 of ICJ5)
CLK0 input (pin 9) :	1.8432 MHz (from pin 9 of ICM14)
OUT0 output (pin 10) :	Tracking delay (to pin 14 of ICN14 and pin 1 of ICL8)

⑧ CTL REF clock generation
(PTC-2 ICN14 : Channel 1/mode 2)
The clock generator is reset by the CTL phase pulses input to the GATE0 terminal, and generates 19.2 kHz clock pulses. The generated clock pulses are used in the CF marker generator and the PB CTL phase measuring circuit. The condition of the channel 1/mode 2 input and output terminals of ICN14 is as follows.

GATE1 input (pin 14) :	Channel 0 (from pin 10 of ICN14)
CLK1 input (pin 15) :	1.8432 MHz (from pin 9 of ICM14)
OUT1 output (pin 13) :	CTL REF clock (to pin 10 of ICK9)

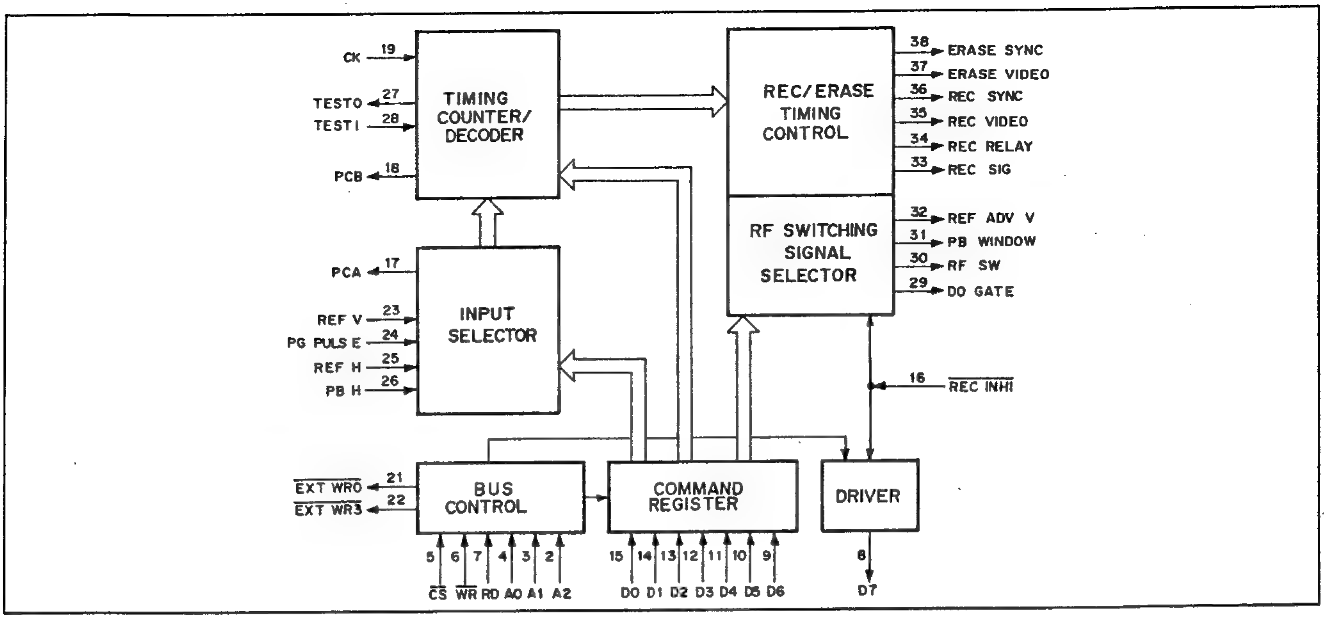


Fig. 4-6-5. Video Head Switching Logic (ICG13/SV-90)

(8) Video head switching logic (SV-90 board)

The video logic timing signals such as REC VIDEO, ERASE SYNC, and RF SW, are generated in ICG13 (CF77049N) on the SV-90 board.
The timing counter/decoder in ICG13 operate based on REF V (pin 23), PG pulse (pin 24), REF H (pin 25), and PB H (pin 26). Mode commands for the recording mode and head select are input to the command register in ICG13 from the main CPU via the data bus. The REC/ERASE timing controller and RF switching signal select circuit in ICG13 are controlled according to the control timing of ICG13 and also the mode command from the main CPU (ICK19).

(9) Reference pulse generator (SV-90 board)

This circuit generates the REF V signal and REF2 signal based on the SEL FRAME signal supplied from the RD-6 board (RD-7 board for the PS model), and also generates the REF4 and REF8 signals using the SEL CF signal.
The channel 1 of the ICL12 interval timer operates in mode 3, and outputs the 50% duty V×128 pulses from pin 13. ICK14 and ICJ10 divides the 128V pulses by 1/128, resulting in the REF V signal. In addition, the REF2, REF4, and REF8 signals are obtained by frequency dividing REF V in ICJ10.
The SEL FRAME signal supplied by the RD board and the REF 2 signal obtained by frequency dividing the 128V pulses output from ICL12 are synchronized as shown below.

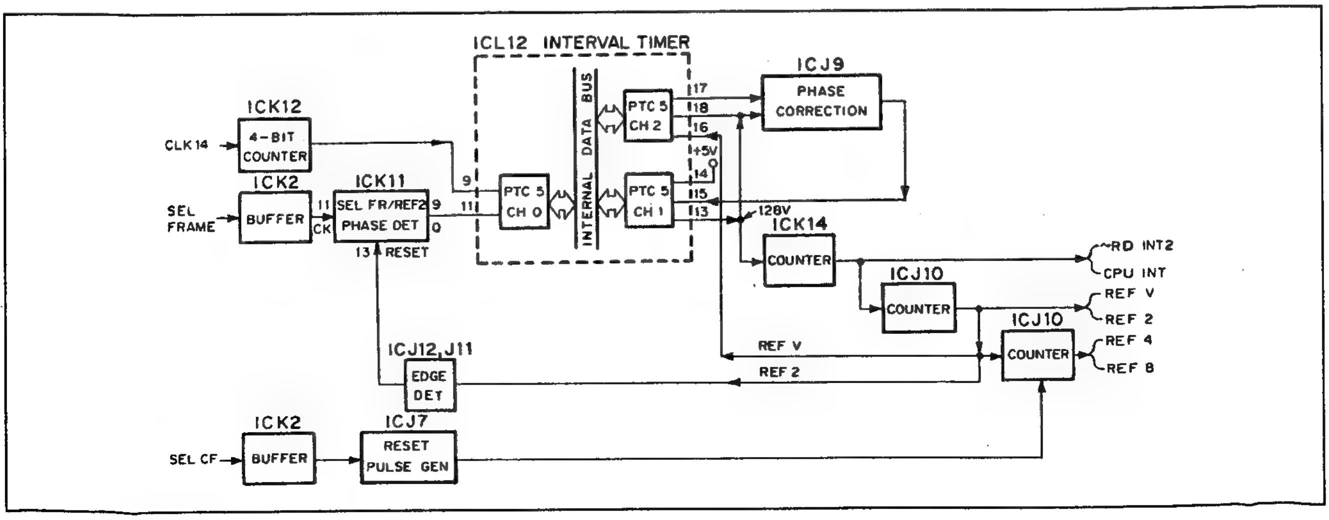


Fig. 4-6-6. Reference Pulse Generator (SV-90)

The SEL FRAME signal is input to pin 11 (clock terminal) of D flip-flop ICK11 via buffer ICK2. The REF2 signal is supplied to the reset terminal of ICK11 via the edge detection circuit consisting of NAND gate ICJ11 and latch ICJ12. The $\overline{\text{HREFMR}}$ signal output from pin 14 of address decoder ICK4 is input to pin 4 (set terminal) of ICK11, causing pin 12 (data input terminal) of ICK11 to be set to "H" level. As a result, a pulse of width equal to the period from the rising edge of the clock input to the rising edge of the reset input, that is, the phase difference between the SEL FRAME signal and the REF2 signal, is output from pin 9 (Q output terminal) of ICK11. The pulse width corresponding to the phase difference is measured at channel 0 of ICL12. In order to increase measuring accuracy, CLK14 (14.7456 MHz) is used as a clock in ICL12. In order to obtain 20-bit resolution, the lower 4 bits are measured by the 4-bit counter ICK12, and the upper 16 bits are measured by the 16-bit counter in ICL12. The measured phase data is applied to ICL12, and channel 1 of ICL12 is operated in mode 3, causing a 50% duty clock of frequency V×128 to be generated. The generated 128V clock is frequency divided by counters ICK14 and J10, resulting in $\overline{\text{RD INT2}}$ of frequency V/32, CPU INT of frequency V/4, REF V of frequency V, and REF2 of frequency 2V. Counter ICJ10 which uses REF2 as the clock is reset by the SEL CF signal supplied from the RD board, and generates the REF4 and REF8 signals.
Channel 2 of ICL12, latch ICJ9 and NOR gate ICH10 operate as a phase adjustment circuit for the 128V signal. The clock input to the 128V signal generator circuit (channel 1 of ICL12) is gated by ICH10 and the number of clock pulses controlled, thus controlling the phase of the 128V signal.

(10) Sub CPU (SV-90 board)

The sub CPU (ICB15 : μPD78C10) is an 8-bit CPU which contains an A/D converter. It operates on the same 7.3728 MHz clock as that of the main CPU (ICK19). The sub CPU contains a 256 byte RAM. Also, an external 8k byte ROM (ICE15) and a 2k byte RAM (ICE16) are connected to it. RAM ICE16 is used as a common memory for communication with the main CPU.
Port A (PA7 to PA0) and port B (PB7 to PB0) of the sub CPU are general purpose input/output ports. Inputs and outputs can be specified in bit units. Port C (PC7 to PC0) functions as a general purpose input /output port, and can also be used as a control signal. In this unit, port C is used as an output port and also as a serial communication port. Port D (PD7 to PD0) is used as a multiplex address bus for an external memory. Port F (PF7 to PF0) is used as an input/output port and also as an address bus.
The data terminal (D7 to D0) of the RAM (ICE16) is connected to the data bus of the main CPU (ICK19) and the data bus of the sub CPU via bi-directional bus transceivers ICD17 and ICD16.
The switchover between ICD16 and ICD17 is performed by the V/4 rate CPU INT signal output from pin 5 of ICJ12, thus preventing a collision between the data buses of the main CPU and the sub CPU.
The address bus and the control signal of the RAM (ICE16) are selected by selector ICD13, ICE17 and ICF17. Also, switching between ICD13, ICE17 and ICF17 is performed by the CPU INT signal in the same way as the data bus.

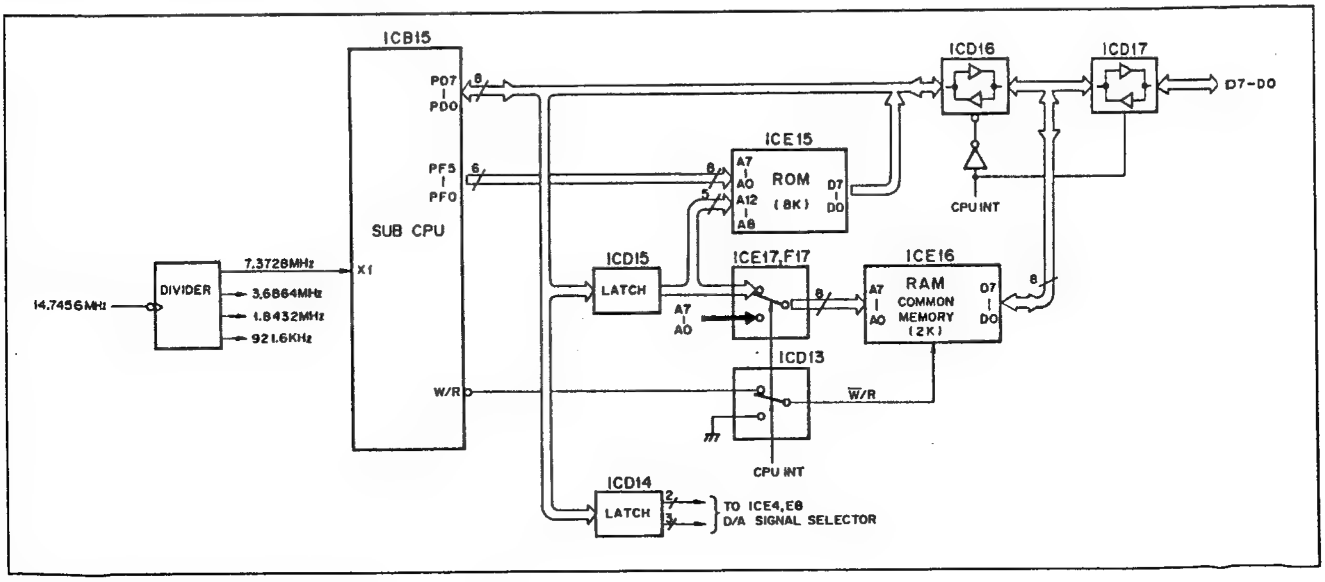


Fig. 4-6-7. Sub CPU (SV-90)

(11) D/A converter (SV-90 board)

The upper 12 bits of the 16-bit data processed in sub CPU ICB15 are supplied to the D/A converter (ICA16) from PB7 to PB0 and PA7 to PA4 of the sub CPU. The offset level of the analog signal output from ICA16 is adjusted by RV2 and the conversion gain adjusted by RV3. The resulting signal is current /voltage converted by IC11, and output to the analog switcher ICE4 and ICE8 in the next stage.
The analog signal which is output from the D/A converter is used not only as a motor driver signal but also as an offset compensation signal and a gain control signal. These analog data are stored in non-volatile memory IC1 on the mother board as data which indicate the mechanical characteristics of the tape transport system, and are read out when the CPU is initialized. After replacing a part such as the tension arm, change the adjustment data saved in the non-volatile memory IC1, using "T17. MAINTENANCE" of the setup menu.

4-6-3. Drum Servo System (SV-90 Board)

Each time the drum makes one revolution, 76 pulses of the FG (Frequency Generator) signal and one pulse of the PG (Pulse Generator) signal are generated. The 2-phase FG signals (DRUM FGA and DRUM FGB) are used for detecting the rotational speed and direction of the drum, and the DRUM PG signal is used for detecting the rotating phase of the drum.
The DRUM FGA and DRUM FGB signals which are supplied to the SV-90 board are converted to TTL level by ICC1, D1, and C4, and input to ICA5. ICA5 outputs the DIR signal which indicates the direction of rotation of the drum, and also the 2FG signal which has a frequency of twice that of the FG signal. The DIR signal is output from pin 3 of ICA5, then supplied to pin 64 (PB0) of the I/O expander (ICG15). The 2FG signal which is obtained by EX-OR gating in ICA5 is supplied from pin 15 of ICA5 to pin 16 (GATE2) of ICN12. When the CPU starts speed measurement, pulses of width 105 μ sec (388 clocks)

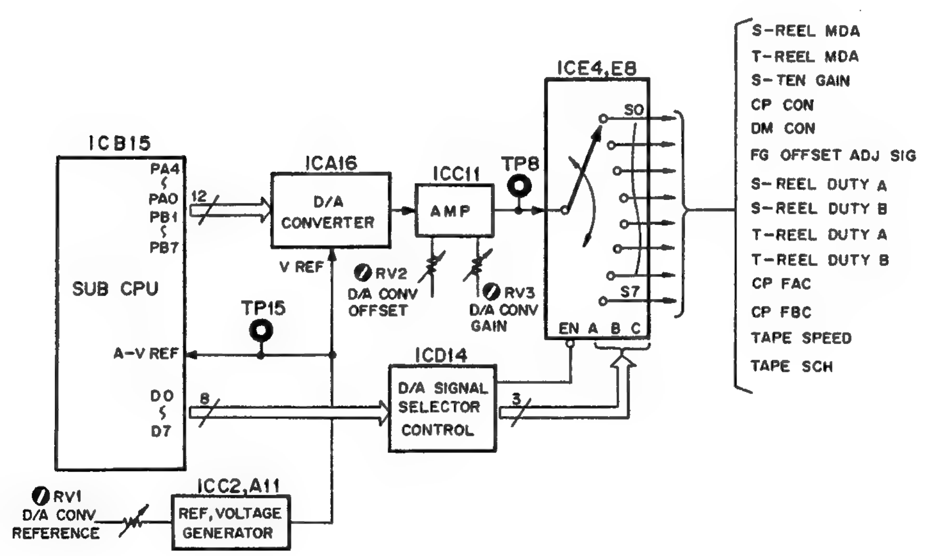


Fig. 4-6-8. D/A Converter (SV-90)

are output to pin 17 of ICN12. These pulses are used in the T/V converter circuit in the analog servo system.
The analog servo system converts the pulse width of the FG signal into a voltage, in the following way: The 2FG signal output from pin 15 of ICA2 and also the output of pin 17 (OUT2) of ICN12 are AND-gated in ICB5. The pulse width of the OUT2 signal from pin 17 is 105 μsec. This is equivalent to about 96% of the pulse width (109.6 μ sec) corresponding to normal speed. A pulse of width equal to the difference between the widths of both pulses is output from pin 3 of AND gate ICB5, and C14 is charged by constant current source Q3 for exactly the duration of this pulse. The voltage to which C14 is charged is applied to sample hold ICB7 in the next stage. The DRUM FGB signal is delayed by ICC5, ICB6 and ICB5 and input to pin 8 of ICB7.
ICB7 sample-holds the stabilized DC voltage obtained after C14 is charged rather than the voltage obtained while it is still charging. In this way, the width of the sample pulse can be increased, and a stable output obtained. C14 is charged each time a pulse of the double frequency FG signal is input, and immediately after ICB7 samples the charge voltage, C14 is discharged by analog switcher ICC7. Diode D5 operates as a limiter to limit the charging voltage of C14 to a maximum of +5V. The analog velocity error compensation voltage which was sample-held by ICB7 is added to the digital servo signal (DMCON), and output from pin 7 of ICD7. Analog switch ICC7 selects either the digital servo signal to which the analog velocity error compensation voltage has been added, or the digital servo signal to which the compensation voltage has not been added (DMCON). The selected signal is amplified by operational amplifier ICD7, then supplied to the drum drive circuit of the CD-36 board as the DRUM MDA signal. ICC6 is a circuit which forcibly stops the drum motor while the analog velocity loop is operating, to prevent a negative voltage corresponding to a reverse command from being output as a DRUM MDA signal.
Each time the upper drum makes one revolution, a single pulse of the PG signal is output from the head drum. This pulse is converted to TTL level in voltage comparator IC16 on the CD-36 board, then supplied to the SV-90 board. The DRUM PG signal is generated when the magnet installed in the upper drum passes over the detector device in the lower drum. The magnet is installed slightly ahead (in terms of phase) of the R/P head for the video channel. The generated DRUM PG signal is electrically delayed to align it with the V phase of the R/P head output signal for the video channel. If the upper drum is replaced, adjust the delay of the DRUM PG signal from the control panel, using "T17. MAINTENANCE" of the test menu.
The SV-90 board applies a phase servo which maintains the correct phase relation between the REF V signal and the Delayed PG signal (consists of a delayed DRUM PG signal).

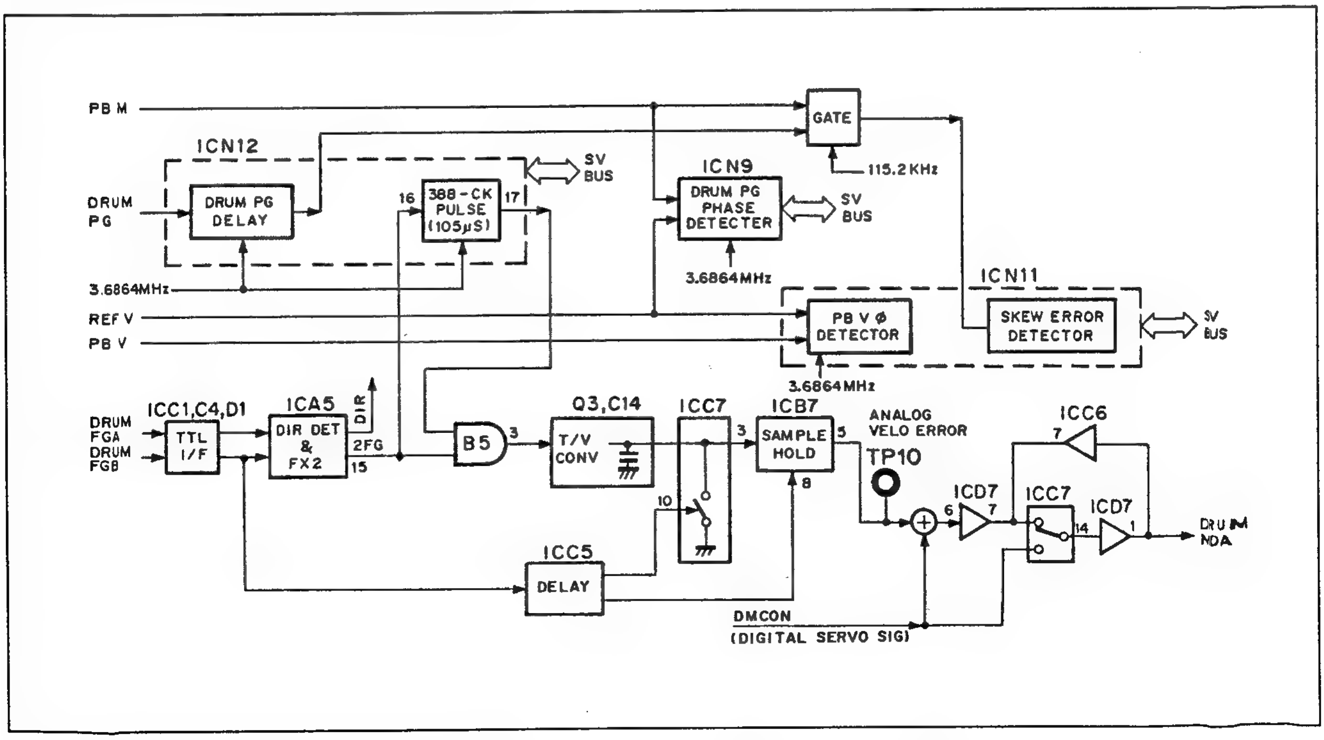


Fig. 4-6-9. Drum Servo System (SV-90)

4-6-4. Capstan Servo System (SV-90 Board)

The capstan servo has the following three purposes.

1. Fixing the tape speed during recording.
2. Aligning the phases of the CTL signal generated from the REF V signal, and the PB CTL signal played back from the tape, to ensure tracking during normal speed playback.
3. Controlling the tape speed during variable playback (−1 to +3 times normal speed).

The above control takes place when the pinch roller is pressed against the capstan (ON). Like the drum servo, the capstan servo is divided into a digital servo area and also analog velocity loop. The analog velocity loop is used in the PLAY, REC, and P-PLAY modes, and the digital servo is used in the variable mode. In the ultra low speed variable mode, the interval between FG pulses increases, hence the FG pulses are A/D converted in the sub CPU, utilizing the fact that the FG signal is a sine wave, and from the resulting data the rotational speed is calculated to a greater degree of precision.

The 2-phase FG signals, of which 96 pulses are output each time the motor makes one revolution, pass through operational amplifiers ICA1 and B1, and buffer amplifier ICB4, then to signal selectors ICF11 and F10 for the D/A converter of sub CPU ICB15.

The DC offset compensation voltages (CPFAC and CPFBC) of the motor FG output are applied to the FG input terminals of ICA1 and ICB1. The offset compensation voltage data is stored in the non-volatile memory (IC1) on the mother board, and is supplied via sub CPU ICB15 and D/A converter ICA16. The outputs of operational amplifiers ICA1 and B1 are supplied to voltage comparator ICA4. FGA and FGB which are output from ICA4 are supplied to the motor rotational direction detection circuit (ICA5).

The following signals are output from ICA5.

• DIR (pin 6):

This signal indicates the direction of rotation of the motor. It is supplied to port PB1 of I/O expander ICG15.

• 2FG (pin 9):

This signal, which is obtained from the EX-OR gate of FGA and FGB is twice the frequency of the FG signal. It is supplied to channels 1 and 2 of PTC4/ICN15 and also the analog velocity loop.

• 4FG (pin 5):

This signal is obtained by sampling FGA and FGB with the 921.6 kHz clock input to pin 7, then EX-OR-gating them, and outputting pulses of one clock width at each rising and falling edge. Consequently, the frequency of this signal is four times that of FG. This 4FG pulse is supplied to channel 0 of PTC4/ICN15.

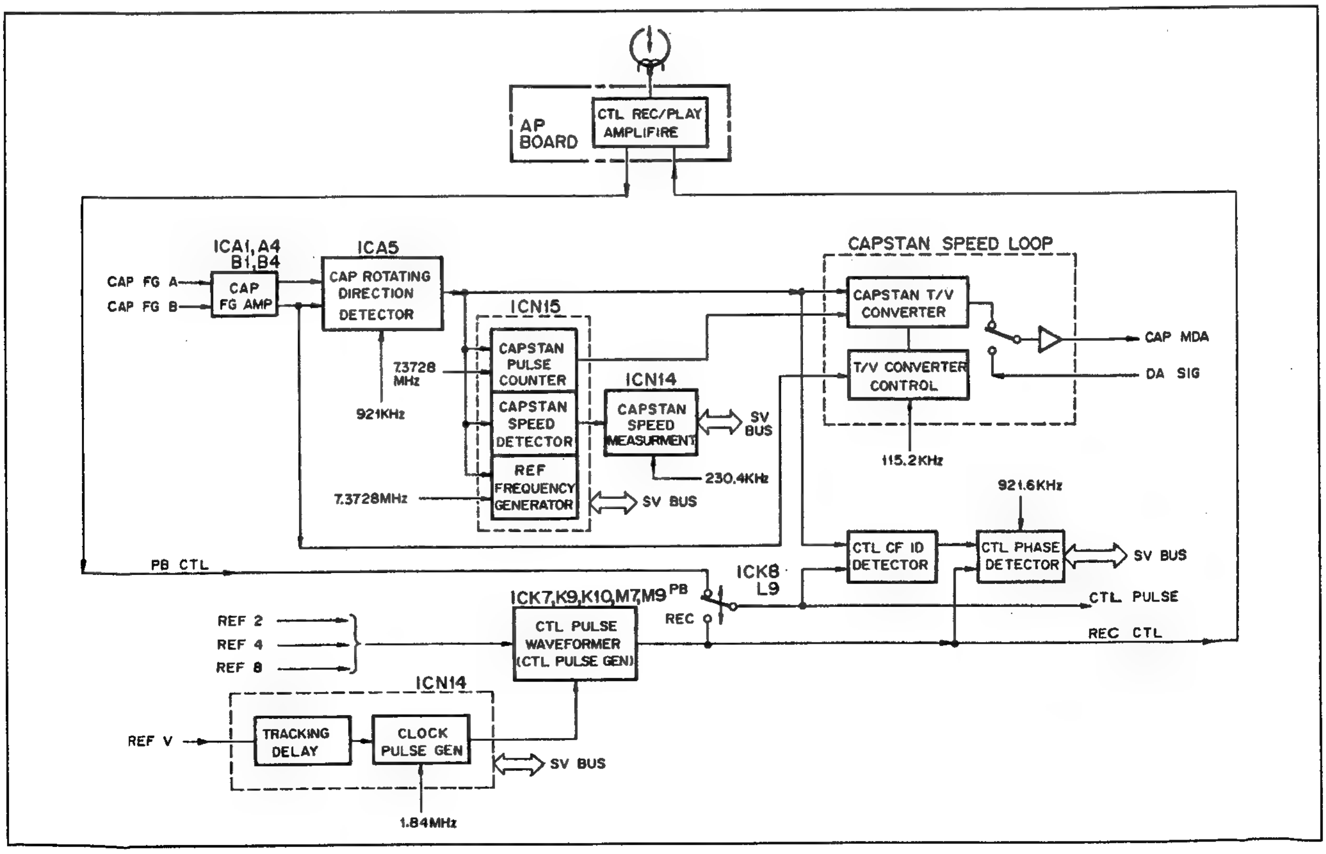


Fig. 4-6-10. Capstan Servo (SV-90)

4-6-5. CTL Processing System (SV-90 Board)

The CTL signal is recorded and played back by the stationary head. The recording amplifier and playback amplifier are located on the AP-15 board. The circuit which detects the color framing data and CTL phase from the CTL signal is located on the SV-90 board.

(1) CTL pulse generator (SV-90 board)

The CTL signal is obtained by delaying the REF2 signal created from the servo reference signal by the specified phase then inserting a color frame marker into it.
The REF2 signal is input to latch ICK10 together with the REF4 signal and REF8 signal which contain the color frame information. The time difference (tracking delay) between the input data and output data of latch ICK10 depends upon the timing of the rising edge of the clock signal input to pin 9. In other words, the CTL phase is determined by the phase of the clock signal.
The clock signal is generated at channel 0 of PTC-2/ICN14.The phase of the clock signal is determined by delaying the phase of REF V input to pin 11 (GATE 0) of ICN14 by an interval determined by the CPU.
The counter in ICN14 is preset by CPU ICB15. This preset value, that is, the clock delay, is fixed during recording, and depends on the setting of the tracking control on the level control panel during playback.
The adjustment value set by the tracking control, that is, the preset value, is A/D converted by sub CPU ICB15. The A/D converted preset value is processed by software, then preset in the counter used in channel 0 of ICN14.

(2) Color frame marker generator (SV-90 board)

The color frame marker is a signal which indicates the phase relation between the sub carrier of the recording signal and the H sync signal. If the phase relationship between SC and H changes, the continuity of the sub carrier will be lost, that is, color framing will get out of step, which may cause misoperation of the time base corrector.
Color frame detection is performed by the RD board. The SEL CF signal which indicates the result of detection is input to the SV-90 board. At the SV-90 board, reference pulse signals REF4 and REF8 which contain color frame data are generated based on the CF signal, and are latched together with REF2 by ICK10. The REF2 and REF4 outputs from latch ICK10 are AND-gated by ICK7 to become a color frame marker window for an NTSC signal. ICK9, ICL9 and ICM9 constitute a marker pulse generator circuit. The output from this circuit is AND-gated with REF2 and REF4 by ICK7, resulting in a color frame marker signal for an NTSC signal at pin 12 of ICK7. This color frame marker is input to pin 11 of ICK7, then gated by the REF8 signal output from pin 7 of ICK10, resulting in an 8-field sequence color frame marker signal for a PAL signal.
Channel 1 of ICN14 is a clock generator used for marker pulse generation. The REF V signal which is delayed in channel 0 is input to the GATE 1 terminal, and a 19.2 kHz clock which is reset at that timing is output from OUT1. This clock is frequency divided by counter ICK9, resulting in the timing signal for the marker pulse generator circuit.

4-6-6. Reel Servo System (SV-90 Board)

The reel servo system performs control to obtain a stable tape tension regardless of the mode in which the VTR is operated. The reel servo system uses the maximum software area for the servo system, and performs the following processing using the CPU.

1. Detection and control of tape winding diameter.
2. Tape speed control from very slow, such as in the JOG mode, to a maximum of 50 times normal speed, as in the SHUTTLE mode.
3. Detection and control of load fluctuations due to differences in tape length and reel diameter.

Data concerning the rotational speed and direction of rotation of the reel motor are obtained from the FG signal. The FG signal is output at the rate of 700 pulses per revolution of the reel motor, converted to TTL level at the RM-43 board, then sent to the SV-90 board.
The direction of rotation is detected by ICH6 using S and T reel FG signals. The speed of rotation of the S reel is detected by channel 0 of timer counter PTC-0/ICN17, and that of the T reel is detected by channel 1.
The T reel motor is controlled by an open loop. The data calculated by the CPU from the tape diameter and the rotational speed of the motor is D/A converted to become the T-REEL MDA signal. This signal is input to the T reel motor drive circuit on the RM-43 board, causing the T reel motor to be driven so that the tape tension is the correct value for each mode.
The S reel motor is controlled by a similar open loop to that used for the T reel motor, and also by a feedback loop which maintains the tape tension detected by the tension arm constant. The tension arm signal amplifier circuit (ICG2 and G4) also functions as a filter which removes the inherent vibration component due to the tension arm from the tension arm signal.

4-6-7. Skew Detector (SV-90 Board)

Skew is a phenomenon whereby the tape stretches or contracts due to changes in ambient temperature and tape tension during recording and playback, causing the playback time per field to vary, which in turn results in distortion at the top of the monitor screen.
The output from pin 10 (OUT 0) of PG delay 1 circuit ICN12 is supplied to ICH8, the window pulses obtained are latched in ICM10 by the PB H signal, and the output pulse width is measured in the B channel of ICN11. Although the pulse width of the PB H signal is measured, the width of the window is made 1.38 msec (21H+ α) because if only one period of H were to be measured the effect of velocity errors would become significant and also the amount of change would be very small, making measurement difficult.

4-6-8. Servo Reference Signal Generator (RD-6/RD-7 Board)

(1) Input select circuit and video amplifier (RD-6/RD-7 board)

In the servo reference section, the signals input to the VIDEO INPUT terminal and the REF VIDEO INPUT terminal of the connector panel are 0.5 Vp-p. One of these signals is selected by the "S40. SERVO REF SELECT" select menu. The selected signal is amplified by a factor of about 7 to 8 by the video amplifier in the next stage.

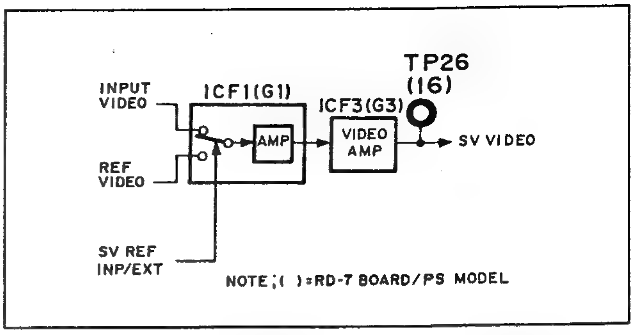


Fig. 4-6-11. Input Selector and Video Amplifier (RD-6/RD-7)

(2) Sync separator (RD-6/RD-7 board)

This circuit separates the sync signal, which is used for frame detection and SC-H phase detection, from the video signal.
The Y signal is taken off from the SV video signal (servo reference signal), which is output from the video amplifier, by a low-pass filter, and the pedestal level is clamped to 0 V by Q15 (Q3). Next, the sync tip is sample-held by ICF9 and IC2 (ICG8 and G9), and the level of the sync signal detected. The level of the detected sync signal is voltage-divided by resistors, resulting in a voltage of 1/2 the sync signal level. The sync signal is separated by comparing the Y signal, the pedestal of which is clamped to 0V, and the 1/2 sync tip level voltage in voltage comparator ICF13 (ICG10).

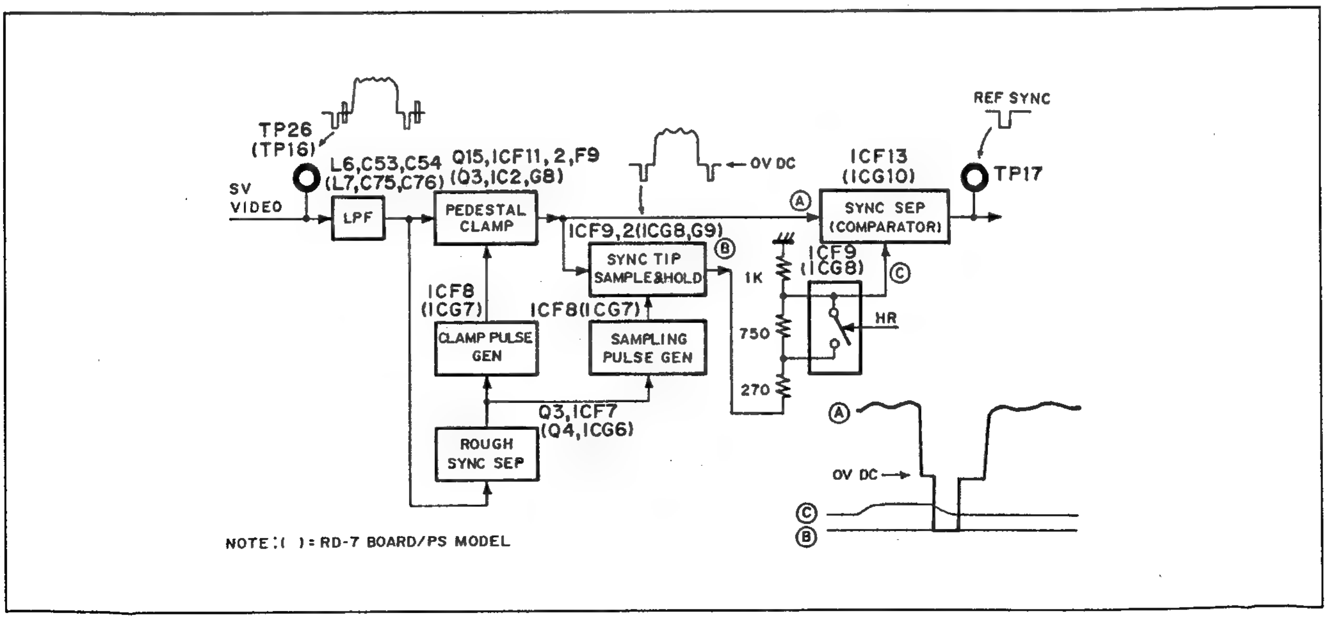


Fig. 4-6-12. Sync Separator (RD-6/RD-7)

ICF9 (ICG8) switches the voltage division ratio of the sync signal level. The voltage compared in ICF13 (ICG10) approaches the sync tip level other than at the leading edge of the sync signal, thus providing noise immunity.
ICF7 (ICG6) is a rough sync separator. Clamp pulses and sync tip sampling pulses are generated from the sync signals generated here.

(3) Burst APC (4Fsc VCO) (RD-6/RD-7 board)

This circuit generates a continuous subcarrier locked to the burst signal, in order to detect the SC-H phase. The signal from the video amplifier is passed through a bandpass filter where the chroma component is taken off, then converted to TTL level by a zero-cross detector. The converted signal is input to PLL, resulting in a continuous 4Fsc signal which is locked to the burst signal. This signal is frequency divided by 1/4, then supplied to the SC-H phase detection circuit as a signal which indicates the SC phase.

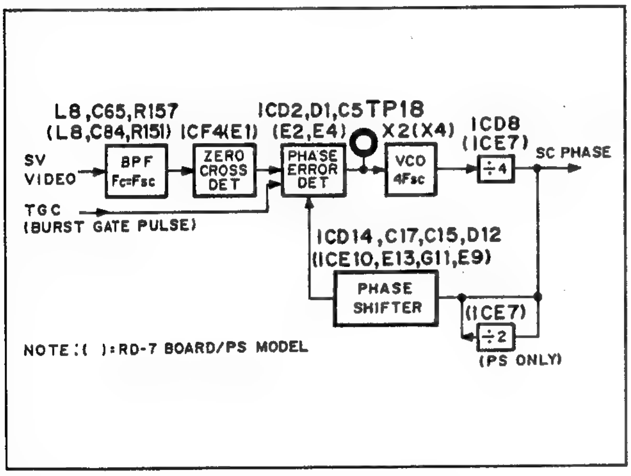


Fig. 4-6-13. Burst APC (RD-6/RD-7)

(4) Field 1/2 detection: NTSC model (RD-6 board)

When the REF SYNC signal is input to pin 15 (EXT SYNC terminal) of ICD9 (CX7903), the VR (REF V) signal is output from pin 7, and the HR (REF H) signal is output from pin 6. The VR signal is output at the fall timing of the 1st pulse in the vertical sync pulse interval. The VR signal is frequency divided by 2, resulting in the REF FRAME signal. Since the REF FRAME signal must be "L" in the 1st field interval, field 1/field 2 is detected and the detector output resets the frequency divider. Field 1/field 2 detection takes place utilizing the fact that the phase relationship between the VR signal and the HR signals in the 1st and 2nd fields are different.

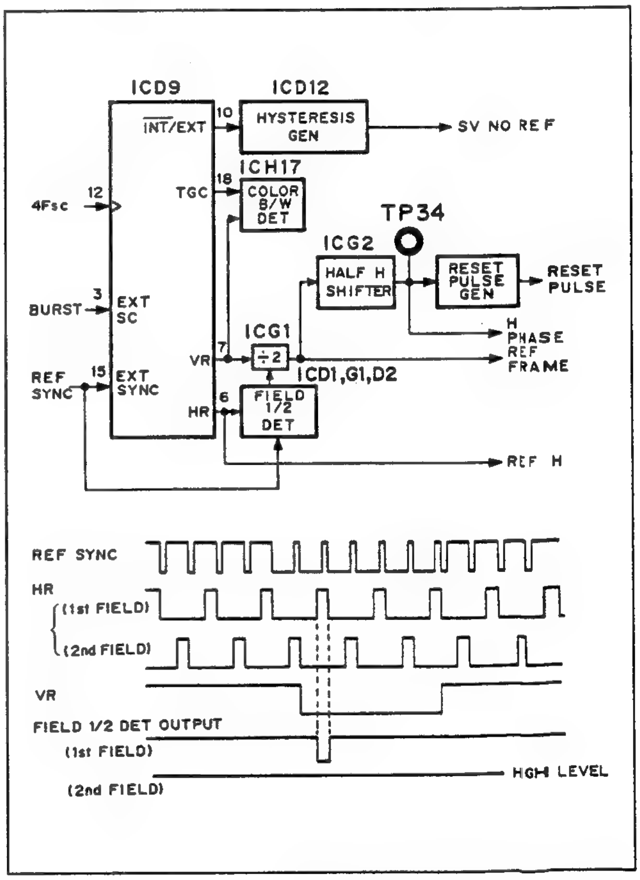


Fig. 4-6-14. Field 1/2 Detector: NTSC Model (RD-6)

(5) Field 1/2, 1/3 detection : PS model (RD-7 board)

Field 1/field 2 detection takes place in a similar way to that of the NTSC model. In the PS model, the REF FRAME signal obtained by field 1/field 2 detection is once again frequency divided by 2, and field 1/field 3 detected. The field 1/3 detection formats for PAL and SECAM are different. In the case of PAL, the field is judged according to whether or not the burst signal of line 6 exists (if there is a burst signal, the field is field 3) ; in the case of SECAM, detection, the field is judged according to whether or not the ID signal of line 8 is DR or DB (if it is DR, the field is field 3).

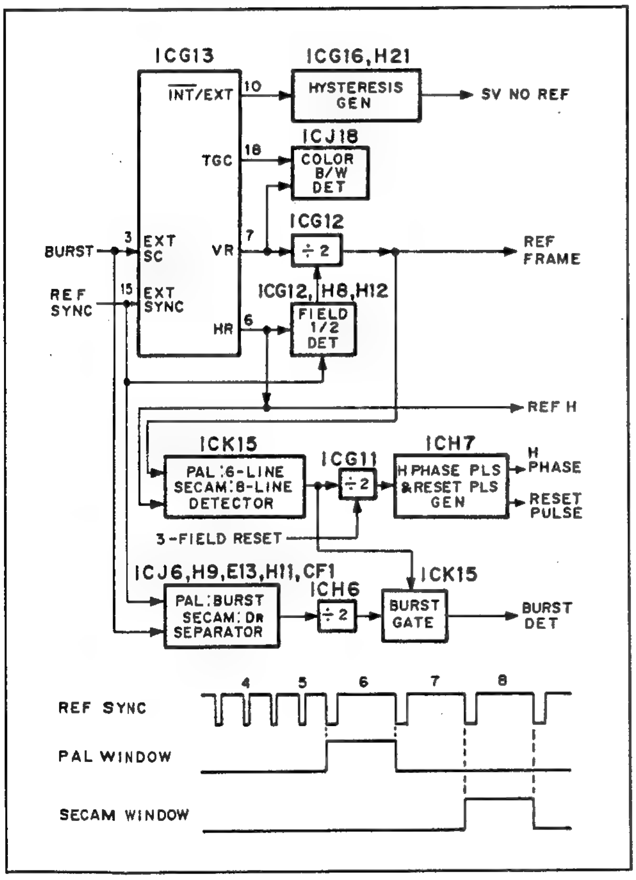


Fig. 4-6-15. Field 1/2 and 1/3 Detectors : PS Model (RD-7)

(6) SC-H phase detection (RD-6/RD-7 board)

The SC-H phase is detected by measuring the phase difference between the falling edge of the H PHASE signal and the SC PHASE signal. The H PHASE signal is inverted at the following timing each field (or every second field in the case of the PAL format).

- NTSC : Fall of the 3rd vertical sync pulse
- PAL : Fall of H sync of line 9

SC PHASE is the output signal of burst APC. The pulses of this signal are generated at the same frequency as the sub carrier.

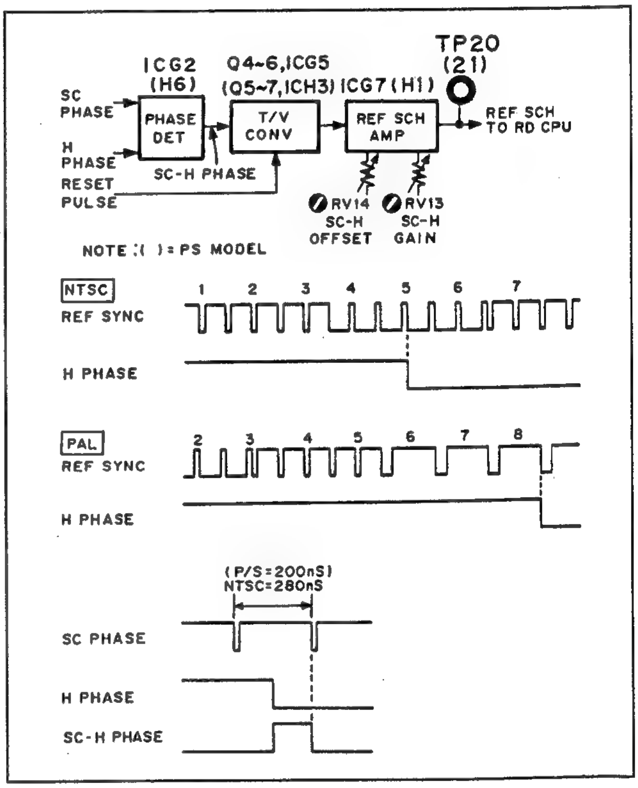


Fig. 4-6-16. SC-H Phase Detector (RD-6/RD-7)

The phase difference between H PHASE and SC PHASE (SC-H PHASE signal) detected by ICG2 (ICH6) is T/V converted and adjusted so that the voltage is 0V at −180° and 5V at 180°, where the period of the sub carrier is defined as 360°. In the NTSC signal, if the SC-H phase of field 1 is 0°, the phase of field 3 will be 180° (in the PAL signal, the phase of field 5 is 180°), hence the voltage of the waveform at this time will be 2.5V for fields 1 and 2 (or fields 1, 2, 3, and 4 in the case of the PAL signal), and 0V or 5V for fields 3 and 4 (or fields 5, 6, 7, and 8 in the case of the PAL signal). By inputting a reference signal so that the SC-H phase of field 1 becomes 0, and carrying out the abovementioned adjustment, a voltage waveform which always matches the SC-H phase will be obtained.

This waveform (REF SCH) is input to the analog port of the CPU and the voltage measured and displayed on the SC-H meter on the meter panel. At the same time, field 1/field 3 detection (or field 1/field 5 detection in the case of the PAL signal) takes place.

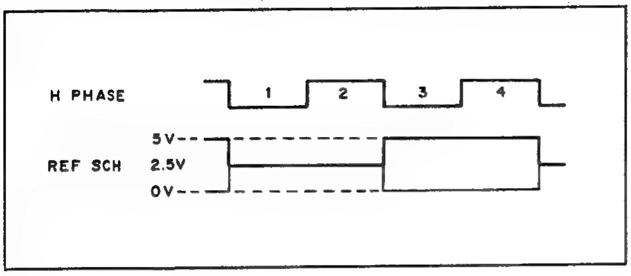


Fig. 4-6-17. SC-H Phase T/V Conversion Level: NTSC (RD-6)

The 4-field sequence of the NTSC signal, and the 8-field sequence of the PAL signal, are prescribed as follows.

NTSC signal (U.S. EIA RS-170A)
The field at which the phase of the subcarrier at the center of the falling edge of H sync of line 10 is 0° is defined as field 1, and a phase difference of up to ±40° is allowed.

PAL signal
The field at which the phase of the subcarrier which has the same phase as the U axis color signal at the center of the falling edge of H sync of line 1 is 0° is defined as field 1, and a phase difference of up to ±90° is allowed.

In both the NTSC and PAL signals, the RD board judges the field in which the SC-H phase is ±70° to be field 1, and outputs the SV CF signal. Also, the range of field 1 can be changed to "−25° to +115° " or "−125° to +25° by setting "S43. SERVO CF DET SHIFT" of the menu to either "+45 DEG" or "−45 DEG".

4-7. SYSTEM CONTROL AND TIME CODE SYSTEM

The main circuitry configuring the system control and time code system is housed on the SY-103 board and control panel. The SY-103 board has the following functions.

(a) Control of the man/machine interfaces and interfaces such as that with an editor (system control)
(b) Time code reader/generator and its control

The above circuitry operates independently. The function described in (a) is carried out by the CPU on the SY-103 board while the function in (b) is controlled by the CPU on the SV-90 board. The time code system circuitry on the SY-103 board can be considered as part of the SV-90 board.

4-7-1. System Control Circuit (SY-103 Board)

CPU ICH14 on the SY-103 board serves to receive both the control signals from the external equipment which are supplied to the REMOTE-1, 2A and 2B connectors and the button signals from the control panel, convert these signals into the VTR control signals and write the data into common RAM ICJ3 which is used for communication with the CPU on the SV-90 board. CPU ICK19 on the SV-90 board serves to decode the commands from the SY-103 board into port information for each of the boards and to transfer this information to the video/audio/TBC and other boards.

(1) CPU and its peripheral circuits (SY-103 board)

In the CPU on the SY-103 board, the internal 16-bit/external 8-bit V20 (μ PD70108D-8) is used in the minimum mode. The 64k-byte ICH11 and ICH12 are used as the external ROMs of the CPU. The 8k-byte ICH10 is used as the external RAM. The 7.3728 MHz frequency signal from ICG14 is used as the CPU clock signal.
The signal with a 14.7456 MHz frequency is divided by ICG13 and ICF14 and used for the peripheral ICs of the CPU. The signal with the 0.3072 MHz frequency in the clock signal provided is further divided down by ICF14 and ICF15 and "READY" display LED D8 is controlled. While ICF14 and ICF15 are counting, D8 blinks on and off at a frequency of 9.375 Hz (106.67 msec). If the counter reset signal from the CPU which is supplied to pins 7 and 15 of ICF15 is interrupted, D8 goes off after approximately 53.3 msec.
In order to read and write data into a slow device from the CPU, a READY signal is generated by ICG12 so that the CPU is made to wait for the equivalent of a clock cycle and this signal is supplied to the RDY1 pin of ICG14. The waiting request signal is supplied to the RDY2 pin of ICG14. In order for the CPU to be made to wait, RDY2 must be off (low level).

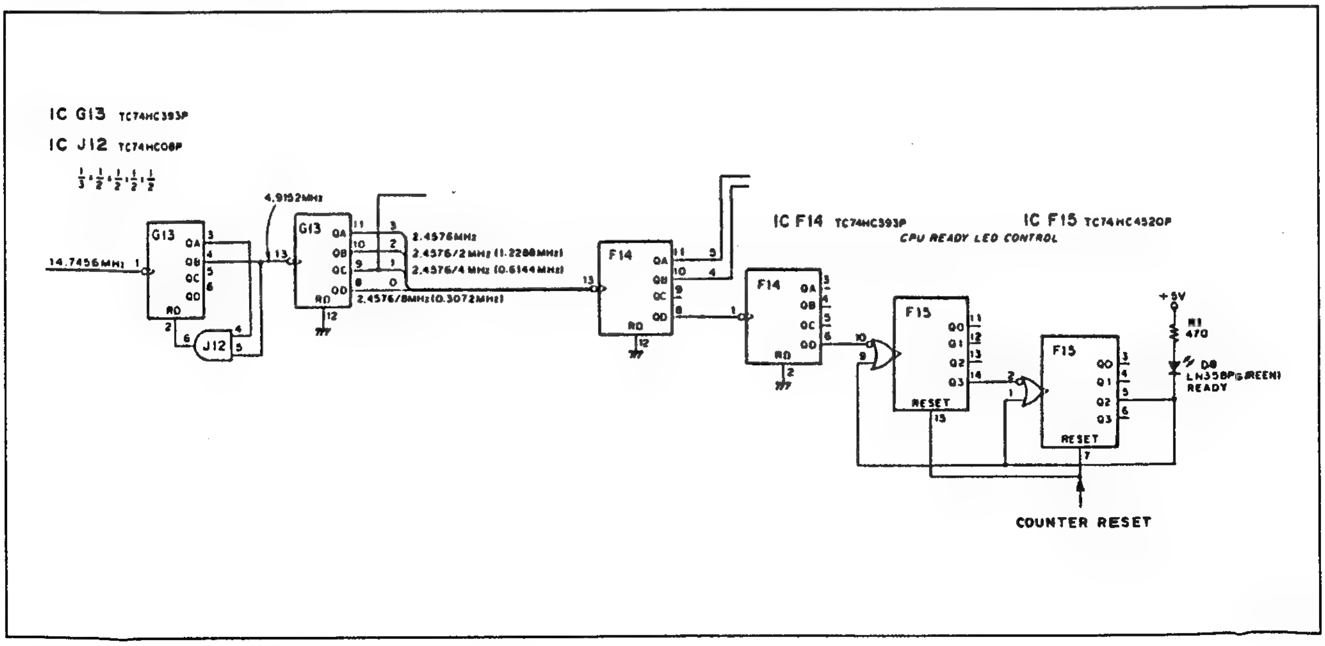


Fig. 4-7-1. Clock Frequency Divider (SY-103)

The timing operations shown in Fig. 4-7-2 are described in detail below.

(a) Since the RDY2 pin (pin 6) of ICG14 is on (high level), the READY pin (pin 5) is also set high and there is no CPU transition to the waiting operation. The CPU enters the READY state only when pins RDY1 and RDY2 are both low.
(b) The RDY2 pin is off (low level) and so READY control is enforced.
(c) The READY signal is now transferred to the CPU. At the timing of the clock T2 fall edge, the CPU checks whether the waiting request is present.
(d) RDY1 is reset after a half clock cycle has elapsed and ICG14 is advised of the termination of READY control. RDY1 is used with each CPU cycle in order to control the waiting which is equivalent to a clock cycle. At the timing of the clock Tw rising edge, the CPU judges whether it should exit or not from the waiting status.
(e) It is now detected that RDY1 is set to high level and the READY status is set on after a half clock cycle.

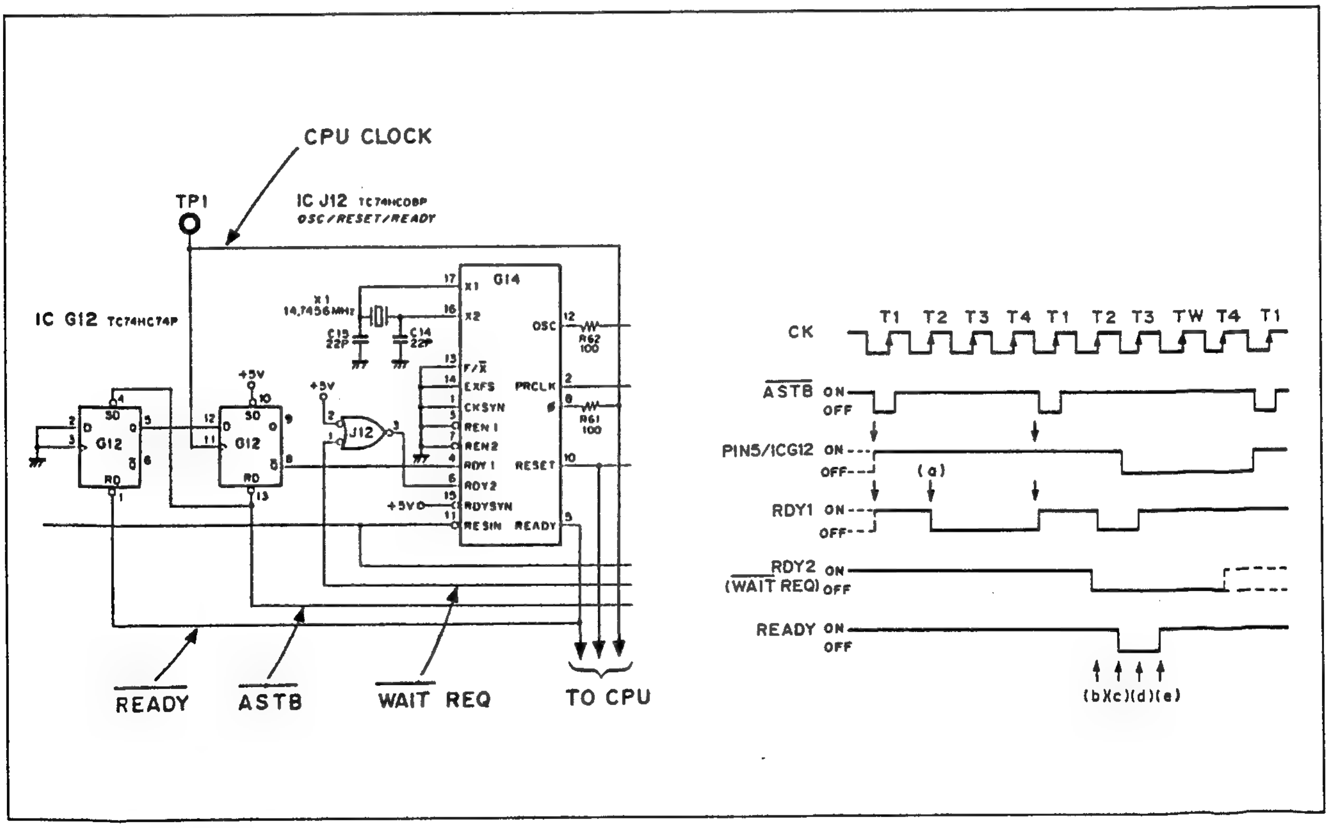


Fig. 4-7-2. Waiting Control Circuit (SY-103)

(2) Address decoder (SY-103 board)

The address decoder is composed of ICK9, K10, K11, K12, J10 and J12. Table 4-7-1 shows the addresses of the various devices mounted on the SY-103 board. The ICH12 (ROM0) addresses are separated into 0000H−3FFFH and C000H−FFFFH so that the start addresses at the time of resetting and the interrupt table can be housed in the same ROM. The reason for this is that if the two sets of addresses are separated in the two ROMs, then the probability that the CPU will operate out of control when a ROM error is detected is doubled, and difficulties arise in remedying the error.
ICH11 (ROM1) has a bank selection capability and two 16k-byte ROM areas.
ICH10 (RAM0) has an 8k-byte memory size. The contents of this RAM are not backed up and all its data will be lost when the power is turned off.
ICJ3 (common RAM) also has an 8k-byte memory size although in actual fact only 2k bytes of this capacity are used. The common RAM is backed up by C38 and data can be retained for at least one week.
Each of the ICH7, H8, J9, H6 and F13 CPU peripheral ICs are allocated a 1k-byte address area although the maximum address area actually used by the software is 9 bytes. Table 4-7-2 lists the peripheral IC addresses.

ADDRESS	CATEGORY	
0000H−3FFFH	ICH12 ROM0 LOWER BYTE	
4000H−7FFFH	ICH11 ROM1 BANK0	ICH11 ROM1 BANK1
8000H−9FFFH	ICH10 SELF RAM	
A000H−A7FFH	ICJ3 COMMON RAM	
A800H−ABFFH	ICH7	
AC00H−AFFFH	ICH8	
B000H−B3FFH	ICJ9	
B400H−B7FFH	ICH6	
B800H−BBFFH	NOT USED	
BC00H−BFFFH	ICF13	
C000H−FFFFH	ICH12 ROM0 HIGHER BYTE	

ADDRESS	CATEGORY
BC00H	PA0−PA7 (INPUT)
BC01H	PB0−PB7 (INPUT)
BC02H	PC0−PC7 (OUTPUT)
BC03H	PD0−PD7 (OUTPUT)
BC04H	PX0−PX3 (OUTPUT)
BC05H	REGISTER 1
BC06H	REGISTER 2
BC07H	NOT USED (DON'T USE)
BC08H	RESET START TRIGGER

Table 4-7-1. Address Map (SY-103)

REF NO.	ADDRESS	FUNCTION
ICH7 (RS-422)	A800H A801H A802H A803H	A-CH I/O DATA A-CH CONTROL REGISTER B-CH I/O DATA B-CH CONTROL REGISTER
ICH8 (COUNTER)	AC00H, AC01H AC02H, AC03H AC04H, AC05H AC06H	COUNTER-0 PRESET WORD DATA COUNTER-1 PRESET WORD DATA COUNTER-2 PRESET WORD DATA CONTROL WORD REGISTER
ICJ9 (INTERRUPT CONTROLLER)	AC00H AC01H	CONTROL REGISTER FOR A0=0 CONTROL REGISTER FOR A0=1
ICH6 (RS-232C)	B400H B401H	SERIAL I/O DATA CONTROL REGISTER
ICF13 (I/O)	BC00H−BC08H	SEE TABLE 4-7-1.

Table 4-7-2. Address Map of Peripheral CPU ICs (SY-103)

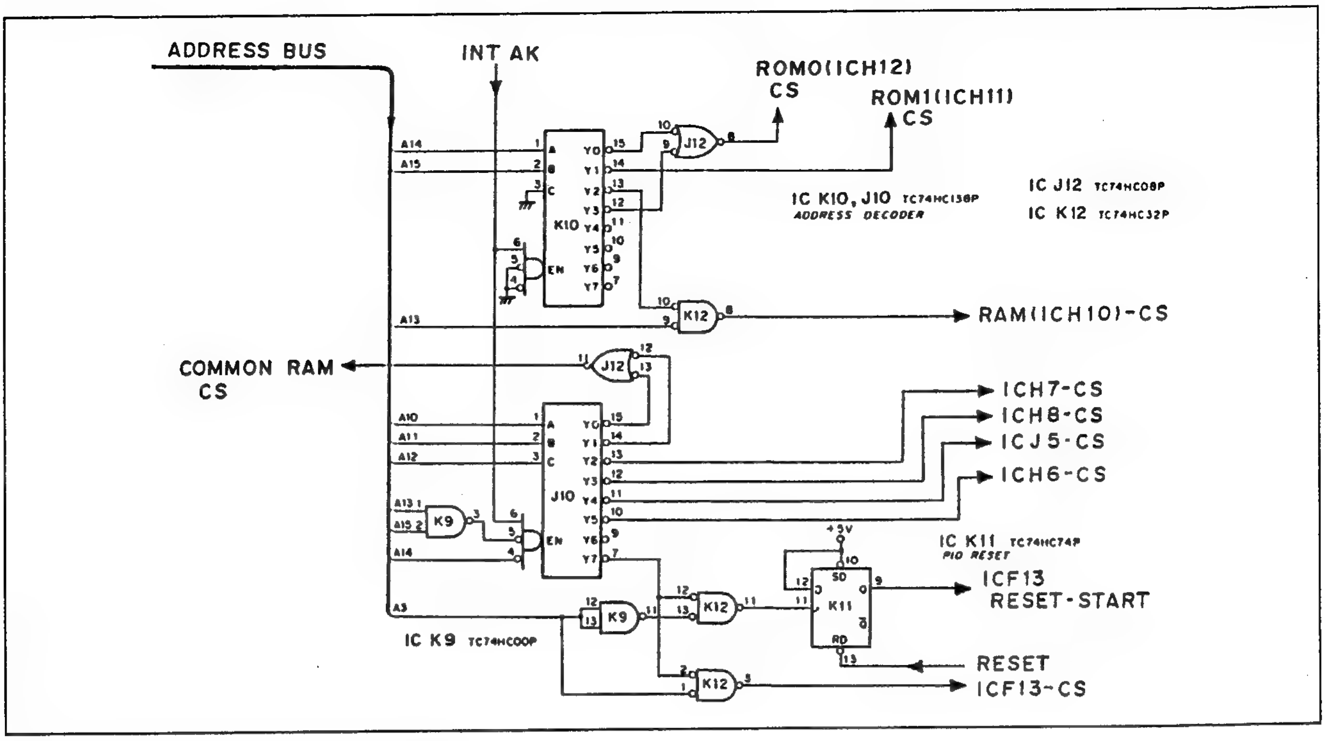


Fig. 4-7-3. Address Decoder (SY-103)

(3) Common memory and peripheral circuitry (SY-103 board)

Interfacing between the SY-103 board and SV-90 board is provided by common memory (RAM) ICJ3. In order for the common RAM ICJ3 to be accessed from both the CPU on the SY-103 board and the CPU on the SV-90 board, one CPU must be made to wait while the RAM is being accessed by the other. For instance, when the CPU on the SY-103 board is to access the common RAM, pin 5 of gate ICG10 is set high by the "~COMMON MEMORY REQUEST" signal created from the output of pins 14 and 15 of address decoder ICJ10. Since common RAM ICJ3 is not being accessed from the SV-90 board, the "~CM CS" signal of pin B18C on the SY-103 board is set high (inactive) and pin 4 of ICG10 is set high. Consequently, pin 8 of flip-flop ICG10 is set high and pin 11 (TP5) of ICG10 is set low.
The high level output of flip-flop ICG10 pin 8 is supplied to common RAM address selector ICH2, H3 and H4 through pin 2 of inverter ICF7, and the SY-103 board address bus is selected. Further, the pin 8/ICG10 output passes through inverter pin 12/ICF7 and gate pin 11/ICF5 to set bus buffer pin EN/ICK1 to high (disable) and isolate the SV-90 board data bus from the common RAM data bus. The low level which is output from pin 11 (TP5) of flip-flop ICG10 sets pin EN of bus buffer ICJ4 to low (enable), thereby connecting the SY-103 board data bus to the common RAM.
When the SY-103 board CPU is accessing the common RAM, the "~CM CS" signal from the SV-90 board is supplied to pin B18C on the SY-103 board if the SV-90 board CPU has attempted to access the common RAM. The "~CM CS" signal passes through pin 10 of inverter ICH1 to set pin 1 of ICG10 to high. However, since pin 8 of flip-flop ICG10 has been set high, pin 8 of ICF8 is set low, the signal returns to the SY-103 board from pin B18a on the SY-103 board as "~SV WAIT" and the SV-90 board CPU is set to the waiting status.
When the SY-103 board CPU has finished accessing the common RAM, the "~COMMON MEMORY REQUEST" signal created from the output of pins 14 and 15 of address decoder ICJ10 is set high and the flip-flop ICG10 status is inverted. If the "~CM CS" signal from the SV-90 board is active at this time, the common memory is accessed by the SV-90 board CPU.

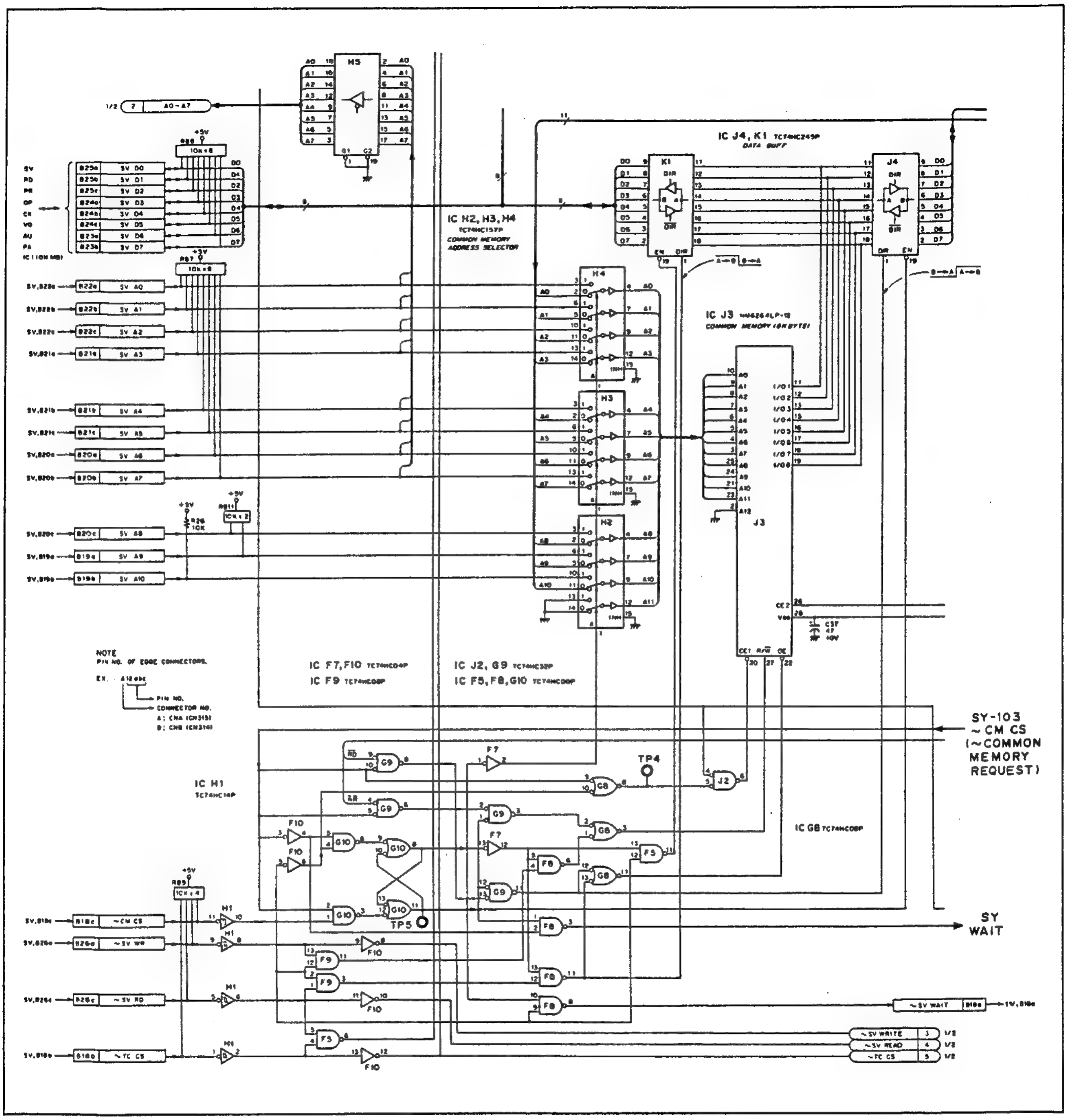


Fig. 4-7-4. Common RAM (SY-103)

The common RAM ICJ3 power supply is backed up by capacitor C38 so that the data are retained for more than 1 week even when the the VTR power is switched off.
When the power switch is set on, a +5V or +12V voltage, whichever is made available faster, is supplied to C38 and C38 is charged by the voltage equivalent to the +5V voltage minus the D3 forward voltage (max. 1.3V). Applied to the D4 anode is the voltage equivalent to +5V plus the D4 forward voltage (max. 0.8V). A common connection is featured for the D4 and D5 anodes and so the voltage drop at both is identical. This means that C38 is charged through the +12V until the D5 cathode voltage reaches +5V and the common RAM ICJ3 is backed up.

When the power switch is set off, the +5V voltage drops, the Q1 base voltage also drops and Q1 goes off. As a result, the voltage at the common RAM CE pin falls below 0.4V before the CPU supply voltage drops below the operating range, and the common RAM retains its data.

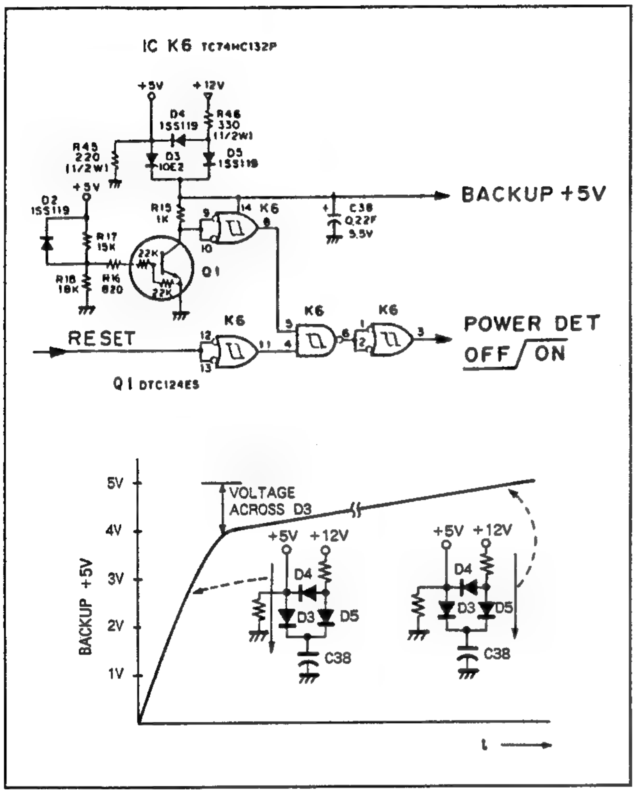


Fig. 4-7-5. Common RAM Back-up Circuit (SY-103)

(4) Interrupt controller (SY-103 board)

Interrupt controller ICJ5 (μ PD71059) can accept 8 types of interrupt request signals. In order to enhance the program efficiency, the interrupt request signals are allocated as shown in Table 4-7-3. The sequence of priority for the interrupts is defined by the software as "INT P7→INT P0→INT P1→··→INT P6." The RS-422 interrupt based on INT P7 is given top priority so that the commands from the remote controller are not lost. ICJ5 and ICH7 stand in a master/slave relationship, and the interrupt vectors based on INT P7 are generated by ICH7. In other words, when the INT P7 interrupt is requested, ICJ5 merely issues the interrupt request to the CPU and the actual interrupt vector is generated by ICH7.
D-type flip-flop ICJ9 is a latch circuit for the slave signals and its output is supplied to pin 19 (pin PRI) of ICH7. When, for instance, an interrupt request for an interrupt other than INT P7 is issued, the INT signal output from pin 17/ICJ5 is latched by both the ASTB signal output from pin 25/ICH14 and the INTAK signal output from pin 24, and a high level is supplied to pin PRI/ICH7. As a result, ICH7 recognizes that the INTAK signal from the CPU has been output to another device. With an interrupt based on INT P7, ICJ5 "SA0, SA1 and SA2" decoded by ICJ8 and ICG8 serve to reset latch ICJ9. Consequently, pin 29 (pin PRI) /ICH7 is set low, ICH7 generates the interrupt vector and the CPU processes the data which correspond to the vector.

Priority	ICJ5	Interrupt request signal
1	INT P7	ICH7 RS-422 transmission/reception
2	INT P0	(Not used)
3	INT P1	REF V detection
4	INT P2	TIMER-0/ICH8 (V timing generation)
5	INT P3	(Not used)
6	INT P4	TIMER-2/ICH8 (RS-422 10 msec detection)
7	INT P5	ICH6 reception
8	INT P6	ICH6 transmission

Table 4-7-3. ICJ5 Interrupt Request Signals (SY-103)

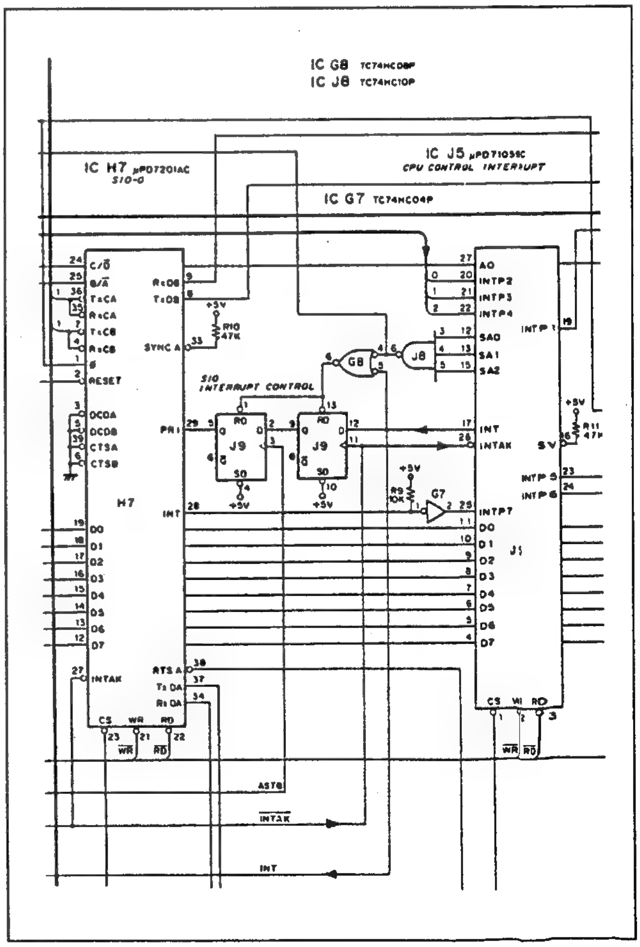


Fig. 4-7-6. Interrupt Controller (SY-103)

The various ICH7 and ICJ5 timing operations shown in Fig. 4-7-7 are now described.

(a) The interrupt request generated by ICH7 is transferred to pin INT P7 of ICJ5 and ICJ5 generates the interrupt request and advises the CPU that the interrupt request is present.
(b) The first $\overline{\text{INTAK}}$ signal is sent to ICJ5 from pin 24 of CPU ICH14. Depending on this signal, ICJ5 judges whether it is to serve as master or slave, and if it is to serve as the slave, the processing that follows is transferred to ICH7.
(c) Since pin 29 (pin PRI) of ICH7 is set high by ICJ9, ICH7 judges that the interrupt request is for another device and it does not generate the interrupt vector.
(d) Since pin 29 (pin PRI) of ICH7 is set low by ICJ9, ICH7 judges that an interrupt with a higher priority than itself is not being requested, and it undertakes the processing of its own interrupt.
(e) The signal produced by AND gate processing the ICJ5 SA0, SA1 and SA2 outputs is supplied to waiting control circuit ICG12 and since the CPU is made to wait for a period equivalent to 1 clock cycle, the TW state is generated once.

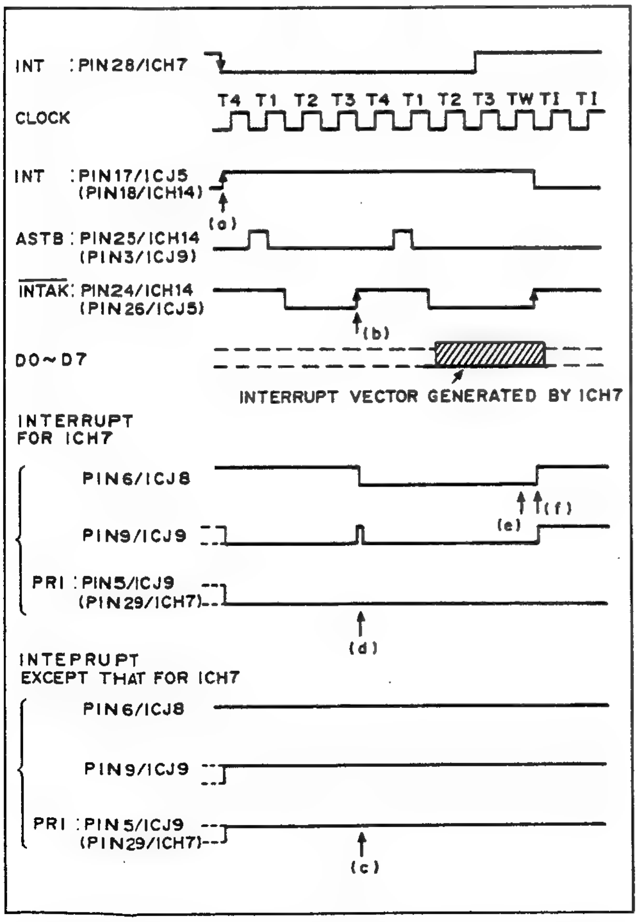


Fig. 4-7-7. Master/Slave Timing Chart (SY-103)

(f) When ICH7 receives the second $\overline{\text{INTAK}}$ signal output from the CPU, it generates the interrupt vector. The CPU executes the transmission/reception processing program in accordance with the contents of the interrupt vector.

(5) REMOTE-1/2A/2B selector (SY-103 board)

ICH7 is used for REMOTE-1/2A/2B connector communication based on RS-422 as well as for data communication between the system control system and the control panel. Channel B is allocated to the control panel and used with a baud rate of 38.4 kbps. ICJ1 is a buffer for communication with the control panel. Channel A is used for the REMOTE-1/2A/2B connectors and it conducts interfacing with external equipments.
REMOTE-1/2A/2B selector ICF6 and ICG6 are selected by the nature of the software using the select signal and priority signal from the CPU, select the signal required from among the REMOTE-1/2A/2B connectors in accordance with the menu instruction, and supply this to ICH7 RXDA/TXDA.
A 0.6144 MHz frequency signal is supplied as the transmission/reception clock signal for channel A of ICH7, and a baud rate of 38.4 kbps is obtained by dividing it down to 1/16 as per the nature of the software using ICH7. When the RS-232C interface kit BKH-3002 (SE-56 board) is employed, the preset data are changed and an RS-232C baud rate is provided so that the transmission/reception clock signal is divided down to 1/32 (19.2 kpbs) or to 1/64 (9.6 kbps) by the CPU.
ICG6 is the REMOTE-1/2A/2B output selector and REMOTE-2A/2B priority signal input selector. REMOTE-1 is fixed as the slave. ICF6 is the REMOTE-1/2A/2B input selector and it selects the input signal based on the select signal from the CPU and the input signal from the master/slave information.

The gate of ICF5 pins 1 and 2 is the master/slave detector circuit. When the CONTROL P or CONTROL R buttons are pressed on the control panel, the high-level master request signal is supplied from the CPU to pin 1 of ICF5. At this time, the PRIORITY 2A or PRIORITY 2B signal has been supplied to pin 2 of ICF5, and pin 3 of ICF5 is turned to high or low by this signal. The CPU detects whether its machine is the master or slave by the state of the inverter ICG7 pin 8 output. When other machine is already being used as the master, it abandons the process of serving as the master, and "LINE ERR" appears on the display of the function control panel.

Tri-state control gate ICG4 and ICF4 set only the output buffer which is being used to the enable status and the other output buffers are placed in the high-impedance state. The buffers for the CCJ RX input pin and CCJ TX output pin are housed on the SE-49 board.

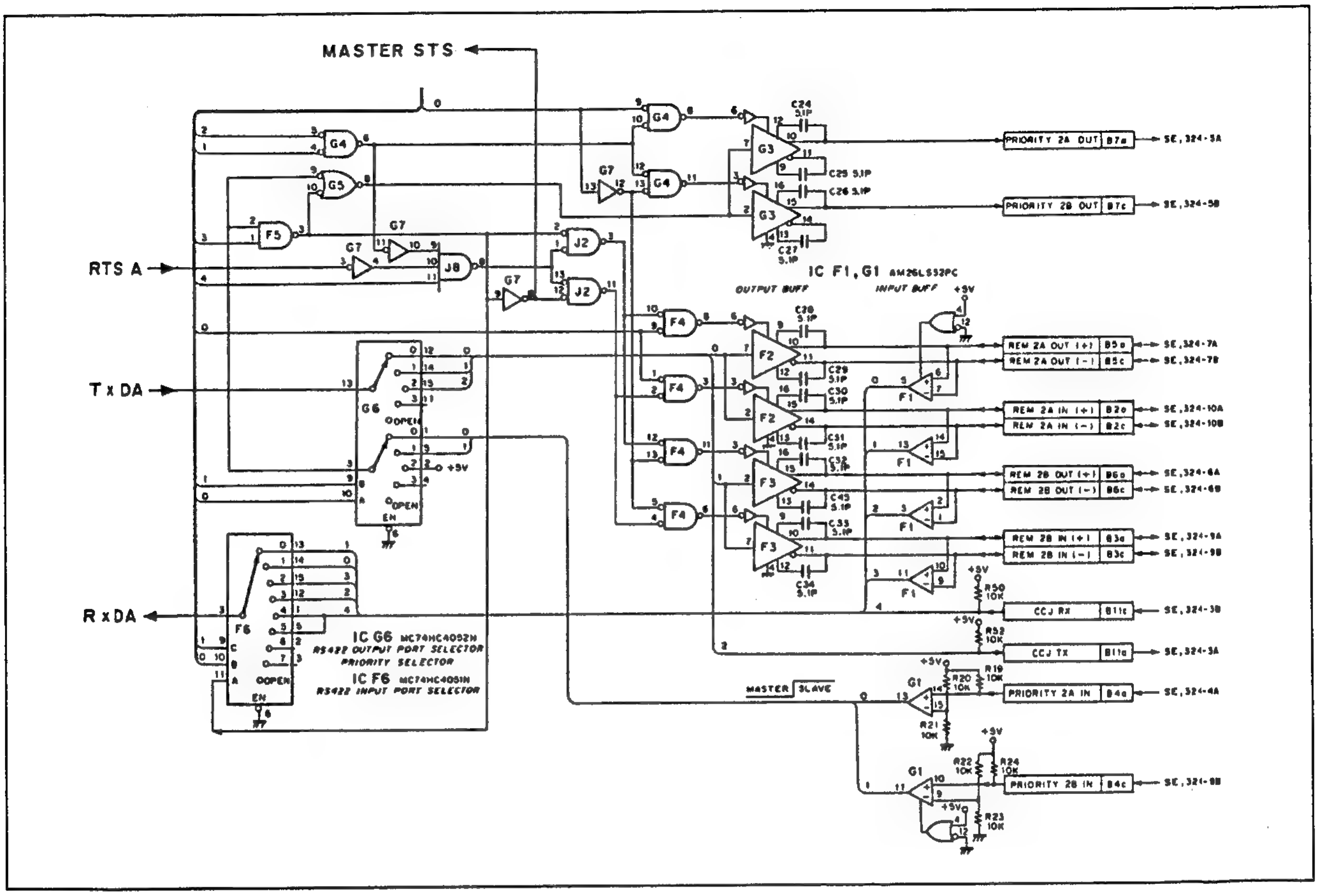


Fig. 4-7-8. REMOTE-1/2A/2B Selector (SY-103)

(6) Programmable timer/counter (SY-103 board)

Programmable timer/counter ICH8 contains three counters, two of which are used in this machine to generate the timing signals in the REF V period and to detect the RS-422 time-out relating to REMOTE-2A and REMOTE-2B. A signal with a 2.4576 MHz frequency is used as the ICH8 reference clock signal and timer detection is possible from 0 to 26.67 msec.

Counter 0 : Generation of timing signals in REF V period
Main processing in V period in REF V+3 msec
Processing of communication with control panel in REF V+11 msec

Counter 1 : Not used

Counter 2 : REMOTE-2A/2B 10 msec time-out detection

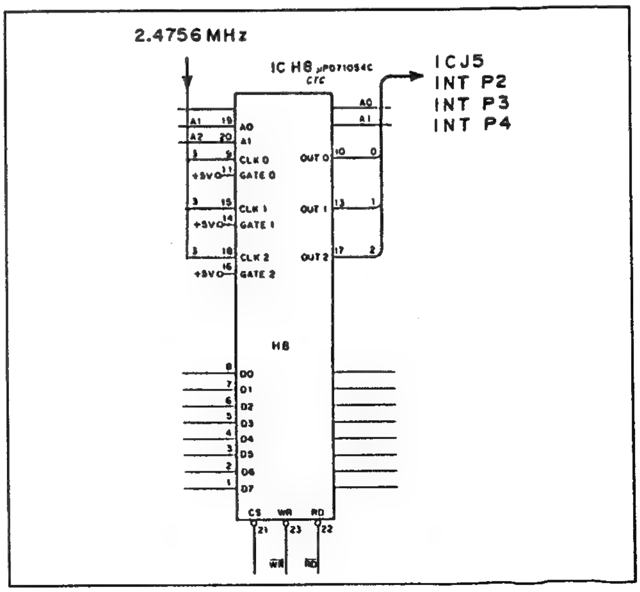


Fig. 4-7-9. Programmable Timer/Counter (SY-103)

(7) Serial control unit (SY-103 board)

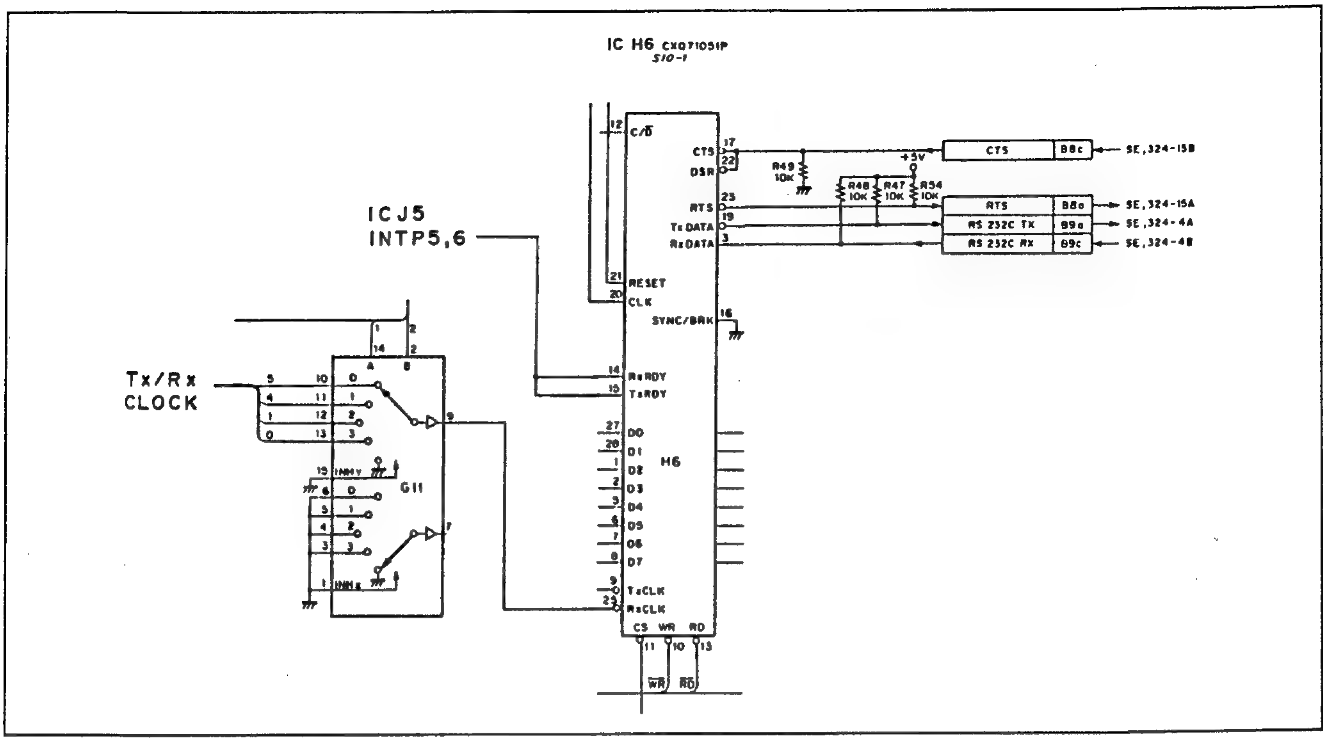


Fig. 4-7-10. Serial Control Unit (SY-103)

Serial control unit ICH6 is provided in order to establish an RS-232C interface between the VTR and a personal computer or other such unit.
There are 4 kinds of communication clock signals : 614.4 kHz, 307.2 kHz, 153.6 kHz and 76.8 kHz. These signals are selected by ICG11. It is possible to assign a baud rate ranging from 38.4 kbps to 1.2 kbps.
Pins RxRDY and TxRDY of ICH6 are connected to pins INT P5 and INT P6 of ICJ5 and this enables the CPU to process the transmission／reception interrupts efficiently.
The CTS (clear to send) signal is supplied to the B8c pin on the SY-103 board and the RTS (request to send) signal is output from pin B8a. These signals can be used as the control line when transmitting or receiving.

(8) I／O port expander (SY-103 board)

ICF13 (CXD1095Q) is an input／output device for enabling the CPU to make full use of the external／internal information.
ICF13 has four 8-bit I／O ports and one 4-bit I／O port, making a total of 36 bits for the I／O ports. On the SY-103 board, the 16 bits of "PA0−PA7" and "PB0−PB7" are used as the input ports and the 20 bits of "PC0−PC7," "PD0−PD7" and "PX0−PX3" are used as the output ports.

PORT	7	6	5	4	3	2	1	0
PA (input)	NO USE	NO USE	NO USE	NO USE	NO USE	NO USE	NO USE	NO USE
PB (input)	TEST SW	RS-232C SENSE	NO USE	NO USE	REF 2	NO USE	NO USE	MASTER STATUS
PC (output)	REM 3 SEL	REM 1 SEL	REM 2 A/B SEL	RS-232C SEL	NO USE	NO USE	μ PD71051 BAUD RATE	
PD (output)	BANK ROM SELECT		NO USE	NO USE	NO USE	NO USE	RS-422 TX ENABLE	MASTER REQUEST
PX (output)	NO HARD	NO HARD	NO HARD	NO HARD	NO USE	NO USE	NO USE	CPU READY

Table 4-7-4. I／O Port Expander Bit Allocation (SY-103)

The bits are defined as follows.

PB7 : TEST SW
Status of TEST switch S2 (SY-103 board)

PB6 : RS-232C SENSE
RS-232C select signal from BKH-3002 (RS-232C interface : SE-56 board)

PB3 : REF2
REF2 information (low=field 1 ; high=field 2)

PB0 : MASTER STATUS
Status signal for advising whether the device connected to the 9-pin connector (RS-422) has output the master signal

PC7, 6 : REM 3 SEL, REM 1 SEL
REMOTE-1／2／3 select signal

PC7	PC6	SELECTION
0	0	REMOTE-2
0	1	REMOTE-1
1	0	REMOTE-3
1	1	UNDEFINED

UNDEFINED : Not output by software

PC5 : REM 2 A／B SEL
REMOTE-2A／2B select signal
(high=REM-2A ; low=REM-2B)
Valid when PC7 and PC6 bits are both low.

PC1, 0 : BAUD RATE
ICH6 baud rate assignment

PC1	PC0	DIVISION	BAUD RATE
0	0	1／64	2.4 kbps
0	0	1／16	9.6 kbps*
0	1	1／64	1.2 kbps
0	1	1／16	4.8 kbps*
1	0	1／64	9.6 kbps
1	0	1／16	38.4 kbps
1	1	1／64	4.8 kbps
1	1	1／16	19.2 kbps

*Not used by software.

PD7, 6 : BANK ROM SELECT
ICH11 bank ROM select signal (1 bank=16k bytes)

PD7	PD6	BANK ROM
0	0	BANK 0
0	1	BANK 1
1	0	BANK 2
1	1	BANK 3

PD1 : RS-422 TX ENABLE
This bit enables REMOTE-2A／2B (RS-422) data transmission. When it is disabled, all the REMOTE-2A／2B transmission lines are placed in the high-impedance state.

PD0 : MASTER REQUEST
This bit is set on by the CPU when its own machine serves as the master. When the controller is connected to the 9-pin RS-422 side and the priority is set to master, the PB 0 bit (master status) is not set on and the CPU is no longer set to serve as the master. In other words, by setting this bit on, the CPU detects the status of the 9-pin connector (high=MASTER ; low=SLAVE).

PX0 : CPU READY
This is the control bit for the LED which displays CPU READY. When it is set on by the CPU, the READY LED lights. When this bit is not accessed for over 106.7 msec, the READY LED goes off.

4-7-2. Time Code Circuit (SY-103 Board)

In the BVH-3000/3100, the time code signals are written and read out directly by the CPU. All the time code system control is exercised by the CPU on the SV-90 board, and the CPU on the SY-103 board gets the necessary data through the common memory (RAM) ICJ3.

(1) Address decoder (SY-103 board)

A total of 256 bytes for addresses "AB00H–ABFFH" are allocated as the time code addresses by the "~TC CS" signal which is supplied from the SV-90 board. The addresses are decoded by ICA13, B13 and C13 on the SY-103 board, and the read and write signals are sent to the various ICs.

ADDRESS	MODE	DEVICE	FUNCTION
AB00H–AB0FH	WRITE	ICE3	I/O PORT EXPANDER
AB10H–AB17H	WRITE	ICC10	TC GENERATOR (LTC)
AB18H–AB1FH	WRITE	ICC10	UB GENERATOR (LTC)
AB20H–AB27H	WRITE	ICE8	TIMER 1
AB28H–AB2FH	WRITE	ICE8	TIMER 2
AB30H–AB3FH	WRITE	ICC10	TCG CONTROL REGISTER
AB40H–AB4FH	WRITE	ICA4	CHARACTER GEN CONTROL
AB00H–AB0FH	READ	ICE3	I/O PORT EXPANDER
AB10H–AB17H	READ	ICC10	TC GENERATOR
AB18H–AB1FH	READ	ICC10	UB GENERATOR
AB20H–AB27H	READ	ICC6	TC READER (LTC)
AB28H–AB2FH	READ	ICC6	UB READER (LTC)
AB30H–AB37H	READ	ICC3	TC READER (VITC)
AB38H–AB3FH	READ	ICC3	UB READER (VITC)

Table 4-7-5. Time Code Address Map (SY-103)

The bit allocation of the I/O port expander ICE3 (CXD1095Q) is described next.
ICE3 has four 8-bit I/O ports and one 4-bit I/O port, making a total of 36 bits for the I/O ports. ICE3 "PA0–PA7," "PB0–PB7" and "PC0–PC7" are used as the output ports, and "PD0–PD7" and "PX0–PX3" are used as the input ports.

PA7 : CHARACTER ENABLE
This enables the TC data of the monitor system to be displayed.

PA6 : VITC ENABLE
This enables VITC to be inserted into the video signal.

PA5 : LTC ENABLE
This inserts the LTC generator signal into audio channel 3.

PA4 : REMOTE-3 TIMER OUT
This activates the timer gate pulse for outputting the TIMER-1/TIMER-2 data to the REMOTE-3 connector.

PA3 : LTC ERROR BYPASS
This sets the error bypass function of the time code reader to ON.

PA0 : CHARACTER RECORD ENABLE
This enables the character display data to be recorded on the tape when REC/EDIT is conducted.

PB6 : VITC FIELD POSITION SELECT
This selects the VITC field position.

PORT	7	6	5	4	3	2	1	0
PA (output)	CHARACTER ENABLE	VITC ENABLE	LTC ENABLE	REMOTE-3 TIMER OUT	LTC ERROR BYPASS	NO USE	NO USE	CHARACTER REC EN
PB (output)	NO USE	VITC FIELD POSITION SELECT	VITC TIME CODE FORMAT SELECT		NO USE	NO USE	LTC TIME CODE FORMAT SELECT	
PC (output)	CHARACTER SYNC SELECT		NO USE	NO USE	NO USE	NO USE	NO USE	CHARACTER IC STROBE
PD (input)	NO USE	VITC ASSIGN 3 BIT (SMPTE)	VITC ASSIGN 6 BIT (EBU)	VITC FIELD DATA	NO USE	LTC BI-PHASE ERROR	VITC READ ERROR	LTC READ ERROR
PX (input)	NO HARD	NO HARD	NO HARD	NO HARD	CFSD–CFSA			

Table 4-7-6. I/O Expander Bit Map (SY-103)

PB5, 4 : VITC TIME CODE FORMAT SELECT
These select the VITC signal format.

PB5	PB4	FORMAT
0	0	PAL, SECAM
0	1	(PAL-M)
1	0	NTSC/PAL-M NDF
1	1	NTSC/PAL-M DF

PB1, 0 : LTC TIME CODE FORMAT SELECT
These select the LTC signal format.

PB1	PB0	FORMAT
0	0	PAL, SECAM
0	1	(PAL-M)
1	0	NTSC/PAL-M NDF
1	1	NTSC/PAL-M DF

PC7, 6 : CHARACTER SYNC SELECT
These select the composite sync signal supplied to character generator ICA4 in accordance with the monitor select or recording mode status.

PC7	PC6	COMPOSITE SYNC SIGNAL
0	0	CHARACTER SYNC
0	1	TBC SYNC
1	0	REF SYNC
1	1	NO SYNC

PC0 : CHARACTER IC STROBE PULSE
The strobe pulse is for transferring data to the register inside character generator ICA4, and it is generated because of the nature of the software by the CPU on the SV-90 board.

PD6 : VITC ASSIGN 3 BIT
This signal indicates the status of VITC ASSIGN 3 BIT (No.35). With the SMPTE time code, it is assigned to the VITC MARK.

PD5 : VITC ASSIGN 6 BIT
This signal indicates the status of VITC ASSIGN 6 BIT (No.75). With the EBU time code, it is assigned to the VITC MARK.

PD4 : VITC FIELD DATA
This denotes the status of the VITC field data specified by the SMPTE or EBU time code.

PD2 : LTC BI-PHASE ERROR
The bi-phase error is detected when the regularity in the BI-PHASE MARK modulation of the LTC playback signal is lost and the data will not be played back properly, and this bit is set on.

PD1 : VITC READ ERROR
This bit is set on when the VITC signal is not played back properly or when a tape with no VITC signal recorded at all has been played back.

PD0 : LTC READ ERROR
This bit is set on when the demodulated time data do not match the regularity of the advance.

PX3−0 : CFSD−CFSA
These indicate the demodulated color frame information from the playback VITC signal. Field 1 and field 2 are identified by the VITC FIELD MARK information.

CFSD	CFSC	CFSB	CFSA	FIELD INFORMATION	
				NTSC	PS
1	1	1	1	F1 & F2	F1 & F2
1	1	0	0	F3 & F4	F3 & F4
0	0	1	1	F1 & F2	F5 & F6
0	0	0	0	F3 & F4	F7 & F8

(2) Clock generator (SY-103 board)

The reference clock signal for the time code reader/generator and the system clock signal for outputting the time data to the REMOTE-3 connector are generated by crystal oscillators X3 (14.31818 MHz for SMPTE) and X2 (14.5 MHz for EBU). I/O port expander ICE5 is accessed and SMPTE/EBU is selected by the CPU on the SV-90 board.

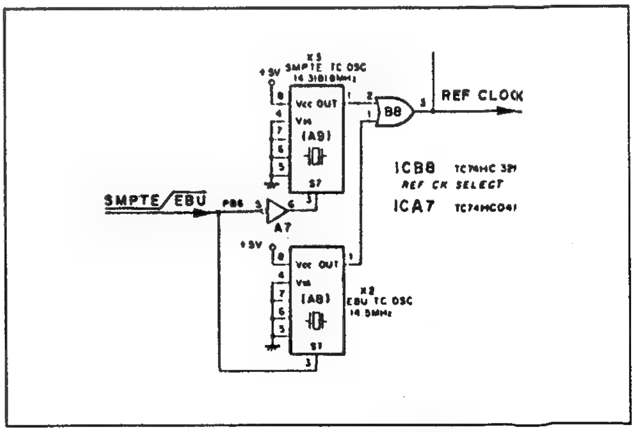


Fig. 4-7-11. Clock Generator (SY-103)

(3) **Time code generator (SY-103 board)**

REGISTER	7	6	5	4	3	2	1	0
SWC	NO USE	NO USE (SLAVE LOCK)	NO USE (DATA LOAD)	TCG $\overline{\text{HOLD}}$/RUN	NO USE (RESET)	NO USE	NO USE (TICT)	NO USE (TIUB)
SWM	CF CTL $\overline{\text{OFF}}$/ON	FIELD-1 IN	ASSIGN-6 BIT	ASSIGN-5 BIT	ASSIGN-4 BIT	ASSIGN-3 BIT	ASSIGN-2 BIT (CF)	ASSIGN-1 BIT (DF)
SWS	NO USE	TIME CODE FORMAT			PHASE CORRECTION $\overline{\text{ON}}$/OFF	VITC FIELD MARK POSITION SELECT		
SWV	VITC POSITION 2				VITC POSITION 1			

Table 4-7-7. TCG Control Signals (SY-103)

Time code generator ICC10 is characterized by free-running operation based on the reference clock input. In order to synchronize the time code signal with the video signal, the REF SYNC signal is supplied to the CS IN pin (pin 27) and ICC10 uses the REF SYNC and reference clock to generate the VITC and LTC time code data.
ICE10, E11, E12 and E13 convert the parallel data from the CPU into serial data. The control signal is read into the register inside ICC10 by the SCK0 clock signal which is output from pin 4 of ICC10.

SWC4 : TCG HOLD/RUN control
This controls the HOLD/RUN status of the time code generator.

SWM7 : CF CTL ON/OFF
When this bit is set on, the time code signal which is generated is locked to the SWM6 color frame information.

SWM6 : FIELD-1 IN
This is the color frame information ; it is set high in field 1.

SWM5−0 : ASSIGN-6−ASSIGN-1
These assign bits are for setting the time code signal on or off. SWM5, 4, 3 and 2 are null bits.
SWM1 : Color frame bit
SWM0 : Drop frame bit

SWS6−4 : TIME CODE FORMAT
These bits are for selecting the time code format select signals.

SWS6 (S4)	SWS5 (S2)	SWS4 (S1)	FORMAT
1	1	1	NTSC/PAL-M DF
1	1	0	NTSC/PAL-M NDF
1	0	1	(PAL-M)
1	0	0	PAL/SECAM
0	0	0	FILM

SWS3 : PHASE CORRECTION ON/OFF
This controls the PHASE correction bit for parity checks.

SWS2−0 : VITC FIELD MARK POSITION SELECT
These bits select the VITC field mark position.
SMPTE time code : bit 27
(corresponds to ASSIGN3)
EBU time code : bit 59
(corresponds to ASSIGN6)

SWV7−4, SWV3−0 : VITC POSITION-2, 1
These bits select the insertion lines for the VITC signal.
NTSC : Lines 10−25 (standard setting : lines 12 and 14)
PAL/SECAM : Lines 7 (320) −22 (335) (standard setting : lines 19 and 21)

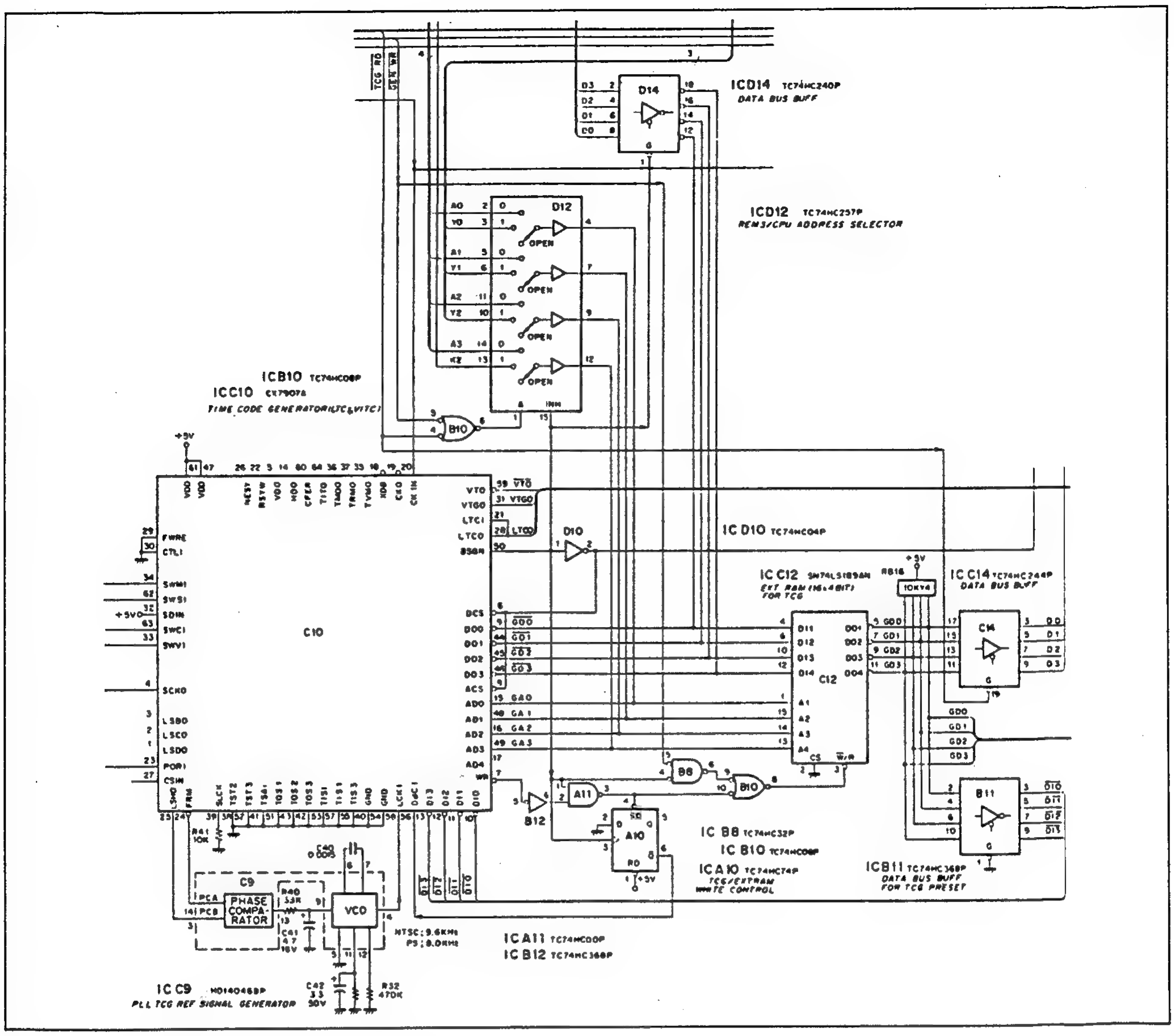


Fig. 4-7-12. Time Code Generator (SY-103)

The time code generator circuit is now described. The basic LTC clock signal is generated by ICC10 and ICC9. The SMPTE LTC clock signal has a frequency of 9.6 kHz (80 bits×30 Hz×4) while the EBU LTC clock signal has a frequency of 8 kHz (80 bits×25 Hz×4). ICC10 generates the 30Hz/25Hz SYNC WORD signal and outputs it from the LSHO pin (pin 25). ICC10 decodes the REF SYNC signal supplied externally and converts it into the frame signal which it then outputs from the FRM pin (pin 24). ICC9 compares the phases of these two signals, drives the VCO with its output and generates the reference clock signal (9.6 kHz for SMPTE ; 8 kHz for EBU) which is synchronized with the video signal. The data arriving from the CPU are preset as follows into time code generator ICC10. All the data are input into, and output from, ICC10 via memory (RAM) ICC12. ICC10 operates in synchronization with the video input signal in frame units and data are input or output once per frame.

CPU ICH14 reads the data while avoiding the input/output timing (FRAME TOP+approx. 29.5 msec) of time code generator ICC10 and when preset data are present, it writes them into ICC12. The data are read at a timing of "V+approx. 1.5 msec" while they are written at a timing of "V+approx. 8.6 msec." ICC10 reads the memory data from ICC12 once per frame and accepts them into its own register. The accepted data are immediately written again into memory ICC12.

When the data from the CPU are written into memory ICC12, time code generator ICC10 accepts the data immediately from ICC12 and sets them into the register inside ICC10. When the data from the CPU have not been set in ICC12, ICC10 repeats the read/write operation of the data applying to the previous frame. Fig. 4-7-14 is the read/write timing chart of external memory ICC12 based on ICC10.

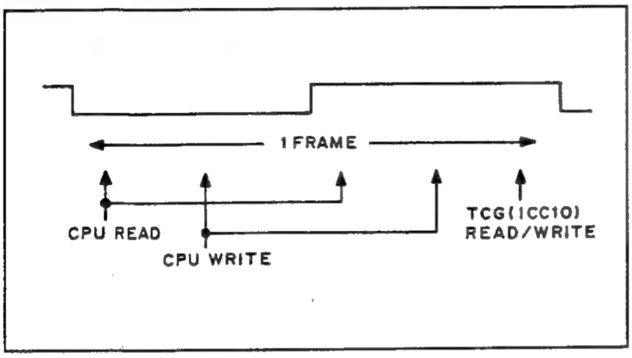


Fig. 4-7-13. TCG CPU Read/Write Timing (SY-103)

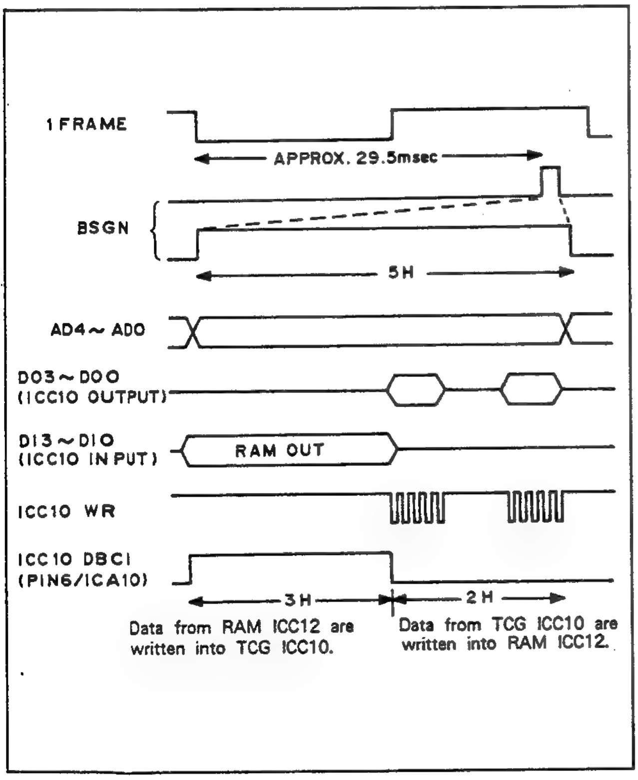


Fig. 4-7-14. External Memory Read/Write Timing (SY-103)

The data interfacing of above-mentioned time code generator ICC10 can be summarized as follows.

- CPU ICH14 reads out the TCG data which are stored in memory (RAM) ICC12 at the "V+1.5 msec" timing.
- CPU ICH14 writes the TCG data into ICC12 at the "V+8.6 msec" timing.
- Time code generator ICC10 reads out the TCG data from memory ICC12 within the time corresponding to 3H from the "frame+29.5 msec" timing, it sets them into its own register and then writes the TCG data into ICC12 in the following 2H.
- Time code generator ICC10 outputs the necessary data to REMOTE-3 immediately after it has output the data to memory ICC12.

(4) LTC reader (SY-103 board)

LTC reader ICC6 (CX7912A) contains most of the circuitry required to read the LTC signal. It operates in synchronization with the time code pulse played back from the tape, and CPU ICH14 is synchronized with the REF V signal. As a result, the ICC6 output is temporarily stored in memory (RAM) ICD7, and the CPU reads out the stored data at the timing which is synchronized with the REF V signal.

The series of operations starting with tape playback and ending with readout by the CPU are processed in the following way.

- LTC reader ICC6 transfers the data which it has read out from itself to memory ICD7 once per field, and it does this at the timing of the fall edge of the V pulse (REF V) which is input to pin 13 of D-type flip-flop ICA10.
- It outputs the time code data to the REMOTE-3 connector at the timing of the rise edge of the memory WR signal which is input to pin 3 of memory ICD7.
- It sets the $\overline{\text{TC BUSY}}$ signal of the CPU to the enable status at the timing of the completing edge (rise edge) of the signal output to the REMOTE-3 connector. The CPU then accesses the memory at a certain timing from the REF V signal, it checks that the TC ERR/BUSY signal is off and it transfers the data to its own memory. When the TC ERR/BUSY signal is on, the data are held or updated by software.

(a) The signal (ICA10 pin 9) indicating whether the time code data have been transferred once per field is reset by the REF V signal.

(b) ICC6 outputs the BSRL signal (pin 50) for outputting the LTC data. The BSRL signal is supplied through ICC2, A12 and B12 to pin 6 of ICC14 to serve as the $\overline{\text{TC BUSY}}$ signal for the CPU. The $\overline{\text{TC BUSY}}$ signal is sent through the data bus to the CPU and the CPU is advised that the LTC data are being read out.

(c) The data output from LTC reader ICC6 are stored by the memory $\overline{\text{W}}$/R signal in memory ICD7. Pin 8 of ICB12 is set high and REMOTE-3 TC gate ICB5 is triggered.

(d) The REMOTE-3 TC OUTPUT STS signal (pin 9 of ICB5) is set high and supplied to pin 11 of ICA10, and the signal (pin 9 of ICA10) indicating that the data have been transferred once per field is set high. As a result, data writing into the memory is prohibited and the data are not written until the next field even if the memory WR signal is output from LTC reader ICC6.

(e) The $\overline{\text{TC BUSY}}$ signal is low and so the CPU does not read out the LTC data.

(f) The $\overline{\text{TC BUSY}}$ signal is high and so the CPU reads out the LTC data.

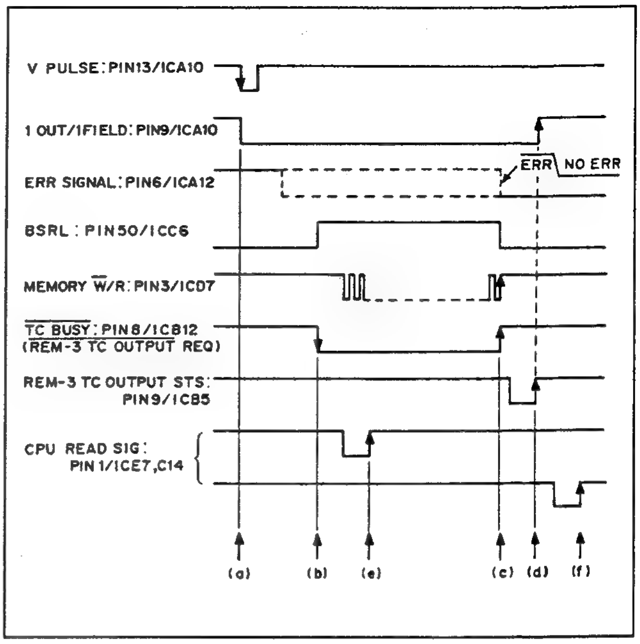


Fig. 4-7-16. LTC Reader Timing Chart (SY-103)

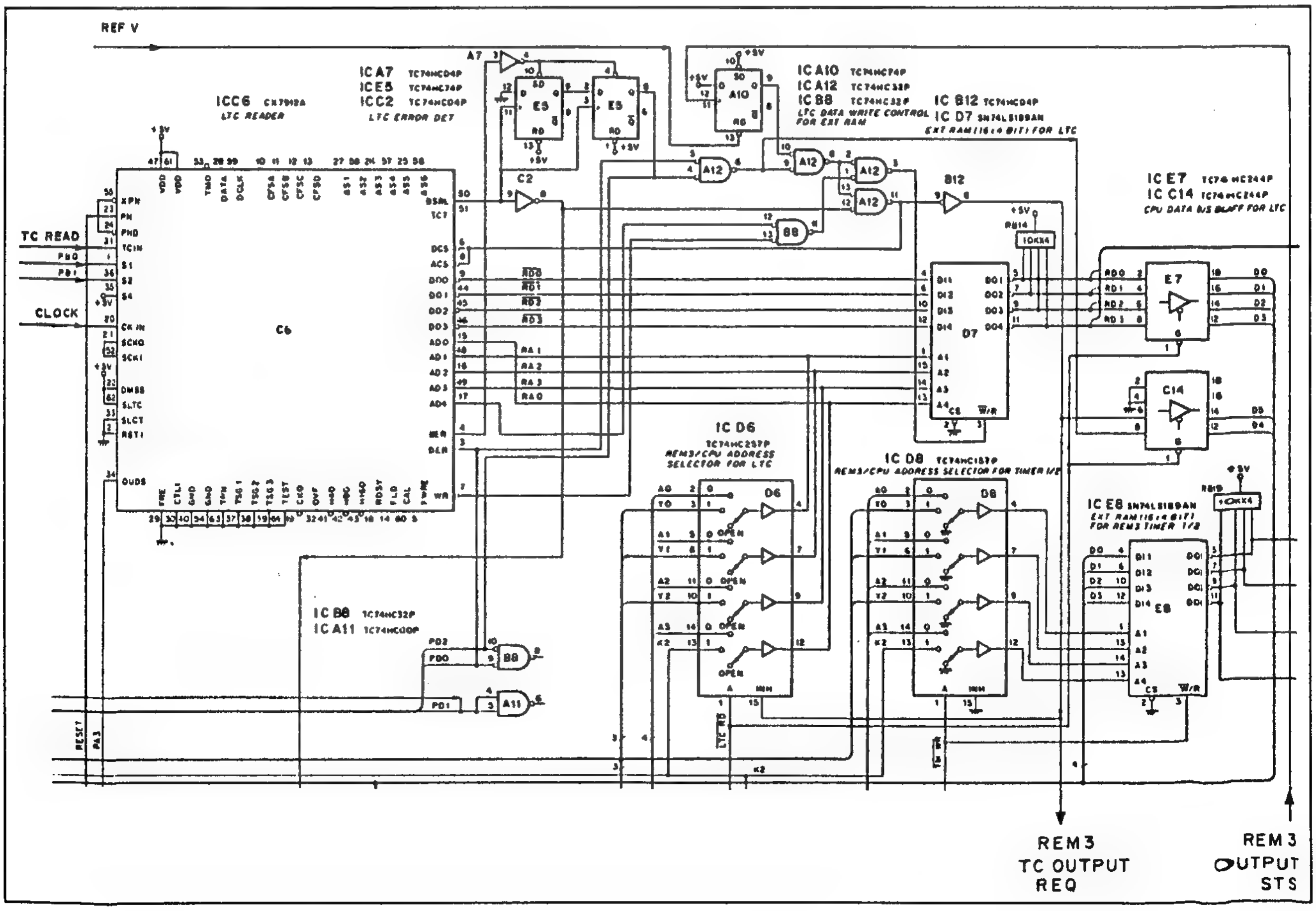


Fig. 4-7-15. LTC Reader (SY-103)

D-type flip-flop ICE5 is the circuit that detects the LTC BI-PHASE bit error. ICE5 latches the BER signal which is output from ICC5 and prevents the error data from being transferred to memory (RAM) ICD7. There is a reason for this : the BER signal, which indicates that the regularity of the BI-PHASE MARK modulation has been lost, is output but this signal is cleared immediately when the regularity is properly restored and the CPU cannot detect the bit errors.
D-type flip-flop ICA10 generates the control signal for transferring the LTC data once per field to ICD7. The V pulse (REF V) is input to pin 13 of ICA10. Pin 9 of ICA10 is set low for that period from the timing of the V pulse fall edge until the completion of the data output to the REMOTE-3 connector, and the LTC data from ICC6 are transferred to memory ICD7. When the data output to the REMOTE-3 connector is completed, Pin 9 of ICA10 is set high to prohibit the transfer of data to the memory.
The system clock signal of LTC reader ICC6 is supplied from VITC reader ICC3 (CX7913A). It is produced by dividing down the system clock signal of the VITC reader to 1/3.

SYSTEM	VITC CLOCK	LTC CLOCK	LTC DYNAMIC RANGE
SMPTE	14.31818MHz	4.7723MHz	1/34 TO 107 TIMES
EBU	14.5MHz	4.8333MHz	1/26 TO 130 TIMES

The CPU on the SV-90 board is responsible for the LTC signal interpolation. When the error bit or BUSY bit is on once the LTC signal has been read, the CPU replaces the display with the LTC interpolation data created from the CTL signal and REEL FG signal. The LTC interpolation data are always provided even when there are no errors, and even immediately after the power has been switched on, it is possible to display precise interpolation data when the data are read out correctly.

(5) VITC reader (SY-103 board)

VITC reader ICC3 (CX7913A) contains most of the circuits required to read out the VITC signal. In the NTSC model (SMPTE), a system clock with a frequency of 14.31818 MHz is supplied to ICC3 ; in the PAL/SECAM model (EBU), it has a frequency of 14.5 MHz. The VITC signal is demodulated inside ICC3 based on the system clock signal, composite sync signal and playback VITC signal. ICA2 creates the composite sync signal. ICA2 gates the playback sync signal supplied from the VO-16 board using dropout information and outputs the sync signal only when it is played back normally from the tape. The playback VITC signal is directly input into ICC3 from the VO-16 board.

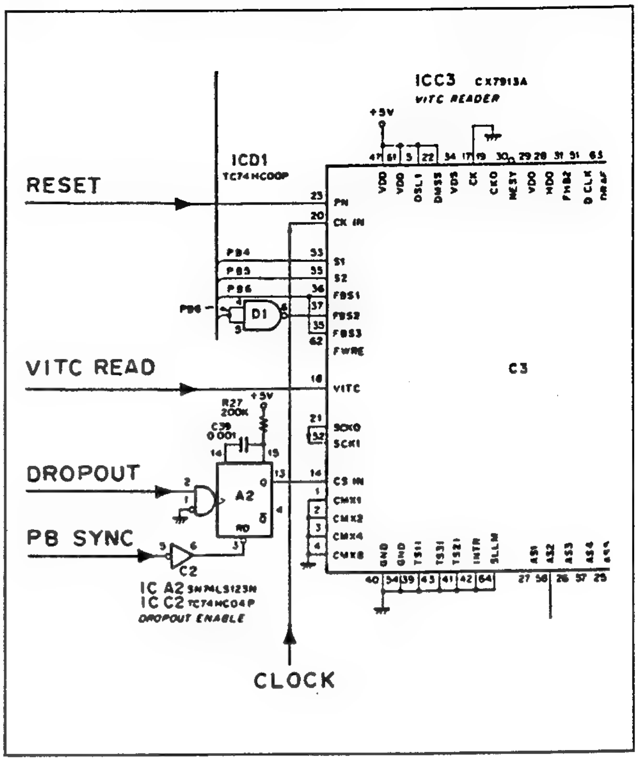


Fig. 4-7-17. VITC Reader Input Circuit (SY-103)

The VITC data provided from the playback signal are read out by ICC3 and immediately transferred to memory (RAM) ICD5. While ICC3 is outputting the VITC data, the BSRV signal (pin 50) is set high, the ICD4 output is prohibited, ICC3 controls the DO0−DO3, AD0−AD3 and WR signals, and the VITC data are written into memory ICD5. The timing at which the data are written is regulated as follows by the position of the VITC data.

SMPTE : V+0.636 ms−V+1.589 ms
(line 10−line 25)
EBU : V+0.448 ms−V+1.408 ms
(line 7−line 22)

Avoiding of the time during which the data are written, the CPU reads out the VITC data from memory ICD5 and it uses these data for the timer display and superimposition characters. "V+approx. 1.8 ms" represents the timing at which the CPU reads out the VITC data from memory ICD5. Memory ICD5 is constantly scanned by the system clock signal and the stored VITC data are output to the REMOTE-3 connector. However, VITC data output gate ICD4 is set on only once per field by the BSRV signal which is output from pin 51 of ICC3.

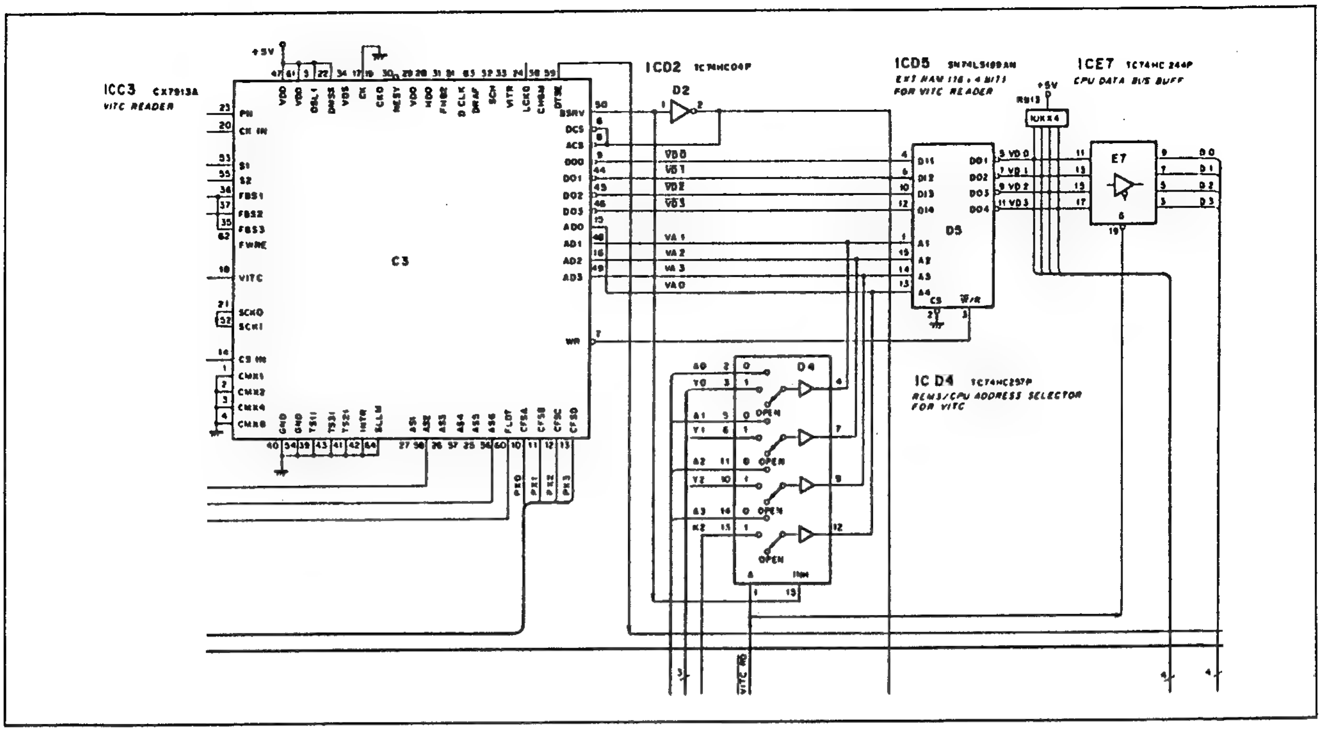


Fig. 4-7-18. VITC Reader Output Circuit (SY-103)

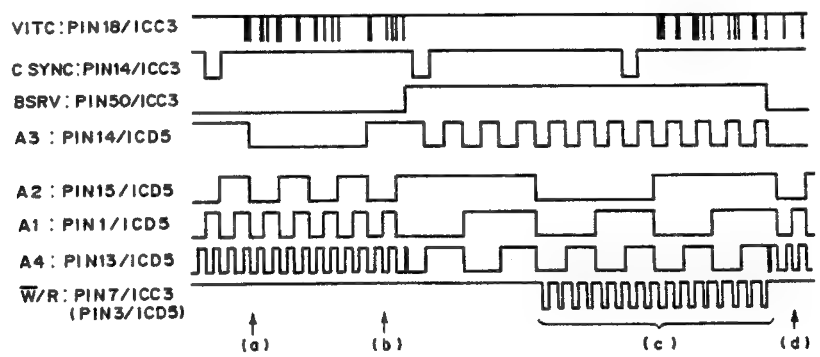


Fig. 4-7-19. VITC Write Timing (SY-103)

(a) The playback VITC signal is supplied to ICC3. The system clock signal is supplied to address pins A3, A2, A1 and A4 of ICD5 via ICD4.

(b) The BSRV signal is set high so that ICC3 will output the data.
The address output of ICC3 is supplied to the address pin of ICD5. The ICD4/system clock system is placed in the high-impedance state.

(c) The VITC data read out by ICC3 are transferred to memory ICD5.

(d) The ICC3 data output is completed.
The gate signal is output to the REMOTE-3 connector from the timing of the BSRV signal fall edge.

The error detector circuit is contained inside ICC3, and the detected error information is sent to the CPU from the DTSE pin (pin 59) via ICE3. ICC3 is also provided with output pins (DFSA–DFSD) for the color frame signal, and the CPU uses ICE3 to read in the color frame signal. The CPU infers the color field numbers in accordance with the NTSC or PAL/SECAM signal from the field mark bit of the VITC signal and this color field signal, and it inserts the number into the time code display.

(6) Timer memory circuit (SY-103 board)

The SY-103 board does not have a circuit which detects the timer data. The timer data are provided by the CPU on the SV-90 board from the CTL signal and REEL FG information through processing which accords with the software. In order for the TIMER-1 and TIMER-2 signals to be output to the REMOTE-3 connector, memory (RAM) ICE8 is provided on the SY-103 board.
Address selector ICD8 selects the address bus side only when the CPU writes the data into memory ICE8, and at all other times it selects the system clock side. The CPU writes the timer data into memory ICE8 once per field at the timing of "V+approx. 13.5 ms." Upon completion of the writing, the trigger (PA4) signal is output by the CPU from pin 60 of ICE3 in order to make REMOTE-3 connector gate circuit ICB6 active.

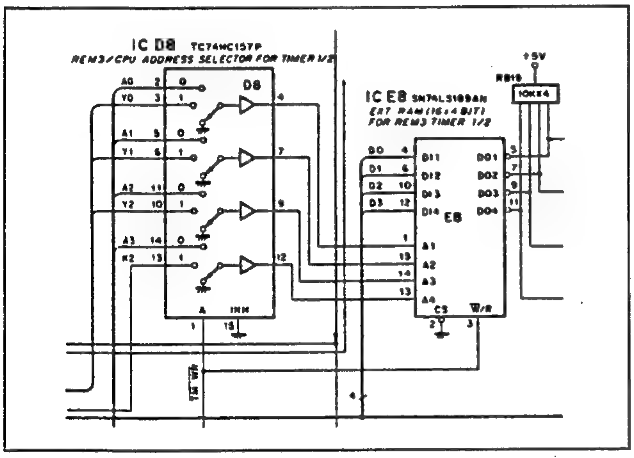


Fig. 4-7-20. Timer Memory Circuit (SY-103)

(7) Time data read/write timing (SY-103 board)

Following the description of the time data circuitry in sections (3) through (6), the following figure shows the read/write timings with respect to the various ICs as seen from the CPU.
The timing of all the time data except the LTC data is controlled by the software so that there will be no conflict due to any restrictions arising from the hardware configuration. It is possible to provide information as to whether even the LTC data have conflicted, and whether the data are to be retained or interpolated is controlled by the software.
When the tape speed is increased, the timing at which the LTC data are written into ICC6 becomes unstable, the data conflict with the read data in the first half of the field and it is no longer possible to write the data stably. The data are therefore read in the second half of the field to prevent conflict.

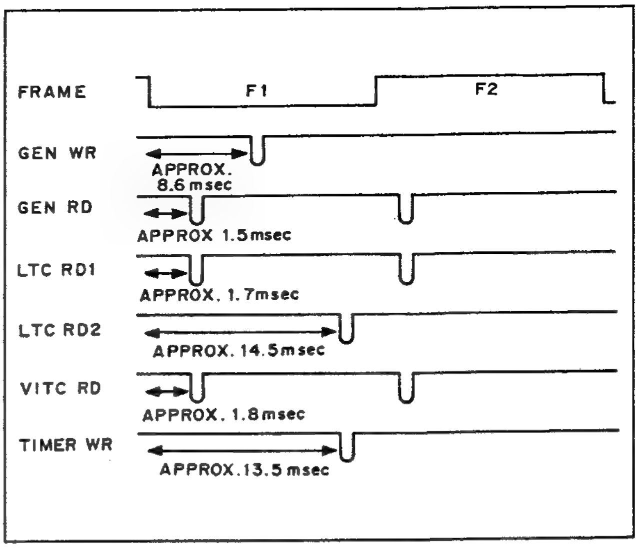


Fig. 4-7-21. Time Data Read/Write Timing (SY-103)

(8) Character generator (SY-103 board)

Character generator ICA4 (μ PD6142C) is capable of displaying 64 characters in a maximum of 24 columns/12 lines using 5×7 dots. It can also control the display position and size of the characters as well as their background, and these can be selected using the menu.
The composite sync signals selected as follows are supplied by ICA3 to the H SYNC pin (pin 14) of ICA4.

- CHARA SYNC

This is the sync signal of the MONITOR output signal selected by the [S02. PICTURE MONITOR SELECT] menu.
The CHARA SYNC signal is selected by ICA3 when INPUT or DEMOD has been selected by menu S02.

- TBC SYNC

This is the sync signal of the TBC output video signal.
The TBC SYNC signal is selected by ICA3 when TBC OUT has been selected by the [S02. PICTURE MONITOR SELECT] menu or when VD2+TBC has been selected by the [S59. MIXED CHARA OUTPUT] menu.

- REF SYNC

This is the sync signal of the servo reference signal which is selected by the [S40. SERVO REF SELECT] menu.
The REF SYNC signal is selected by ICA3 when ENABLE has been selected by the [I60. CHARACTER RECORD] menu, in other words, when the characters are mixed with the video signal and recorded on tape.

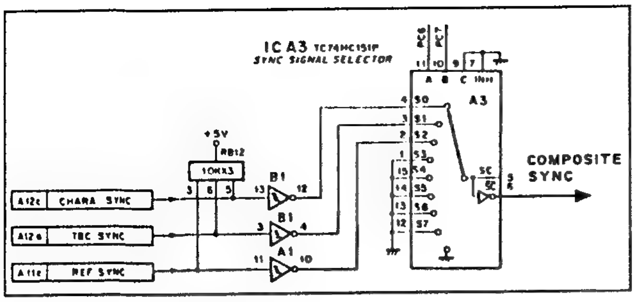


Fig. 4-7-22. Character Generator Sync Signal Selector (SY-103)

The V sync signal which has been separated from the composite signal by R39/C43 is supplied to the V SYNC pin (pin 13). The frequency (min. 4 MHz to max. 7 MHz) of the signal generated by the oscillator inside ICA4 is determined by L1, C184 and C185 which are connected to pins 6 and 7, and the character size in the horizontal direction is regulated. The 8-bit serial data which have been parallel/serial converted by ICE6 are supplied to ICA4 as the control command.

ICB9, A11 and B10 generate the 8 transfer clock signals required to transfer the data from ICE6 to ICA4. The $\overline{\text{CHR WR}}$ signal from the CPU which has been decoded by ICA13 is accepted into latch ICC8 and at the next stage latch ICC8 it is synchronized by the 0.6144 MHz reference clock signal. When pin 8 ($\overline{\text{Q}}$) of ICC8 is set low as a result, pin 8 (QD) of ICB9 is set low, NAND gate ICA11 and ICB10 are made active, and the transfer clock signals are sent to ICE6 and ICA4. When ICB9 reaches a count of 8 for the transfer clock signals, pin 8 (QD) is set high, feedback is then applied from ICC8, operation is suspended, and the output of the clock signal to ICE6 and ICA4 is stopped.

In order to set the transferred serial data in the register inside ICA4, the strobe pulse from the CPU is supplied through inverter ICA7 to pin 3 of ICA4.

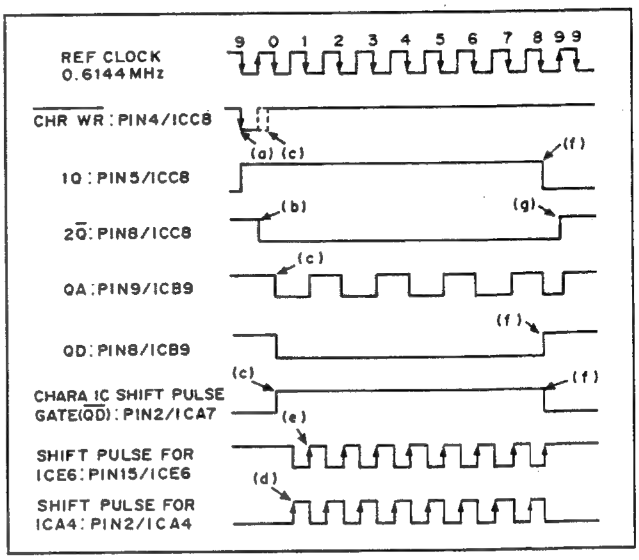


Fig. 4-7-24. Transfer Clock Signals (SY-103)

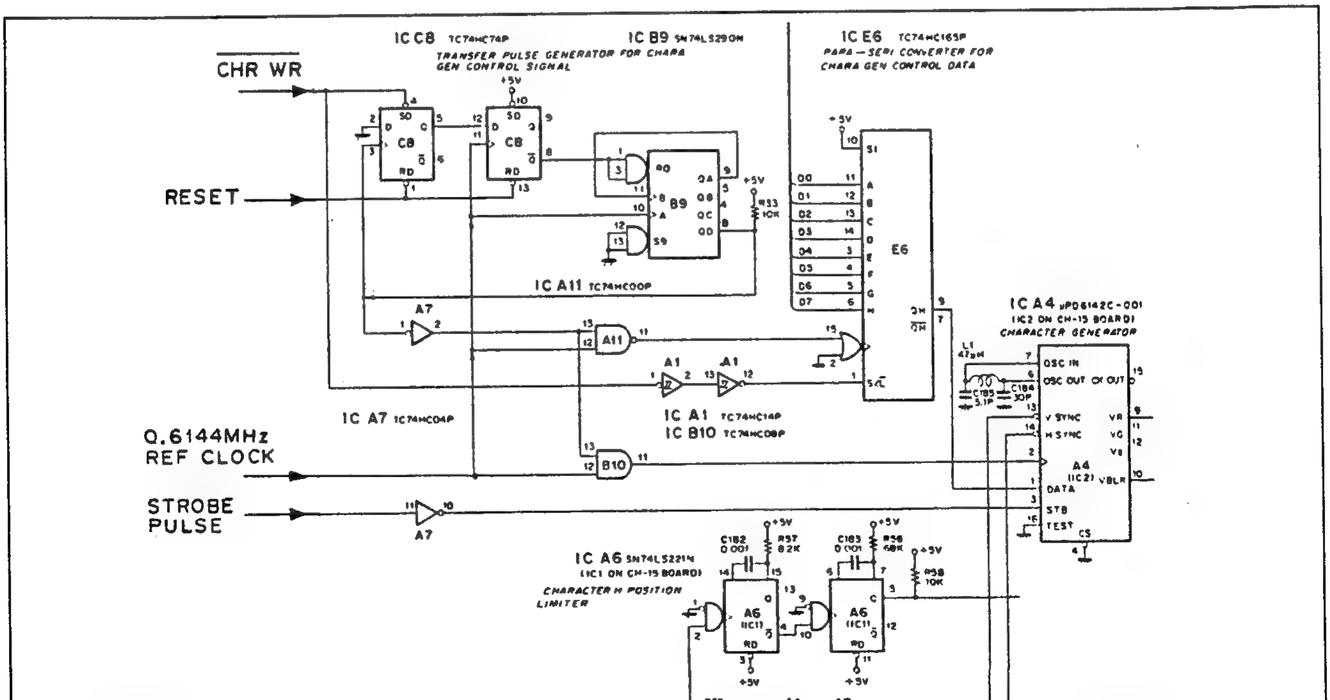


Fig. 4-7-23. Character Generator Input Circuit (SY-103)

(a) When the $\overline{\text{CHR WR}}$ signal is received from the CPU, pin 5 of ICC8 is set high.
(b) It is synchronized with the reference clock signal so that counter ICB9 is set to the enable status at the next rise edge of the reference clock signal.
(c) The counter advances by one count at the next fall edge of the reference clock signal, and the transfer clock signal gate is set to the enable status. When the $\overline{\text{CHR WR}}$ signal does not rise at the gate enable timing, the shift register ICE6 transfer is delayed and a malfunction results.
(d) One bit is transferred to ICA4.
(e) Shift register ICE6 is shifted by 1 bit.
(f) The gate pulse is disabled and pin 5 of ICC8 is reset.
(g) The counter is held after half a clock cycle and the clock signal transfer is suspended.

The characters generated by ICA4 and its gate signal are output to the other circuit boards through the various gates. Monostable multivibrator ICA6 generates the gate signals for adjusting the front porch and back porch width of the character output signal. The signal which is output from monostable multivibrator ICA6 is mixed with the character gate signal by AND gate ICG5, and the character signal is prevented from being mixed in with the front porch (9.4 μ sec) and back porch (1.5 μ sec) signals. Whether or not the character signal and character gate signal are to be valid is controlled by the PA7 signal from the CPU which is supplied to NAND gate ICB2. The PA7 signal from the CPU is the monitor character enable signal and the PA0 signal is the character recording enable signal. The character signal is also mixed with the VITC signal by AND gate ICC1 and, in accordance with the BVH-3000/3100 menu settings, the characters can be superimposed onto the VITC signal and recorded on tape.

(9) REMOTE-3 connector interface

The SY-103 board is provided with an interface circuit so that the time code data are output to the REMOTE-3 connector (parallel remote control, D-SUB 50 pins). The data which are output to this connector are synchronized by the system clock signal which is used exclusively for the REMOTE-3 connector.
The system clock signals are created by dividing down the 14.31818 MHz (or 14.5 MHz for EBU) reference clock signal. While LTC reader ICC6 is outputting data, the system clock signal is stopped by the BSRL signal (pin 50 of ICC6) to be synchronized with the ICC6 output data. The BSRL signal is set high while ICC6 is outputting data.
The following 8 types of data are output from the REMOTE-3 connector in the form of 4-bit×8-digit data strings. These data are output in a single period of the K3 pulse which is output from pin 9 of ICD11.
The K3 pulse period is 143.03 μ sec (or 141.24 μ sec for EBU).

TM1	TM2
LTC TC	LTC UB
VITC TC	VITC UB
TCG	UBG

The system clock signals are defined as below.

TC clock signal :
This is the internal reference clock signal for transferring or updating the data.
SMPTE : 0.447 MHz (2.235 μ sec)
EBU : 0.453 MHz (2.207 μ sec)

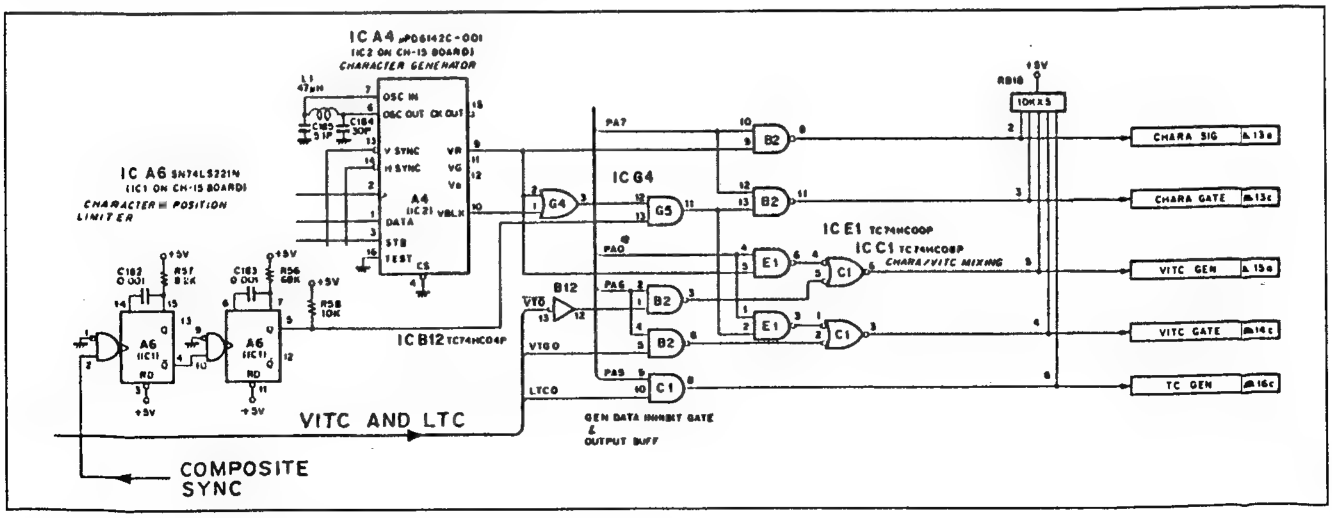


Fig. 4-7-25. Character Generator Output Circuit (SY-103)

Memory WR pulse :
This pulse has the same frequency as the TC clock signal. It is used when an external unit stores the time code data. The memory WR pulse is generated at the timing of the center of the Y0 pulse which is output from pin 4 of ICD9.

Y0−Y2 :
These are the timing pulses for scanning the time data configured by 4 bits×8 digits.

K1−K3 :
These are the timing pulses for scanning the 8 types of timing data.

K4 :
This is the pulse whose period is double that of the K3 pulse. It is used as the sync pulse when accepting the 8 types of data.

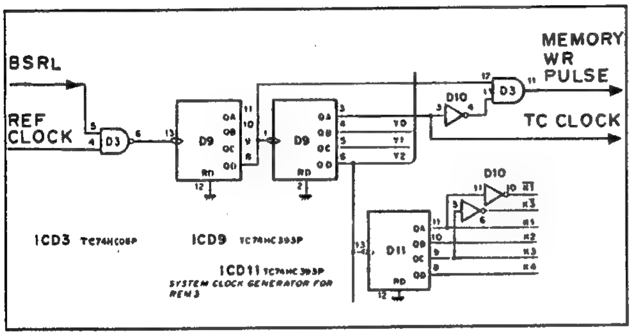


Fig. 4-7-26. System Clock Signal Generator (SY-103)

The digits of "1F−10H" are scanned by the Y0 pulse and the time data are scanned by the K1 pulse. The timing at which the time code reader/generators (ICC3, C6, C10) update the respective data is not synchronized with the system clock signals. ICB5 and B6 (SN74120N) are used in order to synchronize the timing with these signals and make the gates active. The timing is synchronized to the system clock signals by triggering ICB5 and B6 with the trailing edge of the signal indicating that ICC3, C6 and C10 are transferring the data to the memory. TIMER-1/-2 provides the trigger through the software. ICB5 and B6 output the first pulse of the input clock signal when pins S1 and S2 are set low. The time code ICs and REMOTE-3 connector interface are synchronized by using this output pulse as the gate pulse.

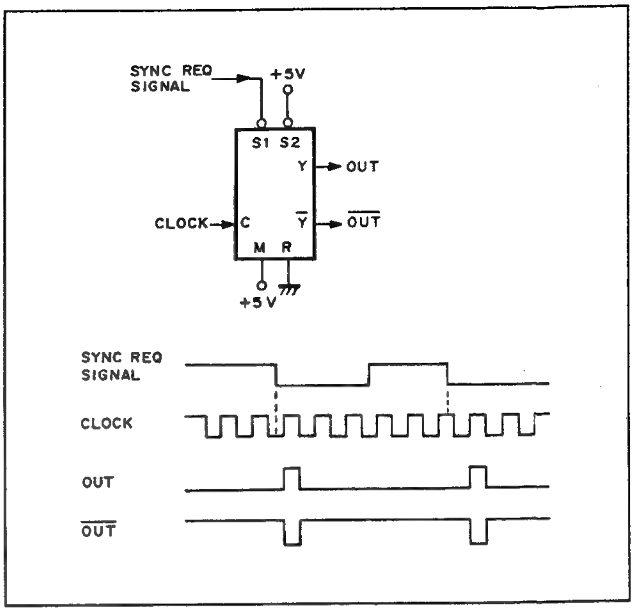


Fig. 4-7-27. SN74120N/ICB5, B6 Operation (SY-103)

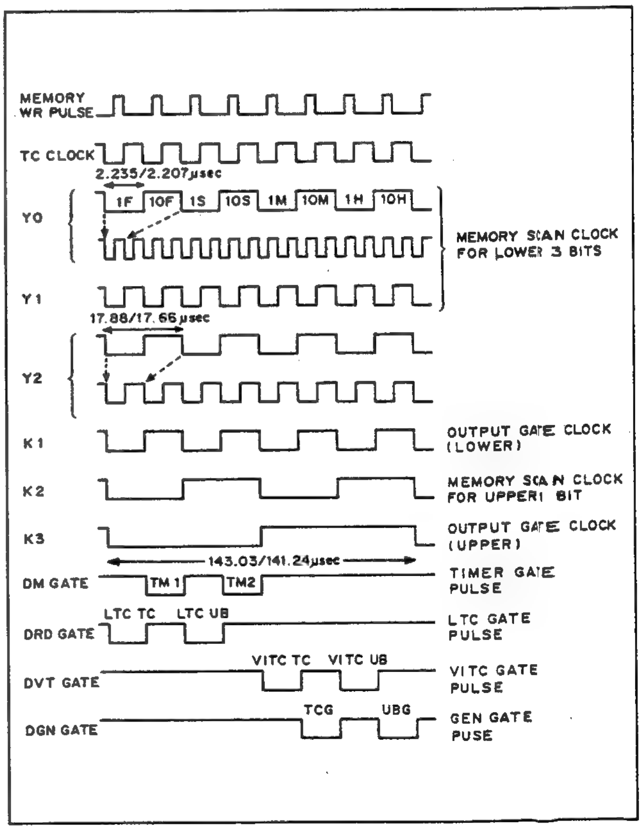


Fig. 4-7-28. REMOTE-3 Output Timing Chart (SY-103)

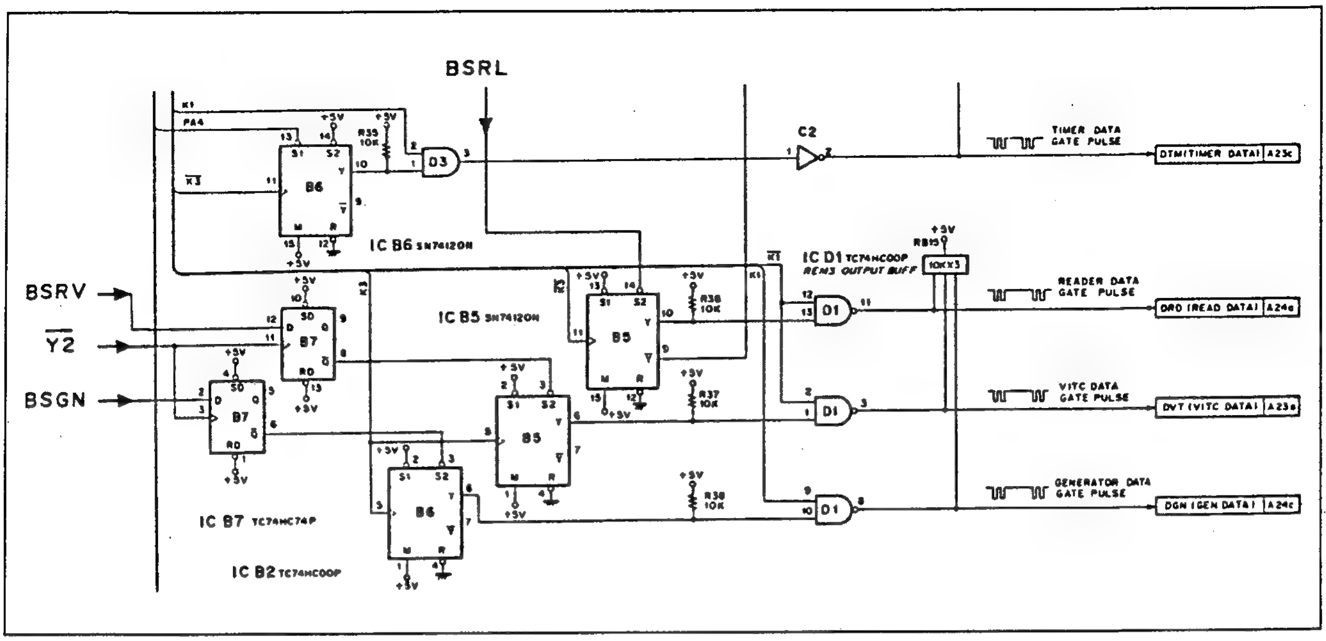


Fig. 4-7-29. REMOTE-3 Output Gate Circuit (SY-103)

ICB3 and B4 are the REMOTE-3 data selector which selects the time code data using the K1 and K3 pulses and which outputs the signals to the REMOTE-3 connector.

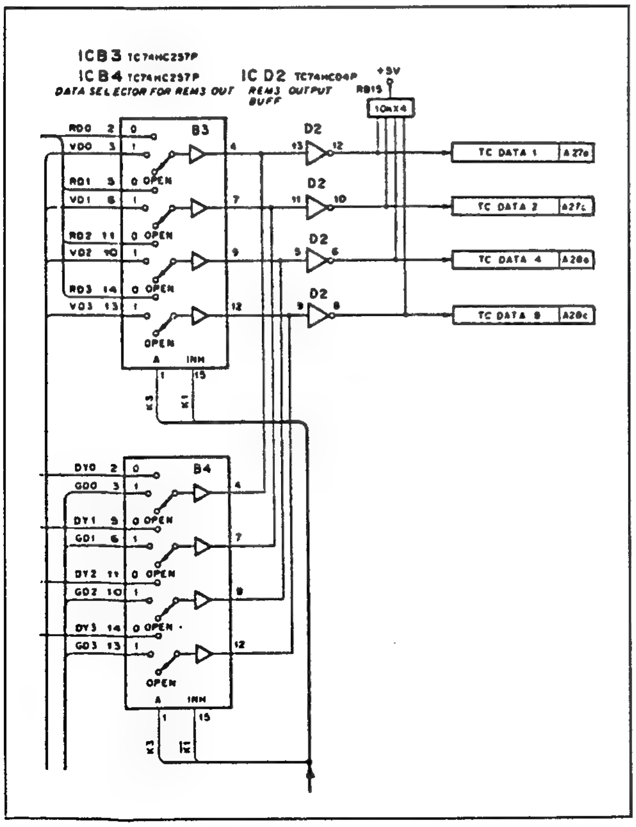


Fig. 4-7-30. REMOTE-3 Data Selector (SY-103)

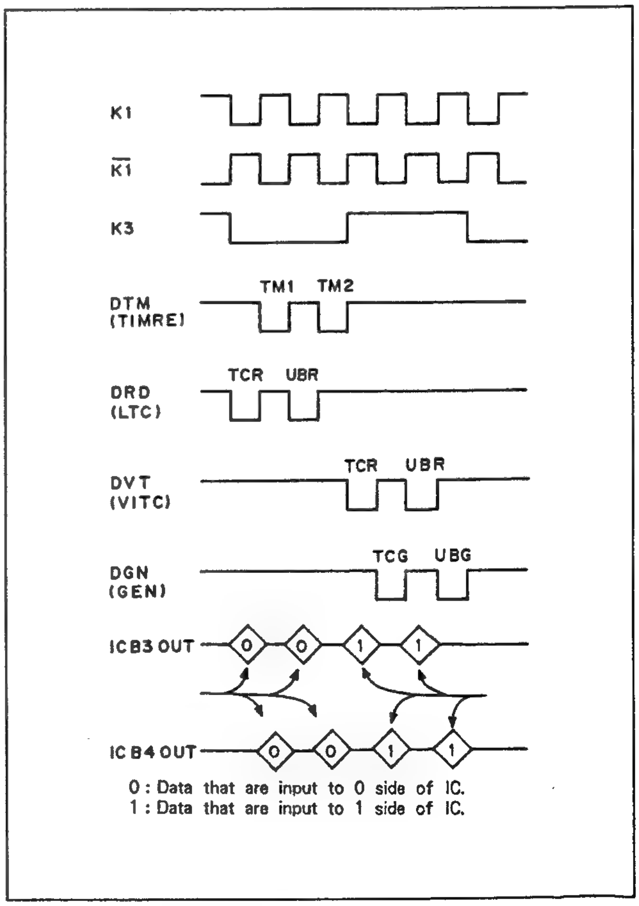


Fig. 4-7-31. REMOTE-3 Data Selector Timing Chart (SY-103)

4-7-3. Control Panel

(1) Outline

The function control panels of the BVH-3000/3100 and BKH-3090 are connected to their respective main units using a single multiple-pin cable (8-pin) in each case. In the case of the BVH-3000/3100, the function control panel can be detached from the main unit and used independently as a remote control unit.

This function control panel is configured with the circuit boards listed below.

- KC-14 board : CPU, power supply, fluorescent display tube driver
- EN-55 board : 21 key switches, LEDs
- DP-63 board : Tape transport control LEDs/switches
- DET-3 board : Search dial pulse detector circuit
- KY-103 board : LEDs, switches, LED decoder/driver, fluorescent display tube

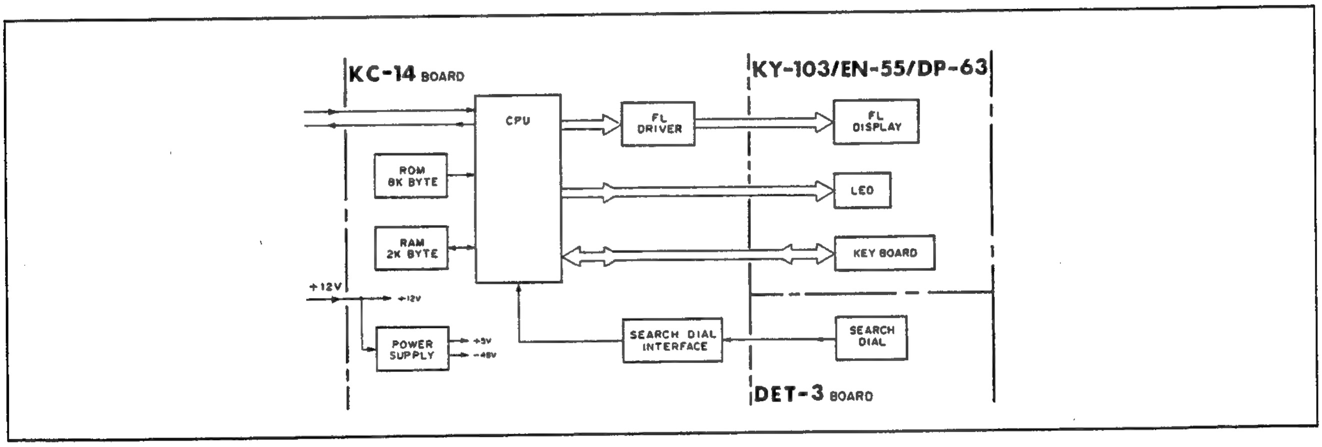


Fig. 4-7-32. Block Diagram of Control Panel

(2) Power supply (KC-14 board)

The +5V, −48V and filament voltage for the fluorescent display tube are generated on the KC-14 board.

The +5V voltage is generated by DC-DC converter ICB3 from the +12V voltage which is supplied to pins 5 and 7 of 8-pin connector CN701. ICB3 oscillates at a frequency of approximately 40 kHz.

ICA4 and Q103 generate the −48V voltage from the same +12V voltage. ICA4 also oscillates at a frequency of approximately 40 kHz. The −48V voltage serves as the power supply for the drive circuit of the fluorescent display tube.

The filament voltage of the fluorescent display tube is generated by Q101, 102 and T101. The 60 kHz square waves which are generated by multivibrator Q101 and 102 are taken out by T101 to provide a 9 Vp-p voltage.

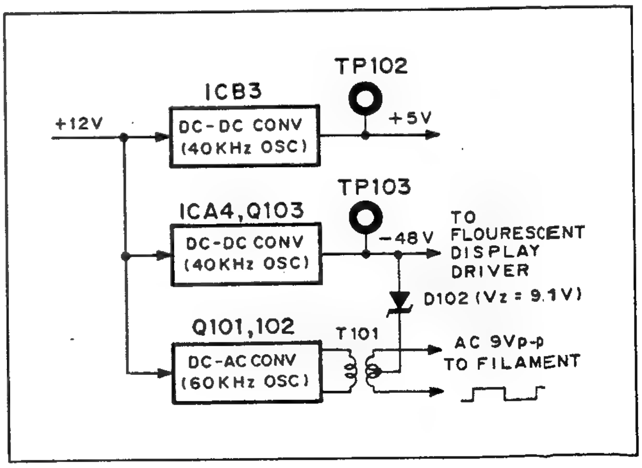


Fig. 4-7-33. Power Supply Circuit of Control Panel (KC-14)

(3) CPU and its peripheral circuits (KC-14 board)

The CPU ICG5 clock signal with its 14.7456 MHz frequency is generated by crystal oscillator X101. The frequency of this signal is further divided down to 1/24 by ICG7 and J7 to provide a clock signal with a frequency of 614.4 kHz and a duty ratio of 50%. This frequency is 16 times higher than the 38.4 kHz frequency of the clock signal which is used for communication.

Q104 serves to generate the low-level CPU reset pulse when the power is switched on and when RESET switch S101 has been pressed.

A non-maskable interrupt (NMI) function is not employed with CPU ICG5. The test mode is initiated by pressing TEST switch S102 which is connected to the INT1 pin (pin 26).

Communication between the BVH-3000 (or the RM-53 board of BKH-3090) is conducted via ICC7 in accordance with the RS-422 format.

The parallel I/O ports of CPU ICG5 are allocated as listed below.

PA7−PA0 : Input port for key data from KY-103/DP-63/EN-55 boards
PB7−PB0 : Output port for key matrix selection of KY-103/DP-63/EN-55 boards
PC7 : Test signal output port (TP109)
PC6 : Display enable port (active high) for fluorescent display tube
PC5 : Dial pulse input port
PC4 : Output port for square waves with a frequency of approx. 4 kHz for the buzzer
PC3 : Dial rotation direction input port
PC2 : 614.4 kHz (16 times the 38.4 kHz frequency used for communication) clock input port
PC1 : Serial data input port
PC0 : Serial data output port
PD7−PD0 : A7−A0 output port/D7−D0 input port
PF5−PF0 : A13−A8 output port
PF6 : Output port (active high) for data latch signals of fluorescent display tube
PF7 : Output port (active low) for scan decoder reset signal of fluorescent display tube.

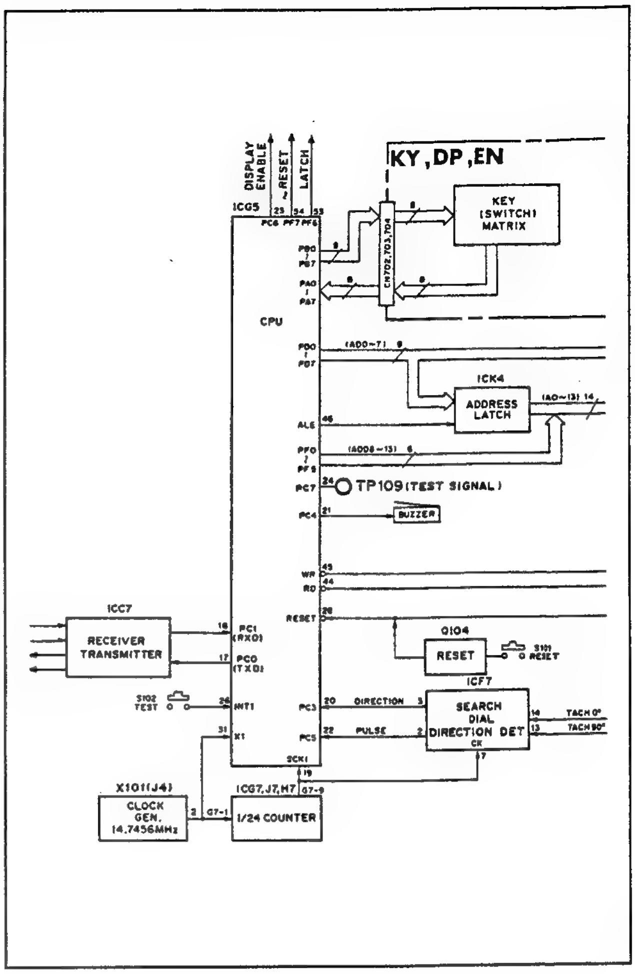


Fig. 4-7-34. CPU and Peripheral Circuits (KC-14)

The addresses of the CPU ICG5 peripheral devices are listed in the table below.

DEVICE	R/W	ADDRESS	SUPPLIED FROM
ROM ICJ5	R	0000−1FFFH	ICG5 PIN-52 (A13)
RAM ICJ6	R/W	2000−27FFH	ICKI7 PIN-3
ND1 (UPPER)	W	3000−3007H	CIF4 PIN-3
ND1 (LOWER)	W	3008−300FH	ICF4 PIN-6
LED LATCH	W	3800−3807H	ICF6 Y7-0

(4) Fluorescent display tube driver (KC-14 board)

CPU ICG5 on the KC-14 board is responsible for controlling fluorescent display tube ND1 and for generating the character patterns.
On its upper and lower lines, the fluorescent display tube displays 40 characters in each case. A character is composed of 5 columns by 7 lines.

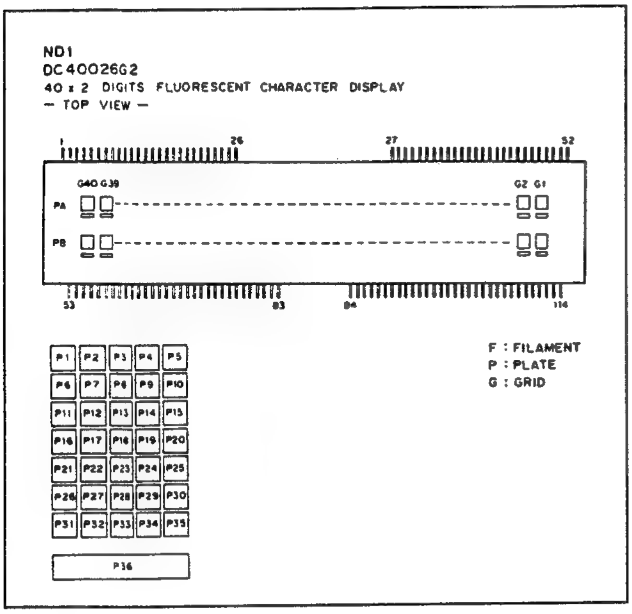


Fig. 4-7-35. Fluorescent Display Tube (ND1/KY-103)

(a) Display pattern latches

The 40 characters on the upper line of fluorescent display tube ND1 are latched to data latch ICM5, K3, J3, H3 and G3 while the 40 characters on the lower line are latched to data latch ICE3, F3, C5, D5 and E5. When the CPU is writing the character data into address 3000−3007H, the upper line 40-character latch signal is output from pin 3 of address decoder ICF4. When the CPU is writing the character data into address 3008−300FH, the lower line 40-character latch signal is output from pin 6 of ICF4.
The strobe pulse which is output from pin 53 (PF6 pin) of CPU ICG5 is supplied to the STRB pin of the data latches. As a result, the parallel data are supplied to the display driver (ICM4, K2, J2, H2, G2, E2, F2, C4, D4 and E4). The strobe pulse is further supplied to the clock input pin of D-type flip-flop ICE7 where the blanking signal is created for preventing the "blur" which arise when the character digits move. The blanking output signal from ICE7 is supplied to AND gate ICD6, it is gated with the display enable signal output from pin 23 (PC6 pin) of CPU ICG5, and it is supplied to the EN pin of the data latch.

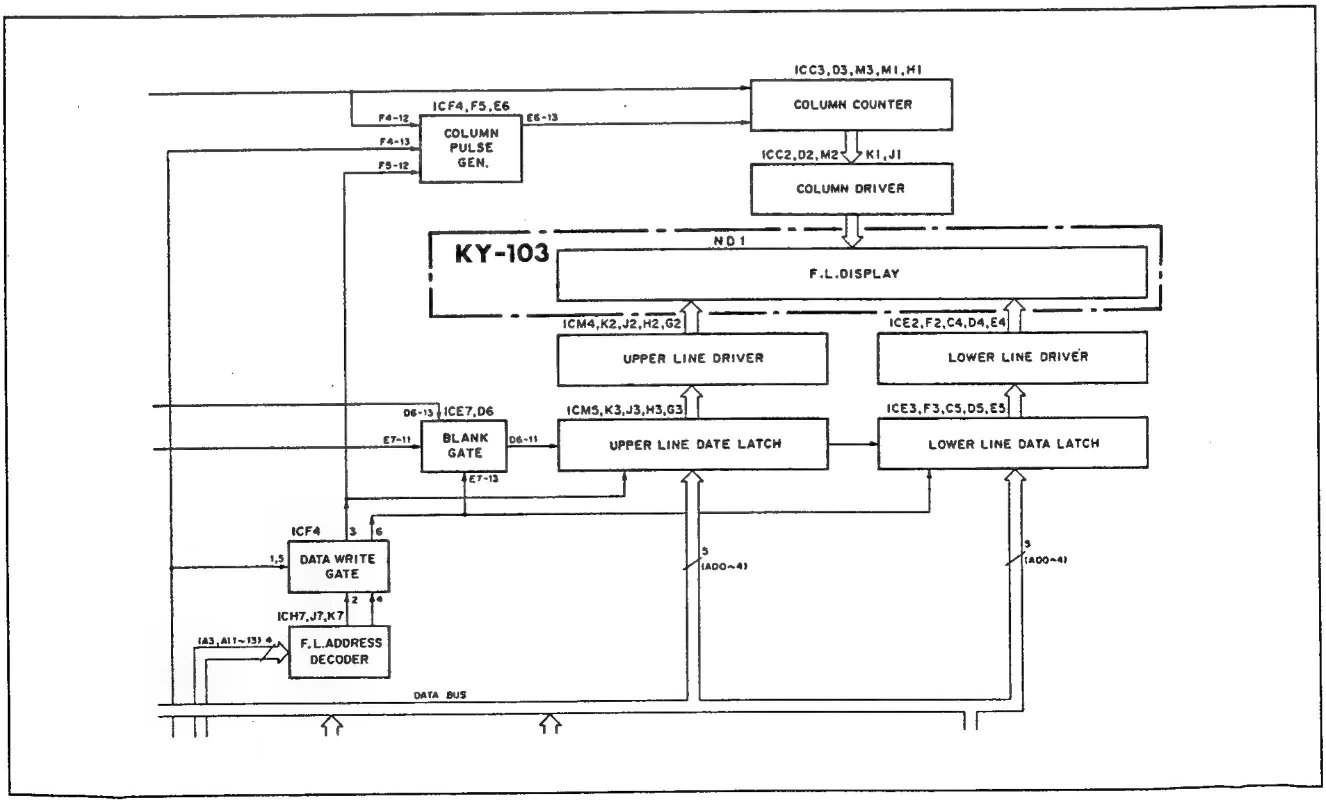


Fig. 4-7-36. Fluorescent Display Tube Driver (KC-14)

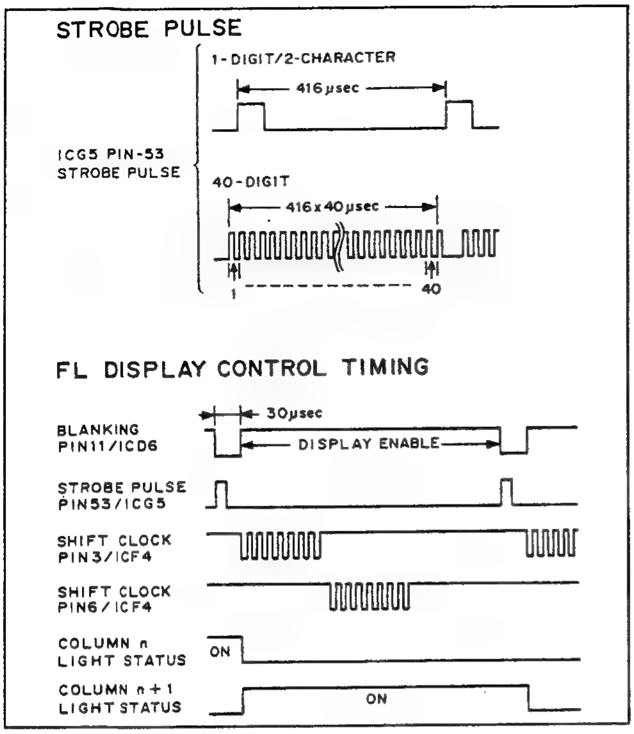


Fig. 4-7-37. Display Pattern Latch Timing (KC-14)

(b) Column decoder/driver

ICC3, D3, M3, M1 and H1 configure the column decoder which is composed of the 9-bit counter and 3-8 decoder. The middle 3 bits (2^3, 2^4 and 2^5) of the 9-bit counter are supplied to the 3-8 decoder. The most significant 3 bits (2^6, 2^7 and 2^8) of the 9-bit counter are compared with the preset value of CS1, CS2 and CS3. It is only when the two values coincide that the data corresponding to the middle 3 bits are sent to the 3-8 decoder and output from the "O1−O8" pins to the grid of the fluorescent display tube. This means that in order to latch the character pattern data of one character, the 3-8 decoder conducts writing 8 times and the output of this decoder is incremented by 1 each time (O1→O8). Only the IC which coincides with the preset value of CS1, CS2 and CS3 is driven.

ICF4, F5 and E6 configure the column clock circuit which is driven by the reset pulse output from pin 54 of CPU ICG5. ICE6 is a monostable multivibrator for setting the pulse width of the column clock pulse to a value equal to or exceeding the rating (1 μ sec).

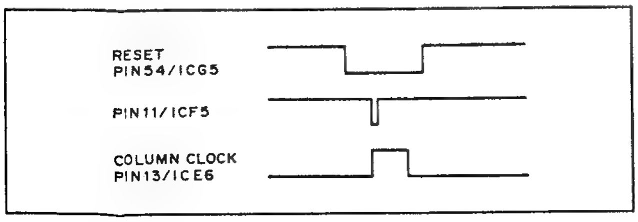


Fig. 4-7-38. Column Resetting, Column Clock Timing (KC-14)

(5) LEDs and clutch driver (KC-14, KY-103 boards)

CPU ICG5 controls the on/off operations of both the LEDs and the clutch on the control panel. Depending on the lamp address "LP7−LP0" from ICF6 on the KC-14 board, IC7, 8, 9, 10, 11 and 12 on the KY-103 board latch "AD7−AD0" and IC2, 3, 4, 5, 6 and 13 drive the LEDs.

The clutch on/off signal is output from pin 16 of latch IC7 and Q1 drives the clutch.

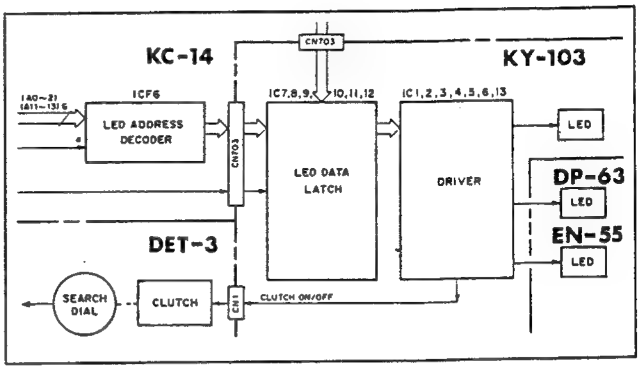


Fig. 4-7-39. LEDs and Clutch Driver (KC-14, KY-103)

(6) Dial pulse detector circuit (KC-14, DET-1 boards)

Mounted on the search dial is a multipolar magnet with an angle resolution of 2.5° . When this dial is rotated, dial pulses "TACH 0° " and "TACH 90° " with a phase difference of 90° are output from the divided magneto-sensing element (DME) on the DET-3 board, these are amplified by IC1 on the DET-1 board, and they are supplied to pins 13 and 14 of rotation direction detector ICF7 on the KC-14 board. The DIR1 signal which indicates the rotation direction of the search dial is output from pin 3 of ICF7 to CPU ICG5 while the dial pulse is output from pin 2 to ICG5. ICF7 is activated by the clock signal with the 614.4 kHz frequency.

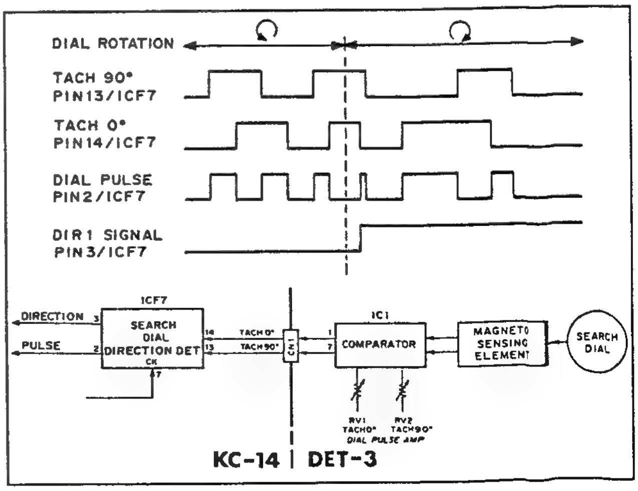


Fig. 4-7-40. Dial Pulse Detector Circuit (KC-14)

4-8. POWER SUPPLY SYSTEM

4-8-1. Outline of Power Supply System

The power supply block of BVH-3000/3100 is the combination of the switching type regulators and series regulators, forming a compact sized, high performance and high efficient power supply. This power supply block can accept AC power input in the range of 100V through 240V, having no need to care for local power supply voltage condition in use.
This power supply block consists of the three printed circuit boards of SP-01 board, SP-02 board and SP-03 board. The SP-01 and SP-03 boards provide the fixed output voltages from these power supply regulators while the SP-02 board provides the variable output voltage to be used in the various motors.

(1) SP-01 board
The SP-01 board consists of the circuits such as the primary rectifier circuit, the starter circuit, ±5V regulators, the regulator for reference +17V and the protection circuits which protect the whole system in case of shorting-circuit and excessive output voltage.

(2) SP-02 board
The SP-02 board consists of the 90V preliminary regulator circuit, and the variable voltage outputs power supply circuits which supply powers to the supply reel motor, the take-up reel motor, the drum motor and to the capstan motor. The variable output voltage power supplies are receiving the input control voltages from the respective motor driver circuits and provide the output voltages in proportion to the input control voltages. These circuits protect the driver circuits using the excess power protection circuits.

(3) SP-03 board
The SP-03 board includes the ±12V regulators, ±18V regulators, +13V regulator for the blower motor, +12V regulator for fan motor and the PA detecting circuit that is detecting the power active signal when the power input/output conditions are normal.

4-8-2. SP-01 Board

(1) Primary rectifier circuit (SP-01 board)

When the S1 power switch is turned on, the commercial AC power input is supplied to the power supply block through the CB1 circuit breaker on the rear panel. This AC input is bridge rectified by the D101 diode bridge through the L101 and L102 choke coils and the L103 power line filter. The rectified AC power is passed through the R101, R102 and RY-101 rush current protector, and is sent to the group of smoothing capacitors.
The other power line filter L104 is installed even after rectification for the purpose of suppressing the switching regulator noise in the vicinity of its generating area. The power line filters are installed in the SP-02 and SP-03 boards too.

(2) Starter (SP-01 board)

IC102 and T105 are the self-exciting type switching regulator circuit, functioning as the starter circuit. When power is turned on, the starter begins to work and supplies the power to the +5V switching regulator control circuit board (UR-20-C1 board). After the +5V power supply system has built-up its operation, the +5V switching regulator sends the control signal voltage that is generated inside, to D107 that stops the starter circuit operation. The D124 and D223 diodes work as the power switches for the control board.

(3) +5V power supply (SP-01 board)

The +5V power supply circuit consists of the half-bridge inverter circuit employing the PWM control method. It supplies not only +5V but also −5V and +17V control preliminary output. The +5V is fed back to IC171 on the UR-20-C1 board for voltage control.

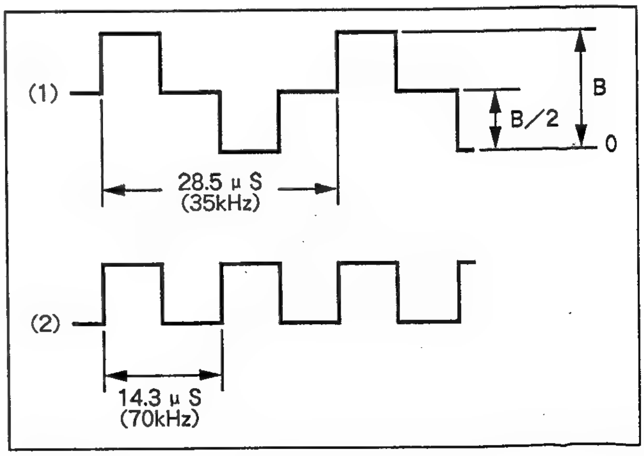


Fig. 4-8-1. Switching Waveform (SP-01)

The half-bridge inverter circuit is made of Q101, Q102, C128, C129 and T101. The primary side rectified voltage is converted to the alternating voltage as shown in Fig.(1), and is sent to the T101 converter transformer and the secondary voltage is obtained in proportion to the winding's turn ratio of the T101 transformer. The secondary output voltage is rectified by the D201 and D202 fullwave rectifier to generate the output shown in Fig.(2). It is smoothed out by the smoothing circuit of L201, C214 through C216 where alternating current is converted to DC current. The output voltage level is determined by the primary rectified voltage and the ON／OFF ratio of the repeating signal waveform. The DC output voltage is passed through the filter consisting of L202, L203, C217 and C218, and is sent to respective loads through connectors. The supplied voltage across the loads is fed back to IC201 on the UR-20-C1 board through the filter on the UR-20-F board, so that it is compared with reference voltage. The difference voltage between load's voltage and reference voltage is added to the IC171 error amplifier where this difference voltage regulates the output pulse width until the output load voltage is regulated.
The IC171 output pulse signal is sent to the Q101 and Q102 switching transistors through the Q171 and Q172 drivers and the T103 and T104 drive transformers. This power supply has the protection against overload that the primary current is detected by T102 and is fed back to IC171 in order to control the PWM pulse width. The characteristics of excessive-load protection circuit is determined by R179, R182 and R185. The output voltage is detected by D178 and D176. When an excessive voltages should be detected, it drives the D177 thyristor to stop output. The rush current caused by the charging current of the primary circuit's smoothing capacitors in the timing of power on, is limited by R101, R102 and RY101. When the switching regulator starts working, the rise-up of the output voltage is controlled to become slow rise-up by means of C178 and R195 of the UR-20-C1 board. The excessive current is thus prevented from flowing. Q174 is the detector circuit for the voltage to be supplied to the UR-20-C1 board. The IC171 is prohibited from functioning until the supply voltage reaches higher than 9V. During when the input voltage remains low, IC171's internal switching transistor has longer ON period, so that IC171's PWM modulation working range is limited by R189.

(4) −5V power supply (SP-01 board)

The −5V power supply is obtained from the +5V power supply circuit. The T101 +5V power's converter transformer has its secondary winding output that is smoothed out by D203, L204 and C219 and is then regulated by the series regulator consisting of Q209 and IC203 so that the −5V power is generated. The −5V power supply system also has the voltage detection across the load in the same manner as in the +5V power supply system. The −5V SENSE signal thus obtained, is fed back and is used for regulation. The excess current is detected for power supply protection by R242 through R245, R263, IC203 and Q216, and the excess voltage is detected by Q206 and D211 for the purpose of power supply protection.

(5) Control-use +17V power supply (SP-01 board)

The control-use +17V power supply is obtained from the +5V power supply circuit. The T101 +5V power's converter transformer has its secondary winding output that is smoothed out by D204, L205 and C221, and is regulated by the series regulator consisting of IC201, Q202 and Q203 so that the control-use +17V is generated. When the +17V output voltage becomes higher, the load for +5V power system is lightened by D208, Q205 and Q204 so that the output voltage should be corrected. The excess voltage is detected by D207 and the excess current is detected at the same time by PS202 and are used for their protection.
On the other hand, because the variable output voltage power supply systems are made to floating, the T101's secondary winding output is again separated by T201 and is then smoothed out by D205, L206 and C222 to generate the control-use +17V (F+17V) that is sent to the SP-02 board. The excess voltage is detected by Q201 and excess current is detected by PS203 and are used for system protection.

(6) Sync pulse generator (SP-01 board)

The one-shot multivibrator IC207 is the sync pulse generator. The generated sync pulse is supplied to the SP-02 and the SP-03 boards through the buffers Q214 and Q215 at the next stage, so that the switching regulators in the SP-02 and SP-03 boards are made synchronized. Because the SP-02 board's switching regulator that is supplying power to the various motors, has the floating output, the Q215 buffer output is supplied outside through the T202 pulse transformer.

(7) Low output and high output voltage protection (SP-01 board)

When the output voltage becomes too low, the positive voltage outputs of the fixed output type switching regulators and series regulators, are compared with the reference +5V by Q212 while their negative output voltages are compared with the reference −5V by Q213 for detection. In the variable output type power regulators, the pre-output voltage is used for detection. When the excessive low output is detected, the LVP signal is sent from the SP-02 and SP-03 boards to Q212. If the outputs are short-circuited, and the shorting condition remains longer than the pre-set time that is determined by the time constant of R261/C231 or R254/C179, the D177 is turned on to stop the +5V power supply and then stop the all regulator outputs. If all regulator outputs should be stopped, turn off the equipment POWER switch and wait until the primary circuit's rectifying voltage is discharged (approx. one minute). Q211 is the circuit that resets the C231 timer when the power is turned on. D207 is the excessive high output voltage detector that stops the regulator outputs when any trouble is detected.

4-8-3. SP-02 Board

(1) Control-use F17V power supply (SP-02 board)

This circuit consists of the Q209, Q210 and IC202 series regulator, using "F+17V" that is supplied from the SP-01 board.

(2) 90V pre-regulator (SP-02 board)

This circuit consists of Q101, Q103, T101, T102, T103, T104, UR-20-C4 board and peripheral circuits. It provides 90V output with maximum 150 Watts that are used for pre-power voltage supplies for the various motors. The circuit configuration is, same as +5V power supply circuit, the half-bridge inverter type switching regulator, using externally synchronized PWM control system. The bridge type rectifier circuit of D202 and D203 is used. Considering the case of non-load conditions, the R202 and R203 idling resistors are inserted. D228 and D477 are installed for the purpose of regulator protection.

IC201 and Q211 detect the overall power consumption of total motor systems so that the power supply regulator should be protected from the excessive heavy load. When the excessive load is detected, the "POWER SENSE" signal is generated to indicate this condition and is sent to the SV-90 board.

When the pre-regulator output voltage becomes too low due to its internal trouble, it is detected by Q214 and D219 and the LVP signal is sent to the SP-01 board through the IC205 photo-coupler so that all systems stop operation.

(3) S REEL VH power supply

This circuit is the variable output voltage power supply for the supply reel motor. This is the chopper type dc-dc converter circuit that operates with externally synchronized PWM system. The dc-dc converter circuit is made of Q201, Q202 and D203. Q201 and Q202 work as the switcher while D203 works as the fly-wheel diode. They are connected to the next circuit of L203 and C207 smoothing circuit. The "S-REEL VH CONT" voltage that is supplied from the motor driver RM-43 board is sent to the dc-dc converter through the UR-20-C6 board. The UR-20-C6 board controls the voltage amplification gain of this regulator so that the output voltage becomes ten times of the input voltage. Q672 of the UR-20-C6 board is the voltage detector of the "S-REEL VH CONT" voltage, stops output when the output voltage becomes too low.

T205 on the SP-02 board works as the input current detector. Because the input voltage and amplification efficiency maintain a constant relationship, the UR-20-C6 board regulates the output power to be maximum 80 Watts. When the output becomes higher voltage with lower current, internal diodes tend to generate the non-linear characteristics. The R257 resistor is providing offset to the T205 transformer that cancels the diodes' non-linearity and improves the power protection accuracy.

The peak value of the switching current is detected by IC203 and D232 that functions to protect the power supply circuit from the excess output current when the output becomes lower voltage. The detected signal is sent to the D477 gate through D230, D229, Q212 and Q213, that puts D477 on which stops the work of the 90V pre-regulator.

(4) T REEL VH power supply (SP-02 board)

This is the power supply for the take-up reel motor. The circuit configuration of this circuit is same as that of the S REEL VH power supply circuit.

(5) CAPSTAN VH power supply (SP-02 board)

This is the power supply for the capstan motor. The circuit configuration of this circuit is same as that of the S REEL VH power supply circuit, but this circuit has the amplification gain of five times for the input "CAP VH CONT" signal and the maximum output power is 20 watts. D238 and D239 are the high output voltage detection circuit. When the output voltage becomes high, the output is stopped in order to protect the driver circuit.

(6) DRUM VH power supply (SP-02 board)

This is the power supply for the drum motor. The circuit configuration of this circuit is same as that of the S REEL VH power supply circuit, but this circuit has the amplification gain of five times for the input "DRUM VH CONT" signal and the maximum output power is 45 Watts. The protection against the high voltage output works in the same manner as that of the CAPSTAN VH power supply.

4-8-4. SP-03 Board

(1) ±18V power supply (SP-03 board)

The ±18V power supply circuit has the same circuit configuration as that of the +5V power supply, of the half-bridge inverter type switching regulator, of the externally synchronized PWM control system. It is controlled by the UR-20-C5 board. Because the load of the ±18V power regulator has the wide range of variation, the idling resistor of R269 is used.

(2) +13V blower solenoid power supply (SP-03 board)

The +13V power supply circuit has the same circuit configuration as that of the +5V power supply, of the half-bridge inverter type switching regulator, of the externally synchronized PWM control system. It is controlled by the UR-20-C2 board. In order to use the air-threading blower in the floating circuit, the L210 filter is inserted.

(3) ±12V power supply (SP-03 board)

This ±12V power supply is consisting of series regulator, and is connected to the afore-mentioned +13V power supply circuit and is output. The ±18V is used for controlling power source of this power supply circuit. The output voltage across load is detected in the same manner as ±5V power supply circuit. The detected voltage across the load is called as ±12V SENSE that is fed back for power supply regulation.

(4) +12V fan motor power supply (SP-03 board)

The power source for the +12V fan motor is obtained by connecting the series regulator IC206 in the output of the +13V blower solenoid power supply circuit.

(5) Power active detection circuit (SP-03 board)

This circuit consists of Q213, IC205, and Q207 through Q210.
The circuit consisting of Q213 and IC205 functions to detect whether the power supplies are working normally or not. If the output voltage is detected to be too low, the detected output is sent to respective power supplies through the driver circuits of Q207 through Q210.
The pin 5 of IC205 is receiving the secondary winding's output voltage of T101 of the +13V switching regulator through D201. The voltage level of the primary circuit rectifying circuit is detected in this way. When the voltage of the primary circuit rectifying voltage is too low, Q210 is turned off. Q211 and Q212 are the detection circuit for excessive high output voltage of −13V power supply. If the excessive high output voltage is detected, the "STOP" signal is sent to the SP-01 board.

SECTION 4
THEORY OF OPERATION

4-1. OUTLINE

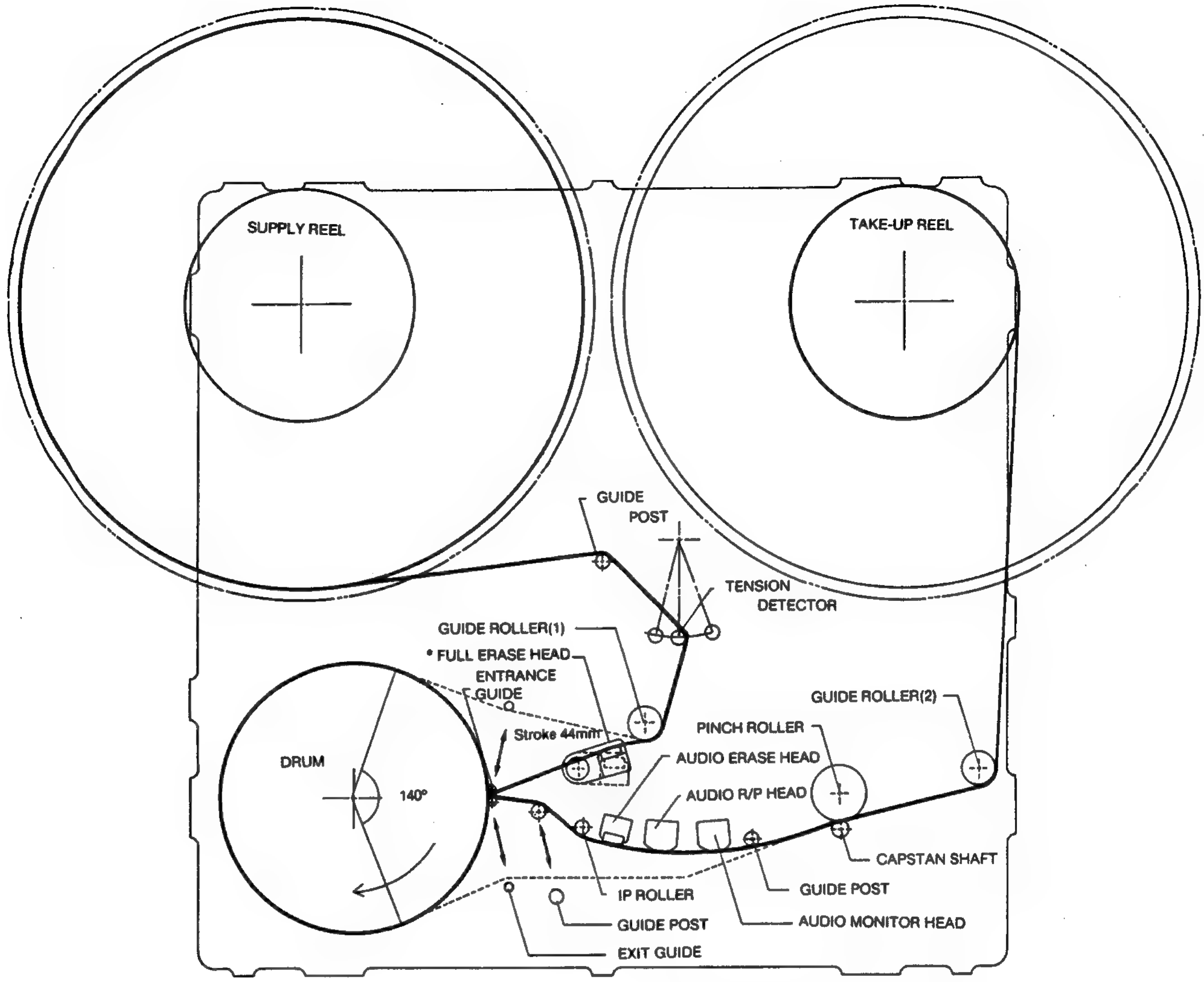
The BVH-3000/3100 is a direct high band FM recording 1-inch helical scan VTR based on the SMPTE type C format (or the EBU type C format in the case of a PAL/SECAM model). The only difference between the BVH-3000 and the BVH-3100 is that the former has a sync head whereas the latter does not.
The PAL/SECAM model is also available with 4-channel audio tracks.

		Sync head	Audio channels
NTSC	BVH-3000	Yes	3
	BVH-3100	No	3
P/S	BVH-3000PS	Yes	3
	BVH-3100PS	No	3
	BVH-3000PS-A4	Yes	4
	BVH-3100PS-A4	No	4

An air threading system employing moving guides, blowers, and a dedicated reel is used, greatly simplifying tape threading.
The timer roller and the take-up side tension arm have been removed from the tape transport system for ease of maintenance. Refer to Fig. 4-1-1.
Figure 4-1-2 shows the tape pattern for the NTSC model, and Fig. 4-1-3 shows the tape pattern for the PAL/SECAM model.

The BVH-3000/3100 system is controlled by the CPU. The entire setup procedure from setting the system conditions to setting the test mode can be done by making menu selections using the keys on the control panel. The CPU controls communication with the control panel and external devices, controls the system control circuit, and servo circuits (S reel, T reel, capstan, and drum), and also controls the audio, video, and TBC circuit mode according to the system control circuit, servo circuit, and menu settings. An RS-422 serial interface is provided for communication between the system and external control equipment. By using an optional BKH-3002, serial communication can also be done with an RS-232C interface.

The BHV-3000/3100 is provided with a simultaneous playback function and a DT (dynamic tracking) function. The video PLAY head is a DT head. The DT head uses an auto jump control function, permitting stable and noiseless playback between −1 and +3 times normal speed.
The SC-H phase of the tape signal and reference signal is displayed on the front panel. This enables the continuity of the video signal at the editing point to be checked prior to editing. (In the case of an NTSC model, the BHV-3000/3100 outputs the video signal at an SC-H phase which matches the RS-170A. Also, if the SC-H phase of the input signal matches the RS-170A, color framing adjustment is unnecessary.)
The TBC processor can select either a standard processor BKH-3010/PR-91 board or a higher performance BKH-3050/PR-96 board (in the case of a PAL/SECAM model, the BKH-3020/PR-92 board or the BKH-3060/PR-98 board). The BKH-3050 (BKH-3060) uses a new Y addition method to improve the up and down motion of the screen and also flicker, during DT playback.
The TBC circuit has a field freeze function for preventing tape damage during still playback.
By adding a BKH-3080 (NR-26 board), audio channels 1 and 2 will become Dolby A or Dolby SR noise reduction systems.
The generator/reader of the time codes (LTC and VITC) is built into the unit.



*FULL ERASE HEAD FOR NTSC MODEL
V/S ERASE HEAD FOR PS MODEL

Fig. 4-1-1. Tape Transport

4-2. AUDIO SIGNAL SYSTEM

4-2-1. Outline of Audio Signal System

The BVH-3000/3100 audio system has the following circuit configurations as described below.
The numbers of the audio channel are three channels of audio-1, 2 and 3 in the NTSC/PS model and are four channels of audio-1, 2, 3 and 4 in the PS A4 model.
The audio signal system consists of the record/playback circuit of each channel and the CONFI signal playback monitor circuit. But the CONFI playback is possible only in the two channels of audio-1 and 2 in the NTSC/PS model and in the three channels of audio-1, 2 and 4 in the PS A4 model. The bias and erase circuits which reqires during record mode are also included in this circuit.
The audio-3 channel has the LTC processing circuit that enables the time code signal's record/playback, in addition to the normal audio signal's record/playback circuit like other channels.
The BVH-3000/3100 audio circuit has the following features.

- The transformerless balanced input/output circuits are employed that realize the good low frequency response characteristics.
- The record and playback mode switching for the audio R/P head, is done by means of an electronic switch using FET, thus reliability of this circuit is improved and the on/off timing characteristics is also improved.
- The audio phase adjustment for the audio channel-1 versus channel-2 during record mode, is made possible that provides the high quality stereophonic recording.
- When the audio-1 and 2 mix mode is used, the phase difference between the both channels in the stereophonic mode can be easily confirmed.

The audio system of this equipment consists of the following five circuit boards. But the audio-4 is available exclusively only in the PS-A4 model.

(1) AU-88 board
The AU-88 board comprises the input amplifiers, output line amplifiers, record/playback equalizer circuits and also the input/output circuits that interface the various control signals, for all the audio-1, 2, 3 and 4 channels.
(2) AP-15 board
The AP-15 board comprises the record/playback amplifiers for the audio-1, 2, 3 and 4, the CONFI playback amplifiers for the audio-1, 2 and 4, the CTL record/playback amplifier and the bias/erase amplifiers for all channels.
(3) MA-26 board
The MA-26 board comprises the monitor-L and -R channel output amplifiers.
(4) VR-51 board
The VR-51 board comprises the record level adjustment circuit and the playback level adjustment circuit for all channels.
(5) BC-12 board
The BC-12 board has the bias level adjustment controls that are connected to the AP-15 board.

The record/playback circuits of the audio signals are mainly located in the AU-88 board that is housed in the amplifier chassis. The meter panel is including the VR-51 board, MS-21 board, SW-195 board and LP-34 board and is joined to the AU-88 board with screws. The AU-88 board, MA-26 board and AP-15 board are plugged into the mother board MB-140 for connections.

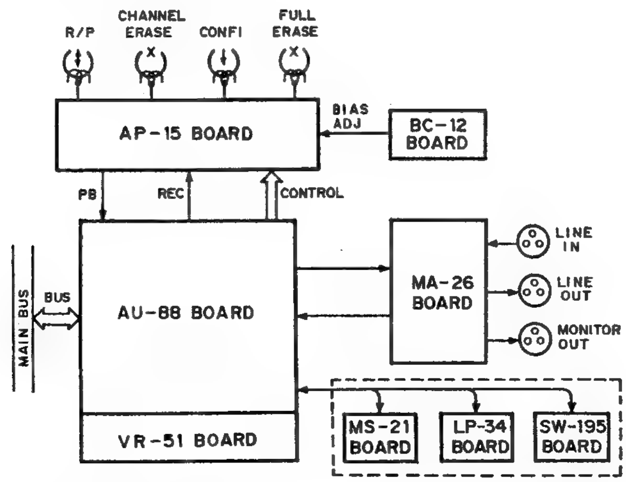


Fig. 4-2-1. Audio Signal System Configuration

The audio system has the following eight major circuit blocks. The circuit description is provided for each block by block.

(1) Audio signal record system
(2) Audio signal playback system
(3) Crosstalk canceller
(4) Audio monitor system
(5) Audio bias system
(6) Erase system
(7) Audio control signal system
(8) Time code system

4-2-2. Audio Signal Record System (AU-88, AP-15 Boards)

The signal flow of the audio signal record system, is shown in the Fig. 4-2-2.

The audio input signal that is fed to the LINE INPUT connector, passes through the MA-26 board and the MB-140 board, and is then sent to the AU-88 board where proper input level and input impedance are selected and the balanced input is converted to the unbalanced input. The input signal is then sent to the Input Level Control circuit (VR-51 board). The signal passes through the TAPE/EE switch, receives the record level adjustment and the equalizer adjustment, passes through the crosstalk canceller, and is then sent to the AP-15 board's record amplifier. The audio record signal input at the AP-15 board, passing through the record amplifier and bias trap. The audio signal and the recording bias are added together and are then sent to the audio R/P head.

(1) Input circuit (AU-88 board)

Because the audio-1, 2, 3 and 4 have all the same circuit configurations, the audio-1 only is described. The circuit is shown in Fig. 4-2-3.

The signal is input to IC103 as the balanced signal that is converted to the unbalanced signal by IC104. C177 and C178 are the capacitors that reject the dc offset component in the input signal.

Resistors R101 through R104 and R231 through R233, are prepared in order to match the input impedance of 10k Ω, 600 Ω and 150 Ω. The desired input impedance can be selected by the combinations of the soldering jumpers in this circuit and by combination of JP101 and JP102. Only the channel-3 can select the input impedance of 47k Ω.

Resistors R105 and R106, and diodes D101 through D104 are used for input protection of IC103. Resistors R109 and R110 are used to determine the amplification gain.

Fig. 4-2-4 shows the channel-3 circuit. Unlike the other channels, the channel-3 accepts the MIC input as well as LINE input so that an exclusive gain-up amplifier is added in channel-3 circuit that amplifies the MIC input signal.

When a MIC is selected by menu, IC505 is turned off so that IC504 becomes a high gain amplifier, enabling the use of microphone.

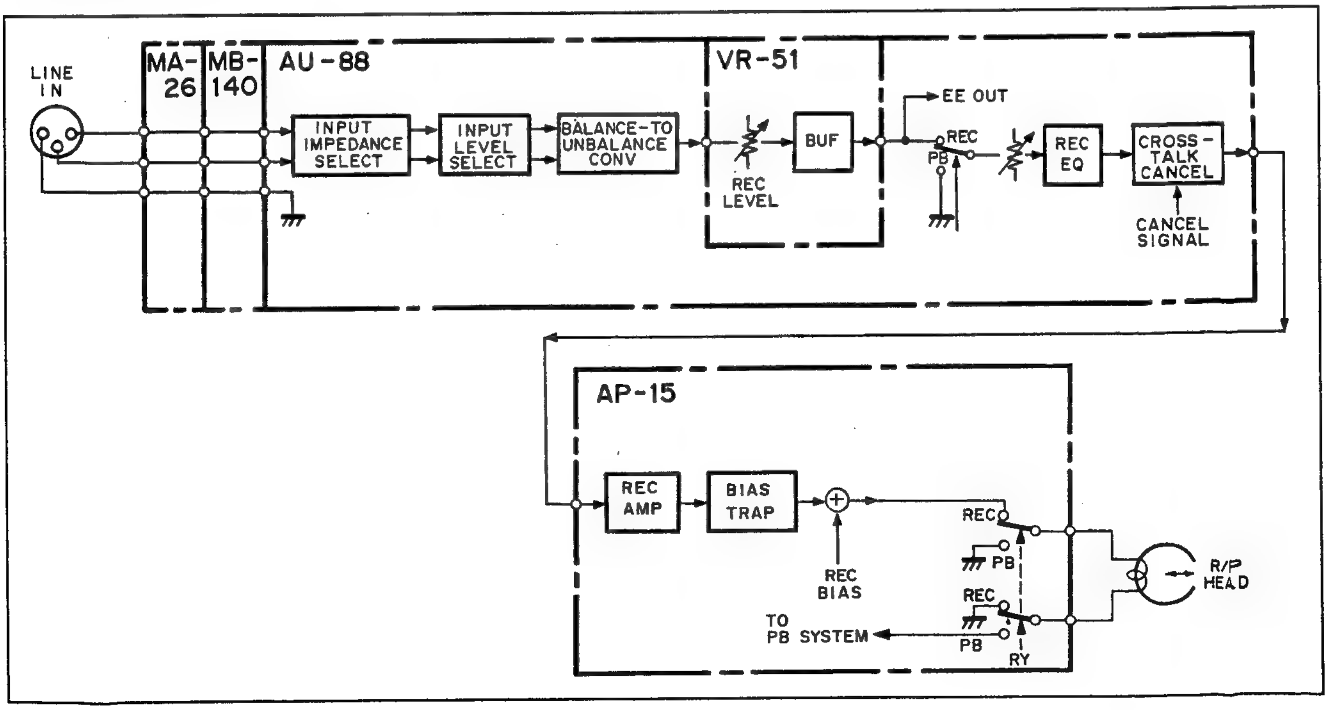


Fig. 4-2-2. Audio Signal Record System

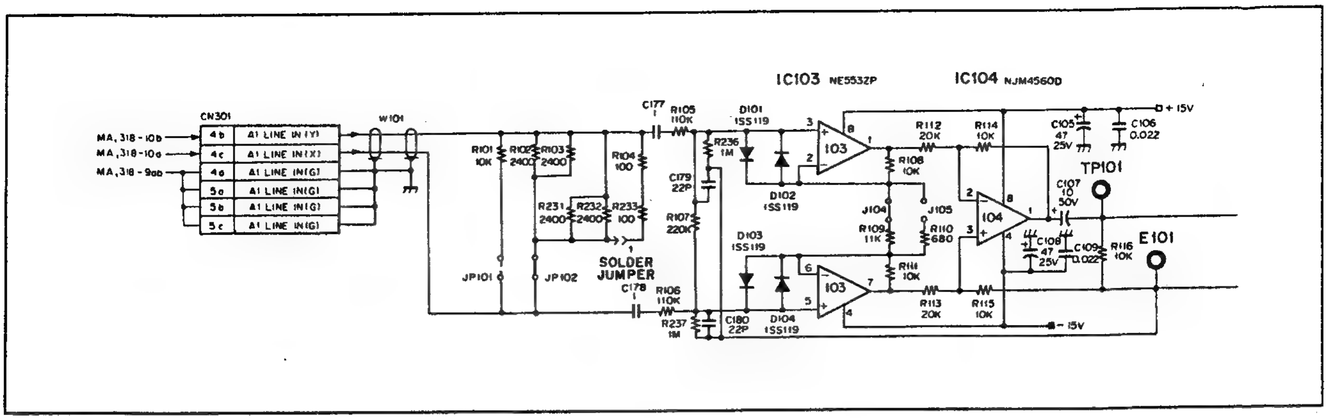


Fig. 4-2-3. Audio-1 Input Circuit (AU-88)

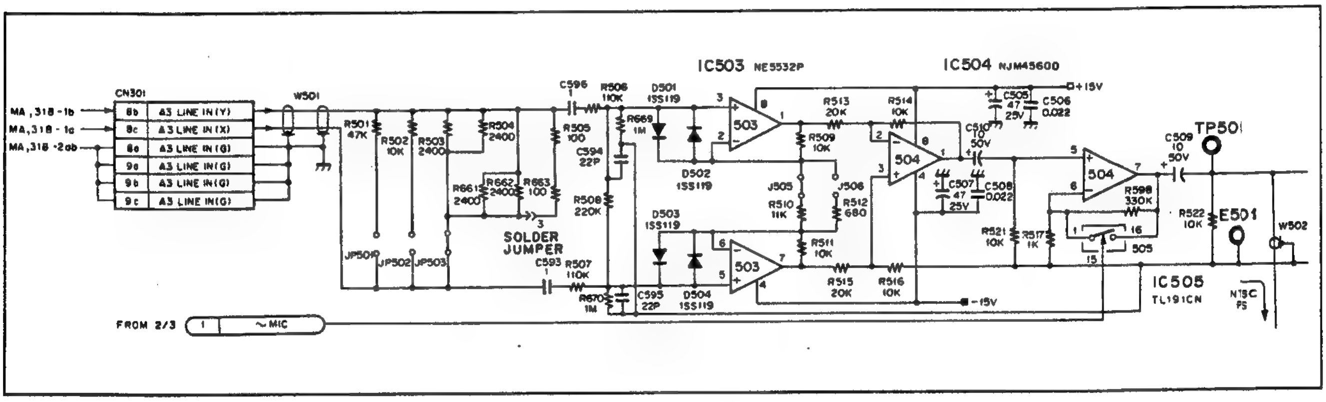


Fig. 4-2-4. Audio-3 Input Circuit (AU-88)

(2) Record/playback selector (AP-15 board)

The record/playback selection of the R/P head is accomplished by FET. Fig. 4-2-5 shows the fundamental circuit.
When the REC/PB signal is "L" level, meaning that the mode is record mode, Q1 is turned off while Q2 is turned on. So, the record amplifier's output signal is sent to the R/P head through the dc-cut capacitor, the constant current resistor and the bias trap circuit.

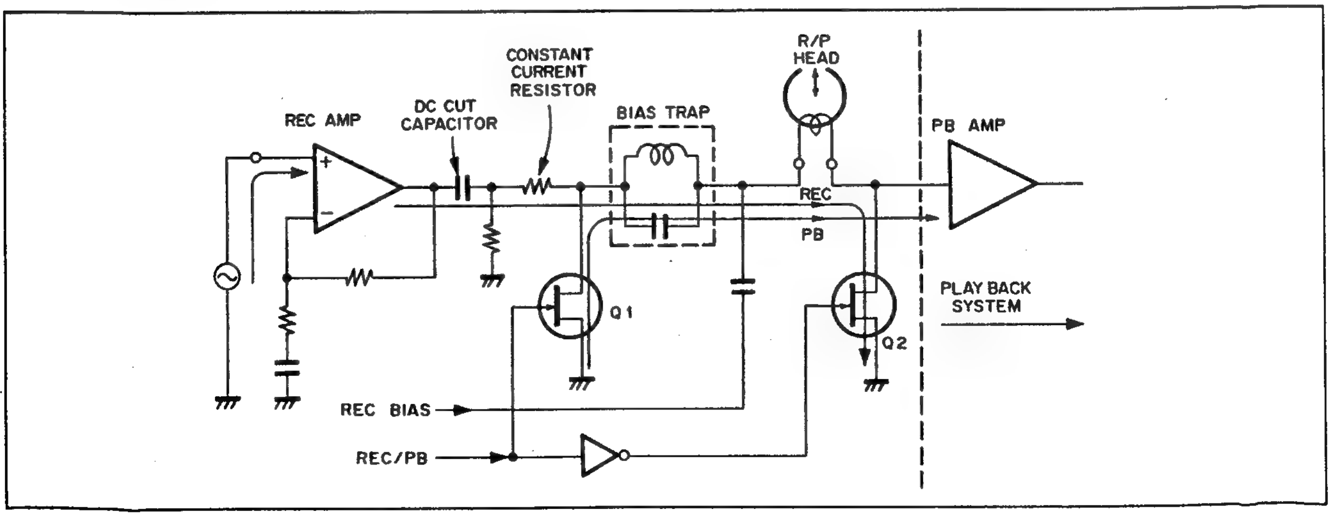


Fig. 4-2-5. Record/Playback Selector Fundamental Circuit (AP-15)

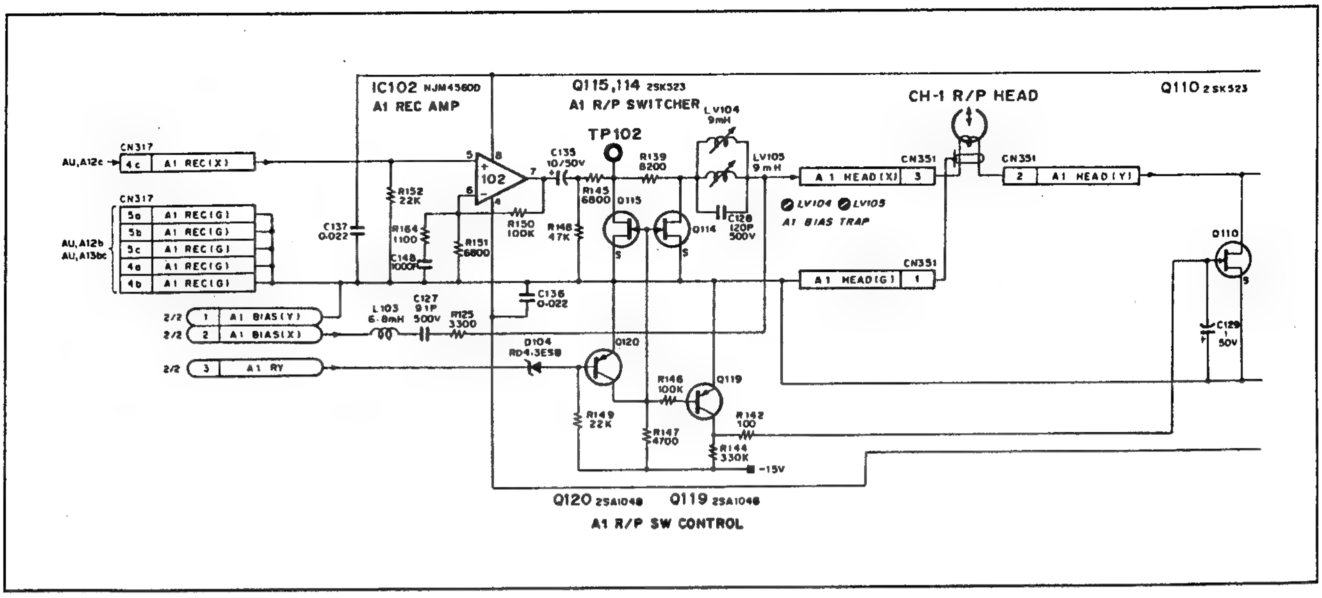


Fig. 4-2-6. Audio-1 Record/Playback Selector (AP-15)

The actual circuit is shown in Fig. 4-2-6. Because all the audio-1, 2, 3 and 4 channels have the same circuit configurations, only the audio-1 channel is described. C135 is the dc-cut capacitor that prevents the dc-current from flowing through the R/P head so that the R/P head should not get magnetized by the dc-current. Transistors Q114 and Q110 are the record/playback switching FETs. Q115 forms the record muting circuit with R145, that prevents the record circuit's noise from leaking into the playback circuit. Inductors LV104 and LV105 and capacitor C128 are the bias trap forming the parallel resonant circuits. Here, LV104 and LV105 are connected in opposite polarities each other so that external noise like hum is cancelled even though it leaks into LV104 and LV105, and the noise will not be recorded on tape.

(3) Record phase adjustment circuit (AU-88 board)

This circuit shifts the signal phase alone, while the original record signal amplitude is maintained. The audio-1 circuit does not have the phase adjusting circuit but the audio-2 has the phase adjusting circuit so that the correct phase relationship between the CH-1 signal and the CH-2 signal is maintained by adjusting the audio-2 signal phase. By using this adjustment, the phase difference between the audio-1 signal and the audio-2 signal can be minimized.

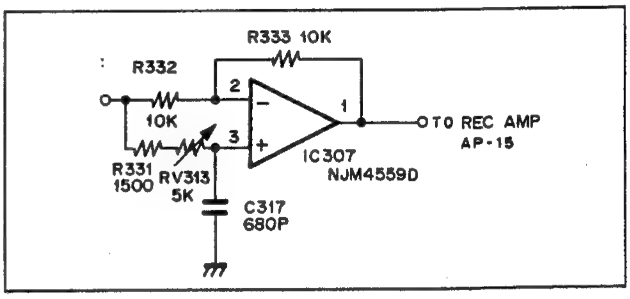


Fig. 4-2-7. Audio-2 Record Phase Adjustment Circuit (AU-88)

(4) Record system frequency response

The record system frequency response is shown in Fig. 4-2-8. Various losses incurred in the record system are compensated with this characteristics curve. Because the NTSC model and the PS model have the different time constant for playback equalizer's low frequency range, the record systems also have different low frequency response.

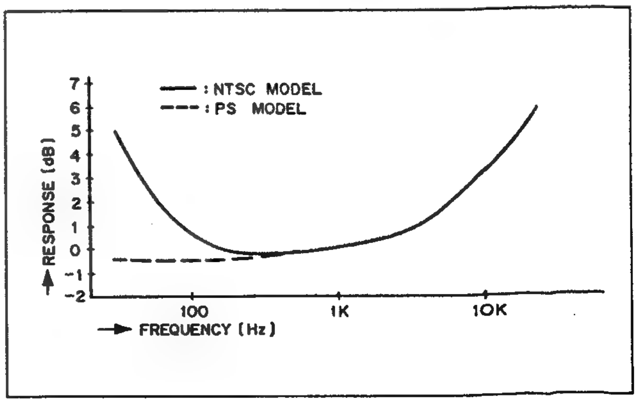


Fig. 4-2-8. Record Equalizer Frequency Response (AU-88)

4-2-3. Audio Signal Playback System (AU-88, AP-15 Boards)

The playback system amplifies the R/P head's playback signal and provides the various signal processing for the playback signal until the playback signal is fed to the LINE OUT connector for output. The playback system's signal flow is shown in Fig. 4-2-9.

The playback signal that is picked up by the R/P head is amplified by the AP-15 board's playback amplifiers and then sent to the AU-88 board.

The playback signal passes through the crosstalk canceller, the bias trap, the playback equalizer, the muting, and the attenuator circuits located in the AU-88 board and then sent to the VR-51 board for playback level adjustment.

After playback signal level is adjusted, the signal is sent from the VR-51 board back to the AU-88 board where it is passed through the TAPE/EE selector, and is then distributed to the monitor circuit and to the output amplifier circuit. The output signal is converted from the unbalanced type to the balanced type signal in the output amplifier circuit. The signal is power-amplified at the next stage, being routed through the power on/off muting relay, and is output the LINE OUTPUT connector on the MA-26 board.

The playback equalizer frequency response is shown in Fig. 4-2-10.

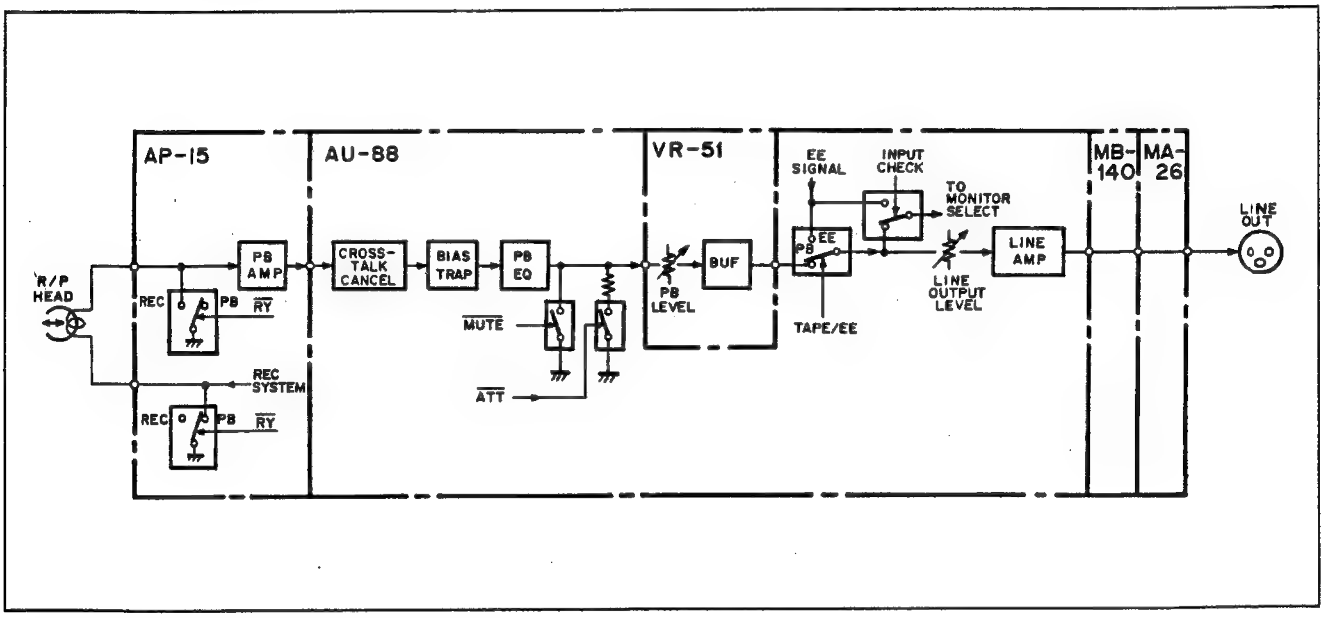


Fig. 4-2-9. Audio Signal Playback System

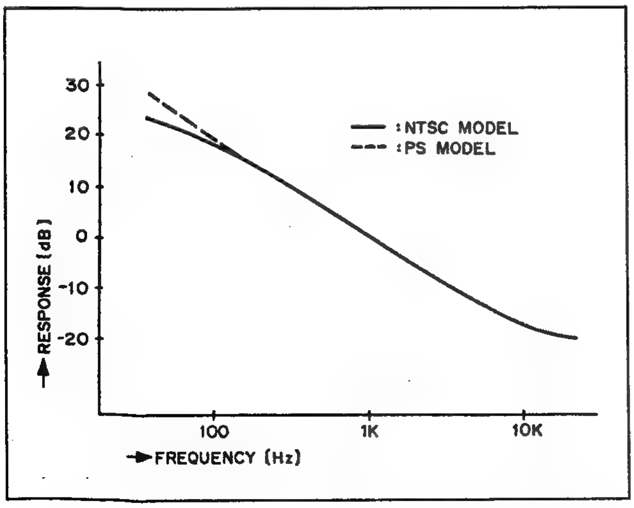


Fig. 4-2-10. Playback Equalizer Frequency Response

The audio line amplifier of BVH-3000/3100 employs the BTL (Balanced Transformer-Less) type amplifiers using no transformer, having the ±18V power supplies. The non-distorted output of this circuit is +28dBm with 1kHz/600 Ω load, having approx. 34dB (1kHz) amplification gain. This circuit can be muted perfectly using relay.
The line amplifier of the audio-1 is shown in Fig. 4-2-11. The audio-2, 3 and 4 channels have the same circuit configurations as audio-1 channel.
The IC118 line amplifier has the two built-in amplifiers where one amplifier is the inverting amplifier and the other is the non-inverting amplifier. The buffer connected after each amplifier functions as the the power amplifier. The line amplifier has the amplification·gain of approx. 33.6dB.
Diodes D109 through D112 function to protect the output transistors. Transistors Q718 through Q720 constitute the muting control circuit of the Schmitt type that controls muting at power on/off timings. The muting time is approx. 6 seconds when the power is turned on, that is determined by the time constant of R824 and C781.

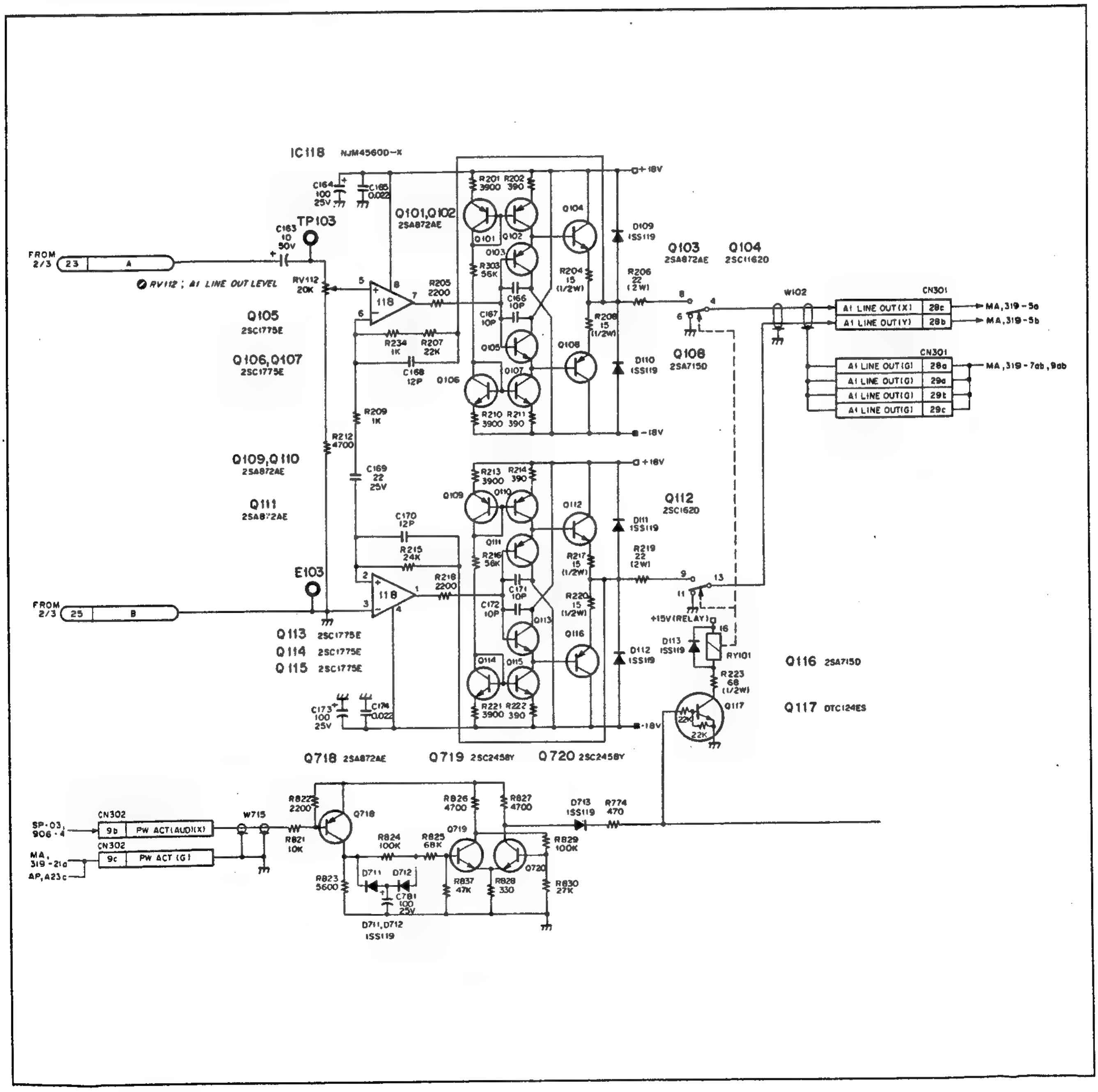


Fig. 4-2-11. Audio-1 Line Amplifier (AU-88)

4-2-4. Crosstalk Canceller (AU-88 Board)

(1) Outline

The crosstalk canceller circuit has the following three kinds in this machine.

a. PB-PB crosstalk canceller
When both of the two channels are put into playback mode simultaneously, a crosstalk will occur. This PB-PB crosstalk between the two channels can be cancelled by this crosstalk canceller. This crosstalk can be cancelled by connecting the playback signals from the two channels in opposite phase each other.

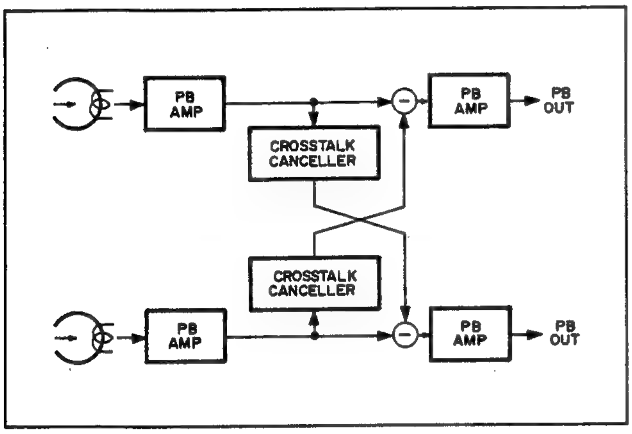


Fig. 4-2-12. PB-PB Crosstalk Canceller

b. REC-REC crosstalk canceller
When both of the two channels are put into record mode simultaneously, a crosstalk will occur between the two channels. This REC-REC crosstalk can be cancelled by this REC-REC crosstalk canceller. This crosstalk can be cancelled by connecting the recording signals of both channels in opposite phase each other.

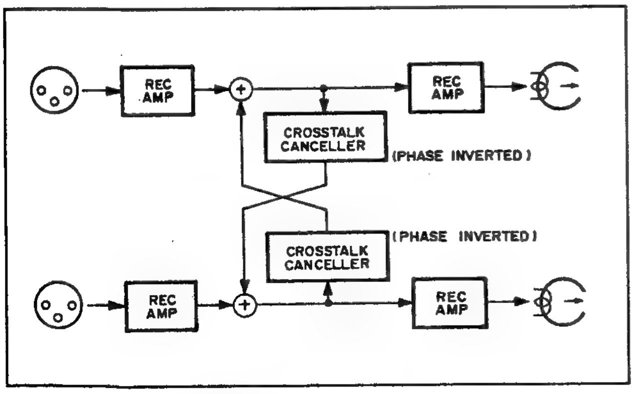


Fig. 4-2-13. REC-REC Crosstalk Canceller

c. REC-PB crosstalk canceller
When one channel is in record mode while the other channel is in playback mode, the recording channel signal can leak into the playback channel, causing crosstalk. This REC-PB crosstalk can be cancelled by REC-PB crosstalk canceller. This crosstalk can be decreased by adding the recording channel component into the playback channel in opposite phase.

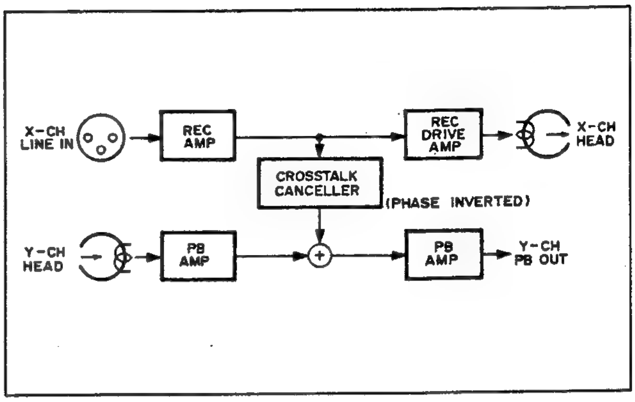


Fig. 4-2-14. REC-PB Crosstalk Canceller

These crosstalk canceller are classified into the following categories in respective channels.

a. Between the channels of audio-1 and audio-2
Between the channels of audio-3 and audio-4 (only in PS-A4 model)
- PB ↔ PB crosstalk canceller
- REC ↔ REC crosstalk canceller
- REC → PB crosstalk canceller

b. Between the channels of audio-3 and CTL (NTSC model)
- PB CTL → PB A3 crosstalk canceller
- REC A3 → PB CTL crosstalk canceller

c. Between the channels of audio-3 and CTL (PS-A3 model)
- PB CTL → PB A3 crosstalk canceller
- REC A3 → PB CTL crosstalk canceller
- REC CTL → PB A3 crosstalk canceller (in the video assemble mode)

d. Between the channels of audio-4 and CTL (PS-A4 model)
- PB CTL → PB A4 crosstalk canceller
- REC A4 → PB CTL crosstalk canceller
- REC CTL → PB A4 crosstalk canceller

(2) PB-PB crosstalk canceller (AU-88 board)

The PB-PB crosstalk canceller between the audio-1 and audio-2 channels, is shown in Fig. 4-2-15.
The cancel signal from the audio-1 to the audio-2, is generated by the circuit of R145 through R148, C126, C127 and RV105, is input to pin 6 (−terminal) of IC309 to be added to the audio-2 channel in opposite phase.
The cancel signal from the audio-2 to the audio-1 is generated by R345 through R348, C326, C327 and RV305.

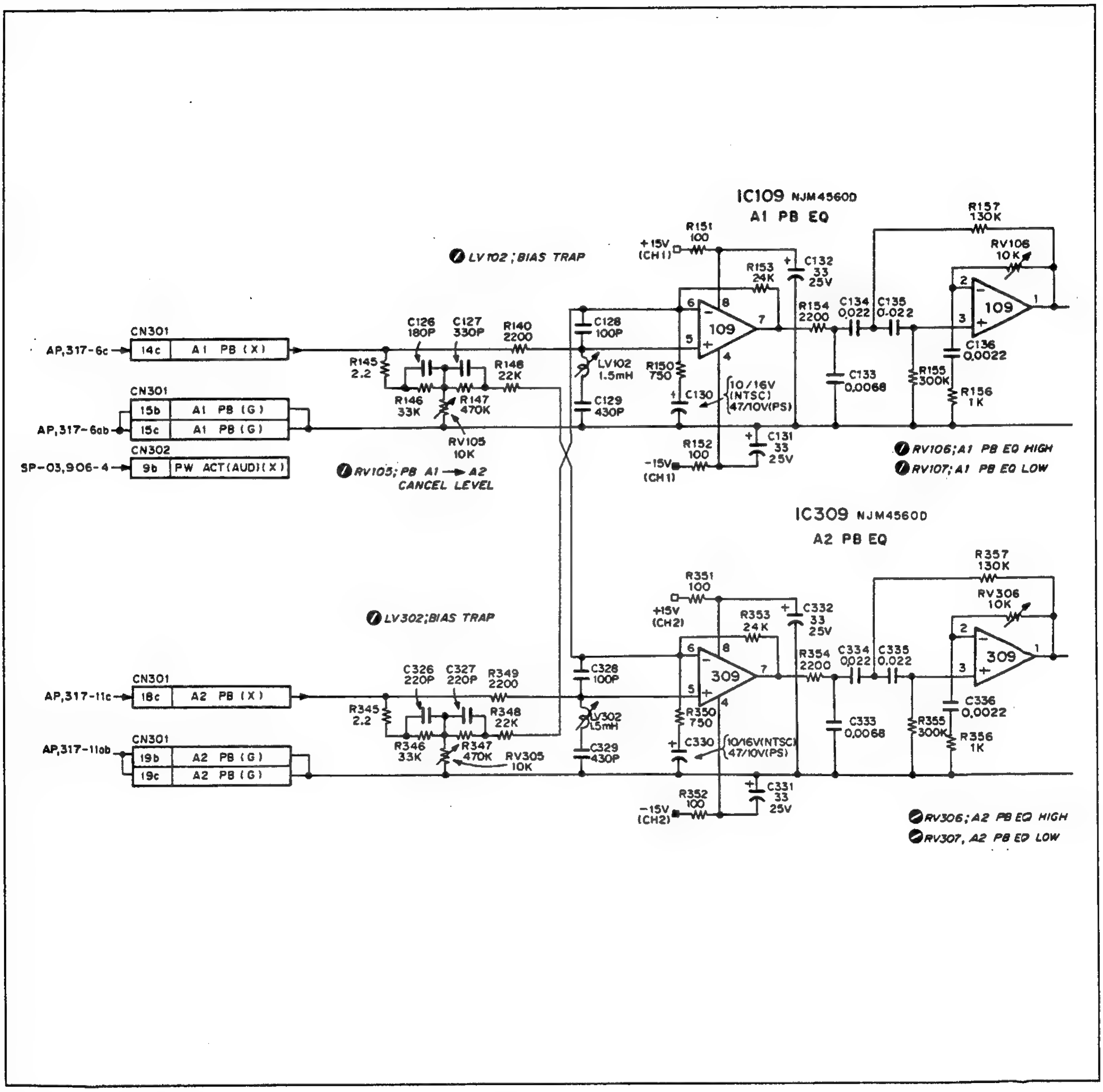


Fig. 4-2-15. PB-PB Crosstalk Canceller (AU-88 board)

(3) REC-REC crosstalk canceller (AU-88 board)

The audio-1 recording equalizer amplifier output is inverted/amplified by IC107 (pin 7), and is added to the audio-2 recording equalizer amplifier output. Thus the crosstalk from the audio-1 to the audio-2 in the record mode is cancelled.

(4) REC-PB crosstalk canceller (AU-88 board)

The pin 7 of IC107 output that is the REC-REC crosstalk canceller circuit's output is added to the audio-2 playback equalizer amplifier circuit through analog switch IC108. This is how the crosstalk is cancelled when the audio-1 is in the insert record mode while the audio-2 is in the playback mode. The IC108 analog switch is kept on in all modes other than record mode of audio-1 channel that prohibits the cancel signal from being sent to the audio-2 channel.
The crosstalk level in the high frequency area during insert mode can be adjusted by adjustment controls RV104 and LV101.

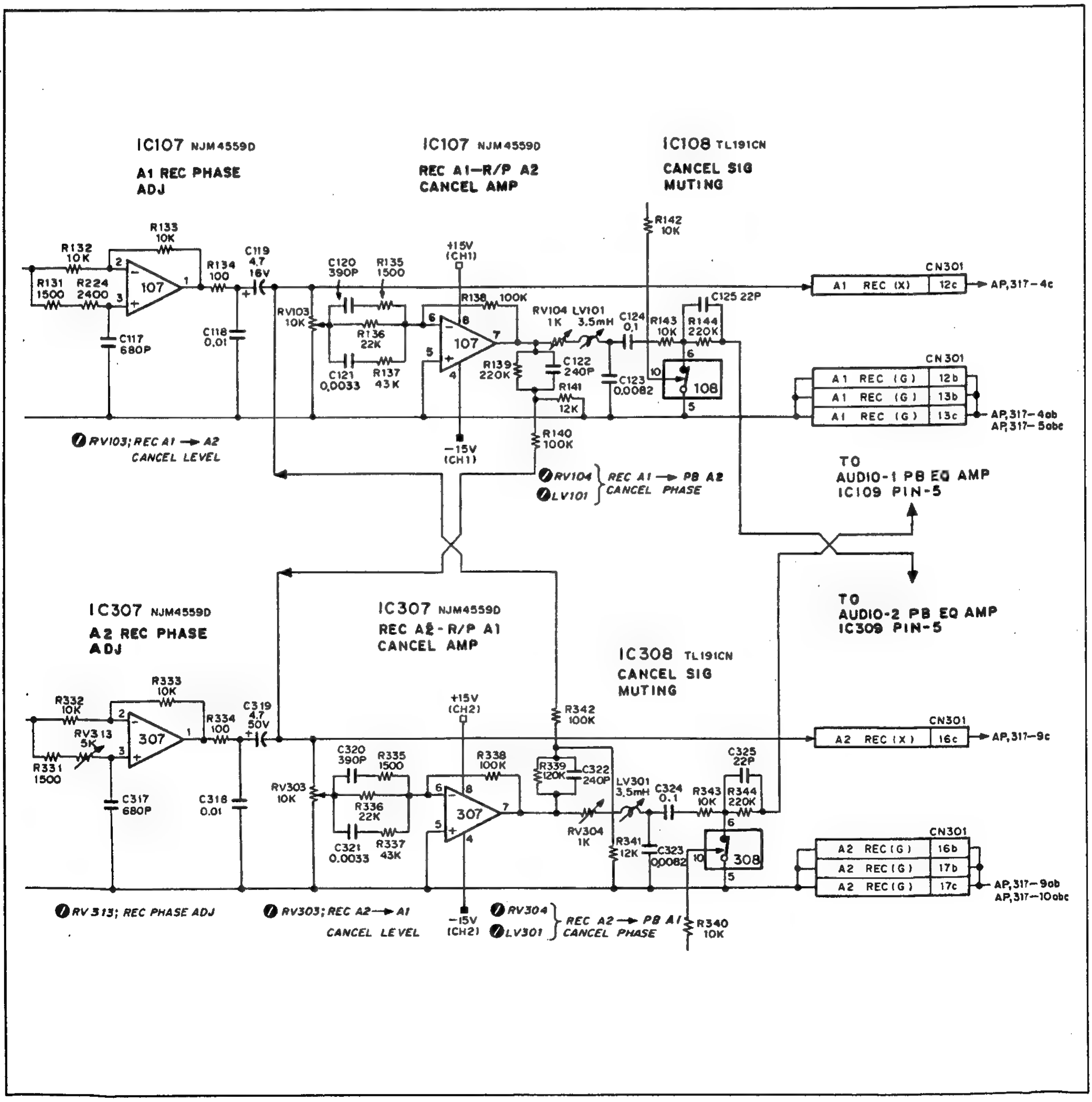


Fig. 4-2-16. REC-REC and REC-PB Crosstalk Canceller (AU-88)

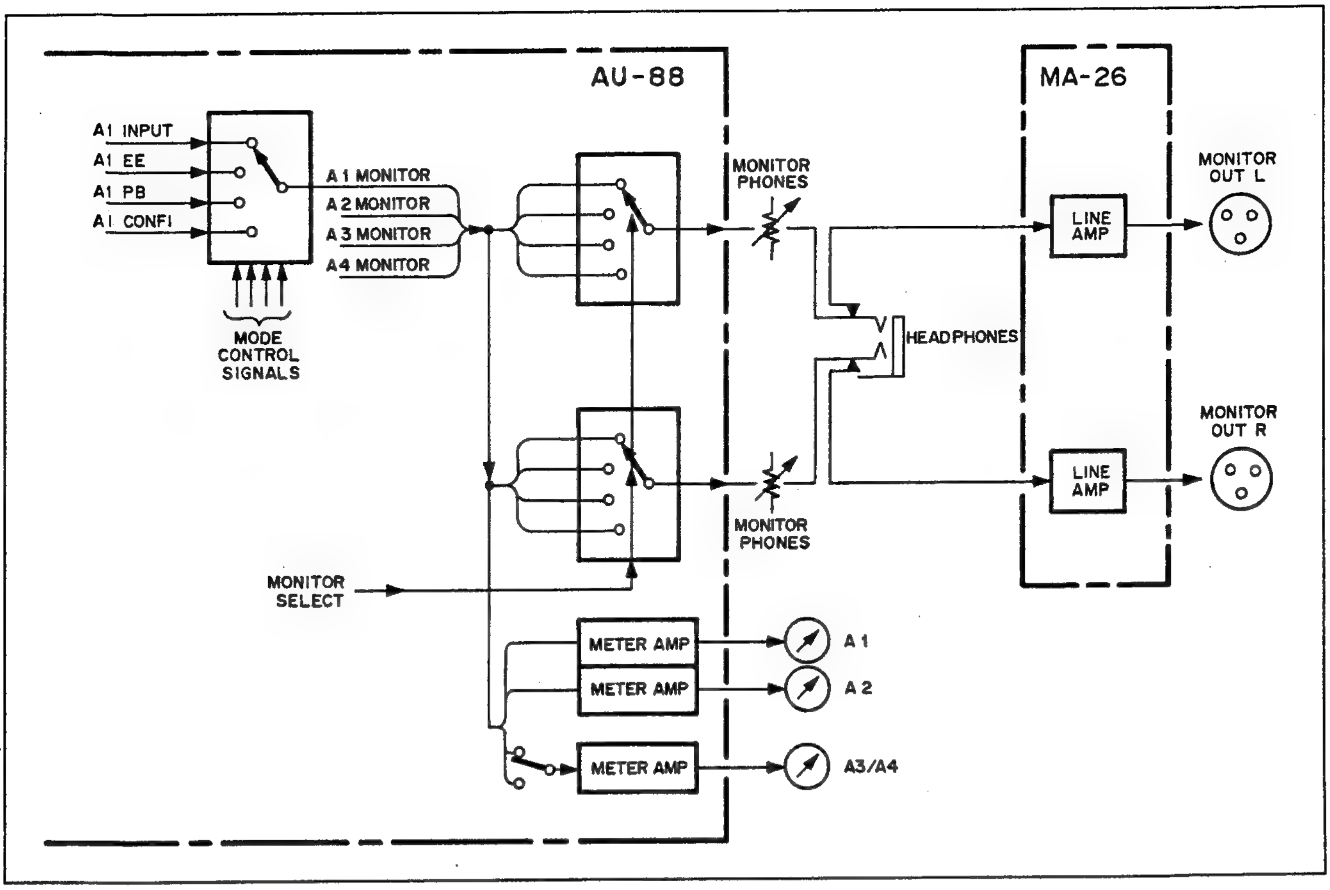


Fig. 4-2-17. Audio Monitor Selector System

4-2-5. Monitor System (AU-88, MA-26 Boards)

The monitor system circuit provides the output signal to the headphone jack on the level control panel, and to the MONITOR OUTPUT L/R connectors located on the connector panel.
The MONITOR SELECT switch on the level control panel can specify which of the A1, A2, A3 and A4 channels is to be selected as the monitor output. Which output of INPUT, EE, PB and CONFI PB signals, should be selected as the monitor signal, is automatically determined depending upon the operating mode of the VTR.
The audio meter is driven by the output signal from the monitor system circuit.

(1) Audio-1/Audio-2 mixing circuit (AU-88 board)

This circuit is to generate the mixtures signal of the audio-1 signal and the audio-2 signal without changing their signal phases. This function can be effectively used in order to confirm the phase difference between the two channel signals during the stereophonic operation very easily.
The audio-1 monitor signal and the audio-2 monitor signal are added and amplified by IC315/IC316 and are fed to the monitor select circuit.
When both signals of the audio-1 and the audio-2 are in phase, the IC316 output signal will obtain the doubled amplitude against the audio-1 or the audio-2 signal.

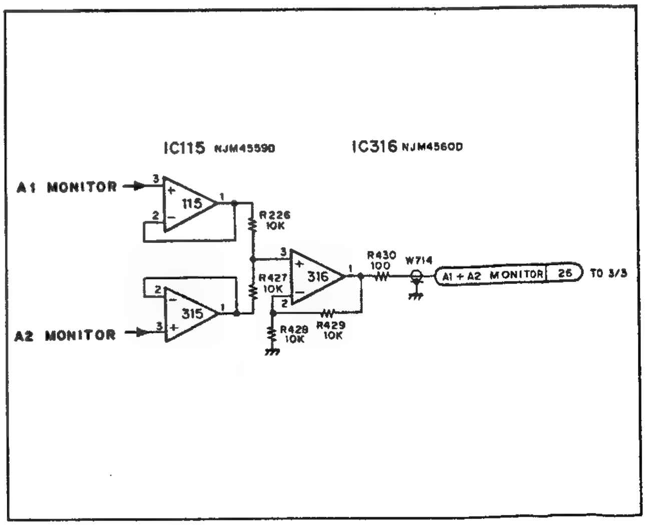


Fig. 4-2-18. Audio-1/2 Mixing Circuit (AU-88)

(2) Audio monitor (CONFI) playback circuit (AU-88 board)

In order to confirm whether the audio signal is surely recorded on tape or not in the record mode or in the edit mode, the monitor heads for the audio-1 and for the audio-2 (in the audio-4 too in the PS A4 model), are equipped.
The playback signal that is picked up by the monitor head is amplified by the playback amplifiers on the AP-15 board and then sent to the AU-88 board.
The CONFI playback signal that is sent to the AU-88 board, is supplied to the equalizer and then to the monitor select switch.

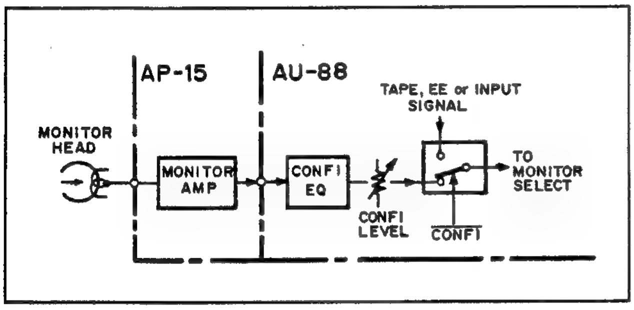


Fig. 4-2-19. Audio Monitor (CONFI) Playback System

4-2-6. Audio Record Bias System (AP-15 Board)

(1) Bias/erase oscillator (AP-15 board)

This circuit is the Colpitts oscillator consisting of the IC1 inverter and the X1 ceramic oscillator. Oscillating frequency of this circuit is 800kHz. The frequency is divided by four to make 200kHz that is sent to the IC4 resonant amplifier. The bias signal input at IC4 is wave-shaped into sine wave and sent to pins 3 and 6 of IC5. The two kinds of signal having 180° out of phase each other, are sent out from pins 1 and 7 of IC5 to the bias drive circuits.

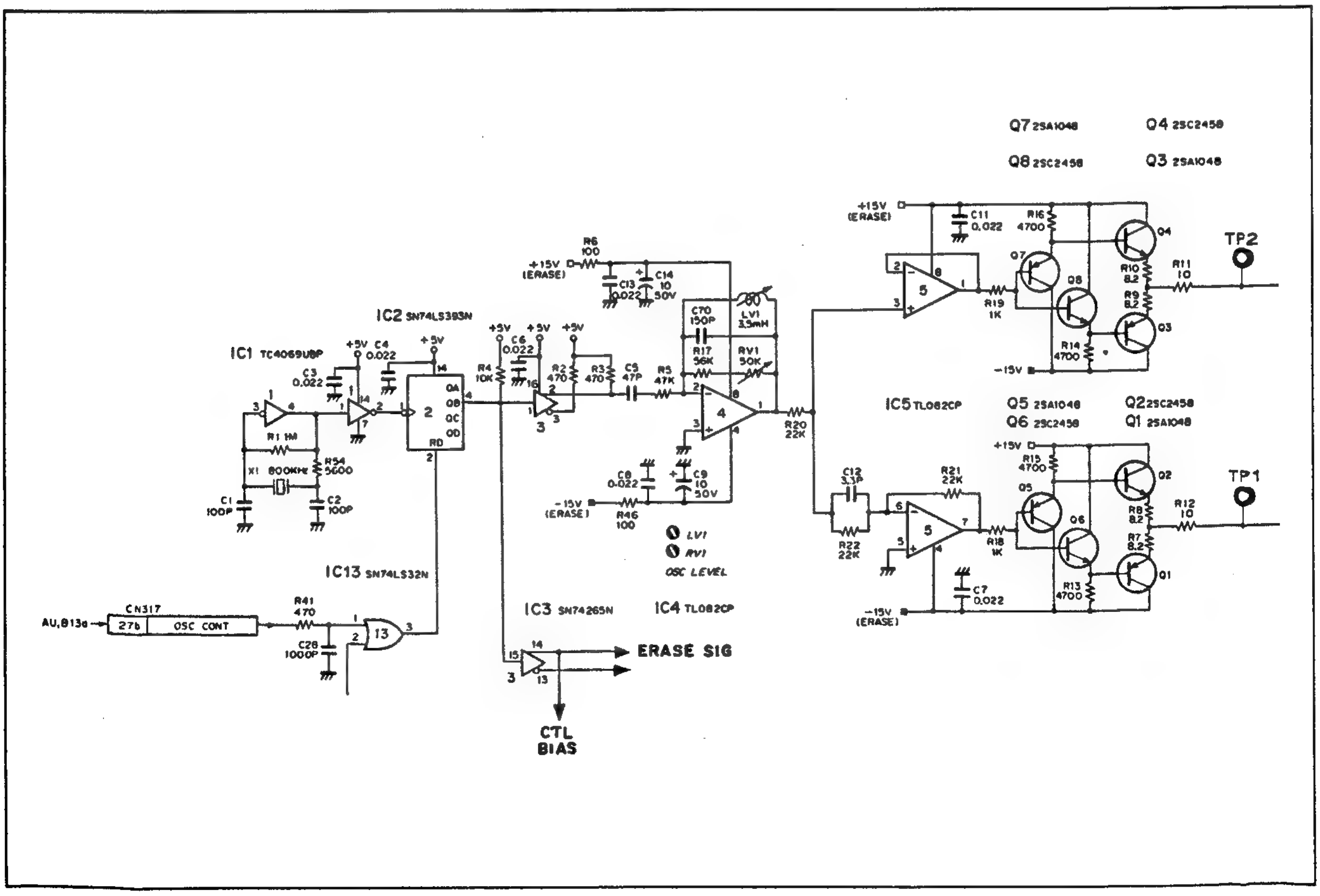


Fig. 4-2-20. Bias/Erase Oscillator (AP-15)

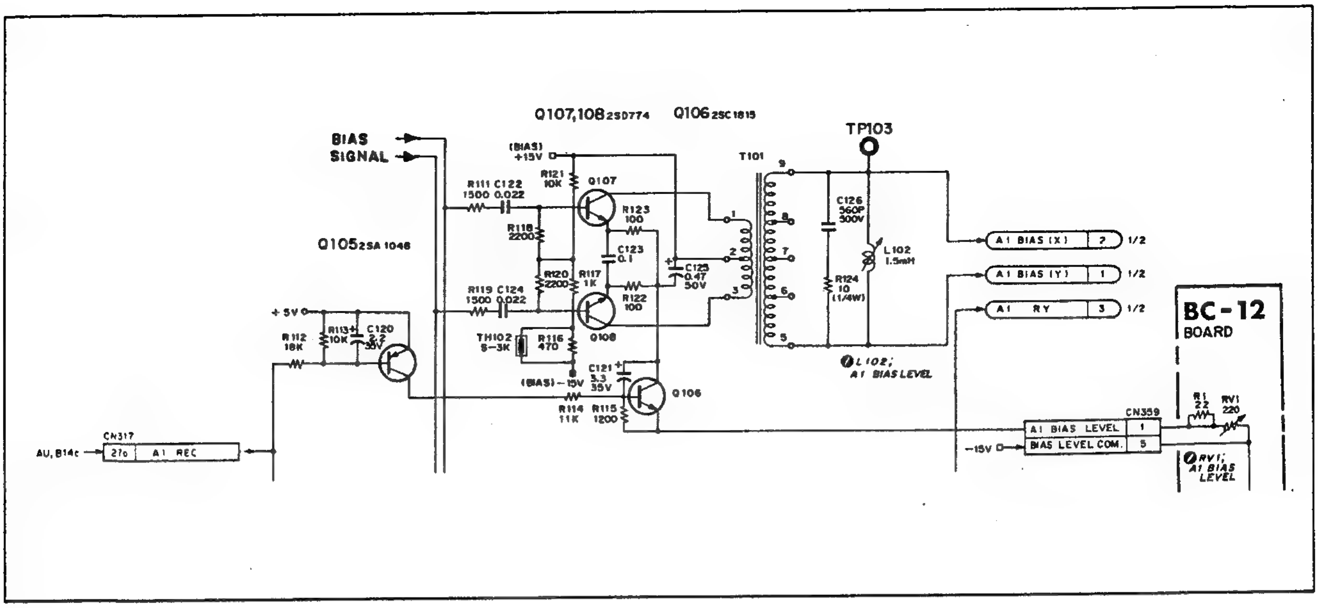


Fig. 4-2-21. Bias Driver (AP-15)

(2) Bias driver (AP-15 board)

The bias drive circuits for the audio-1, 2, 3 and 4 have the same circuit configurations so that only audio-1 channel circuit is described as follows. The audio-4 is installed only in the PS A4 model.
The audio record bias system consists of the bias timing control circuit and the bias drive circuit. The bias drive circuit is constituted by the push-pull type drive circuit using the Q107/Q108 transistors and the T101 transformer.
Q105/Q106 are the bias timing control circuit using an integrator that controls the bias signal on/off timing so that the audio signal should not be made non-continuous at the editing point. The bias level can be adjusted by the RV1 variable resistor located on the BC-12 board that controls the operating current of bias drive circuit.

4-2-7. Erase System (AP-15 Board)

The erase circuits for the audio-1, 2, 3 and 4 channels have the same circuit configuration so that only the audio-1 and 2 channels are described as follows. The audio-4 is installed in the PS A4 model only.
The erase driver circuit in the audio-1 and 2 channels have the same circuit configurations but the signals in both channels have the different phase in 180° apart in order not to leak the erase signals into the opposite channels.
This leak of erase signal into opposite channels is caused by the transformer-coupling between the coil windings inside the erase head, and is cancelled by inserting the inductors and resistors.

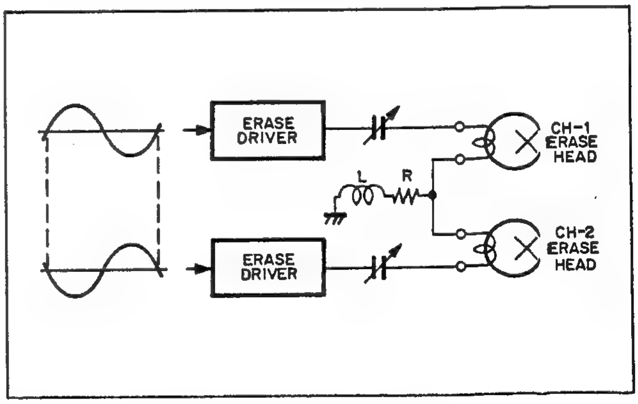


Fig. 4-2-22. Erase System (AP-15)

The 200kHz erase signals having 180° phase difference, is supplied from the bias/erase oscillator to pins 13 and 11 of IC12. IC101 and IC201 are forming the integrator that controls the erase signal's rise-up timing and fall-down timing. The resonant circuits of LV101/C112 and LV201/C212 decrease the waveform distortion.

The IC11 analog switch is the circuit that the erasure should not take place at the power on/off timings. The leakage of the erase signal between two channels are be cancelled by L206 and RV202.

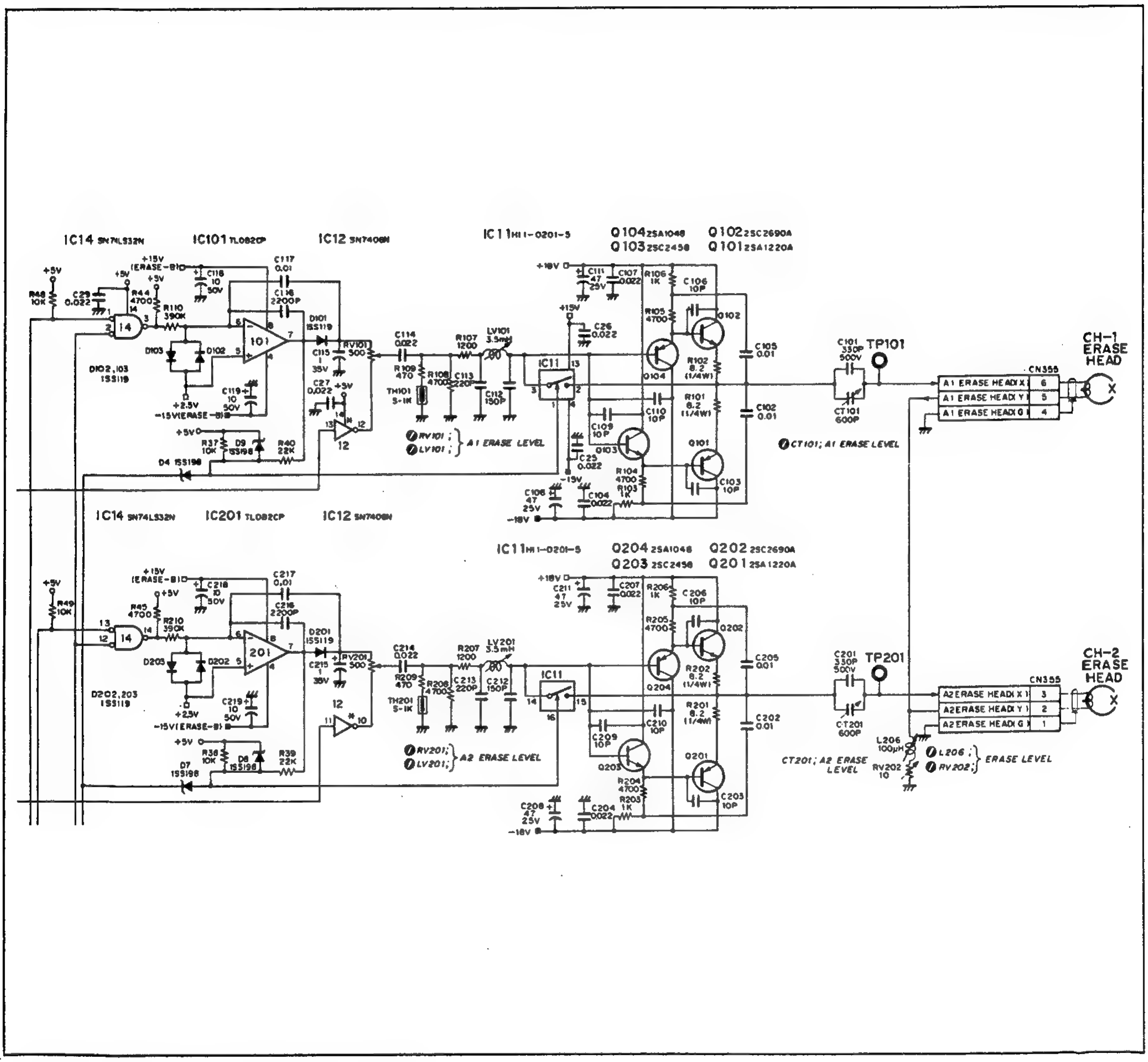


Fig. 4-2-23. Channel Erase Circuit (AP-15)

4-2-8. Audio Control Signal System (AU-88 Board)

The control signals for the audio signal system, are sent from the SV-90 board in the form of 8-bit serial data.
The serial data are converted into parallel data and then used for each control. The serial-to-parallel conversion is done by I/O expander IC4 and IC5 (CXD1095Q) on the AU-88 board.

The control signal for the bias erase system is supplied from IC4 to the AP-15 board in the form of parallel signal. The control signal for the LED display of the monitor select system is sent out from IC5.
The REC inhibit command or the monitor select command that are set-up depending upon the switch settings on the level control panel, are converted from parallel to serial by the same I/O expander, and are sent to the main CPU on the SV-90 board.

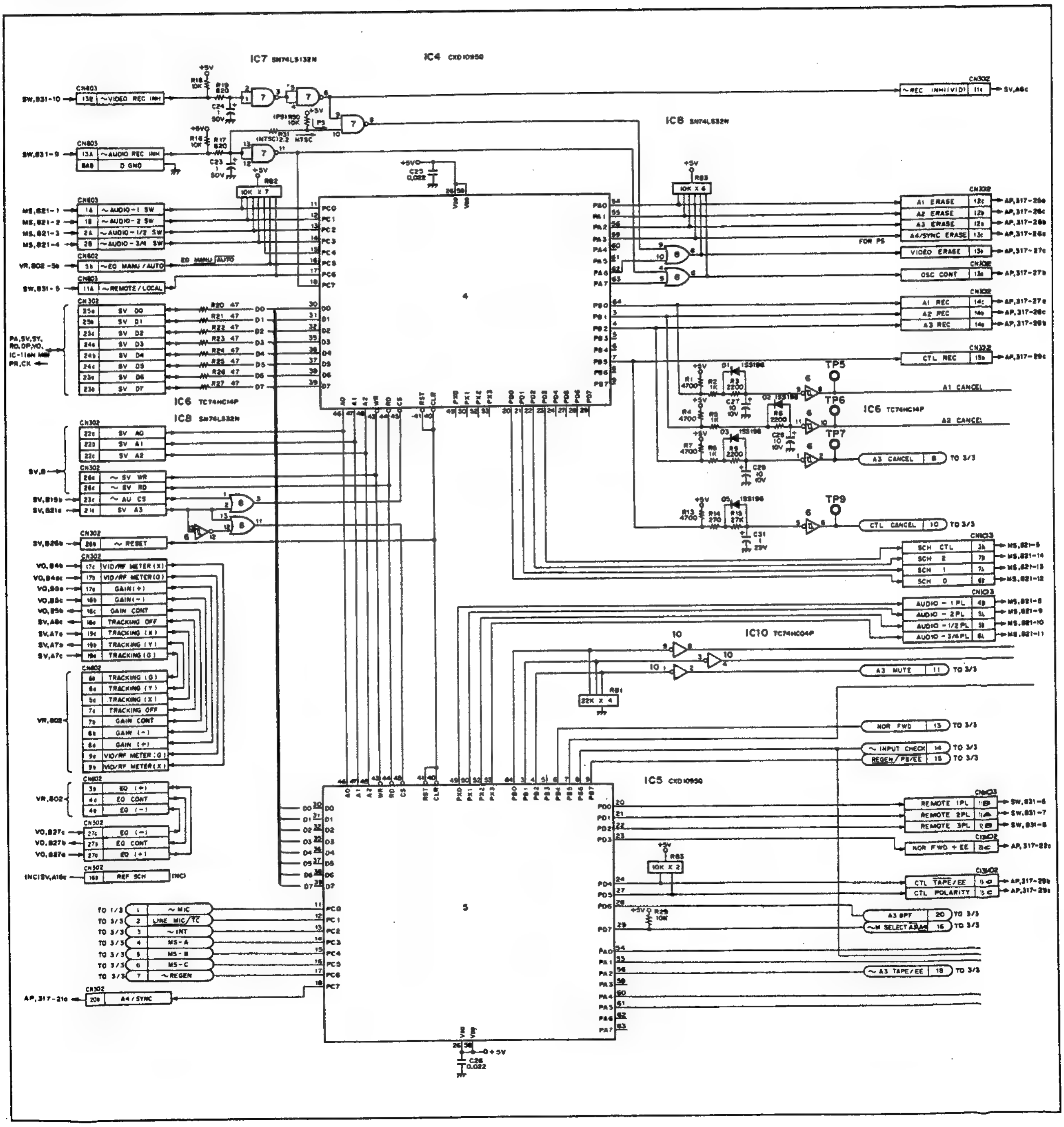


Fig. 4-2-24. Audio Control Signal System (AU-88)

4-2-9. Time Code System (AU-88 Board)

The time code signal is recorded on the audio-3 track. The necessary circuit for time code signal processing is located in the audio-3 circuit block.

(1) Time code record system (AU-88 board)

The two kinds of time code signals can be recorded. One signal is the TC GEN signal that is generated by the SY-103 board's time code generator while the other is the time code signal being supplied from the A3 LINE IN connector. Either one of these two time code input signals, is selected by the IC520. The time code signal selected by IC520, is wave-shaped by the comparator IC521 and then sent to IC519 through IC522 and IC525 where the signal is again wave-shaped. The wave-shaped time code signal is sent to the record equalizer through the IC506 analog switch. The rest of the signal processing is the same as the normal audio-3 signal processing.

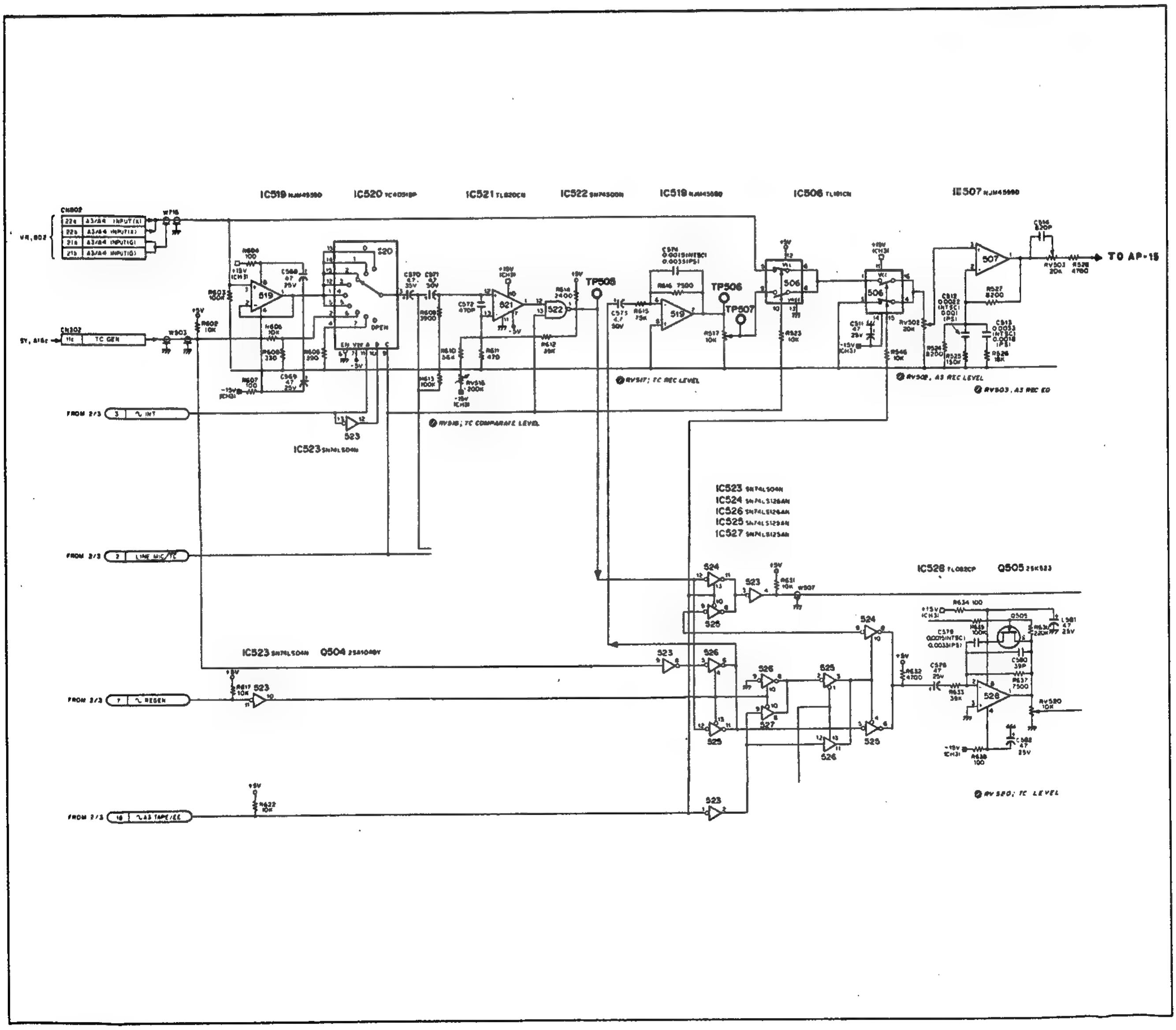


Fig. 4-2-25. Time Code Record System (AU-88)

(2) Time code playback system (AU-88 board)

The playback time code signal is input to the AU-88 board as an ordinary audio signal, amplified by IC510 and IC513, and is then sent to the playback level control circuit as the audio signal, and also sent to the wave-shape circuit of IC521 and IC522 as the time code signal. The wave-shaped time code signal is sent to the time code reader circuit of the SY-103 board through IC525 and IC523. The time code signal is shaped into the specified wave-shape by IC524 and IC528, and is then sent to the audio-3 line amplifier.

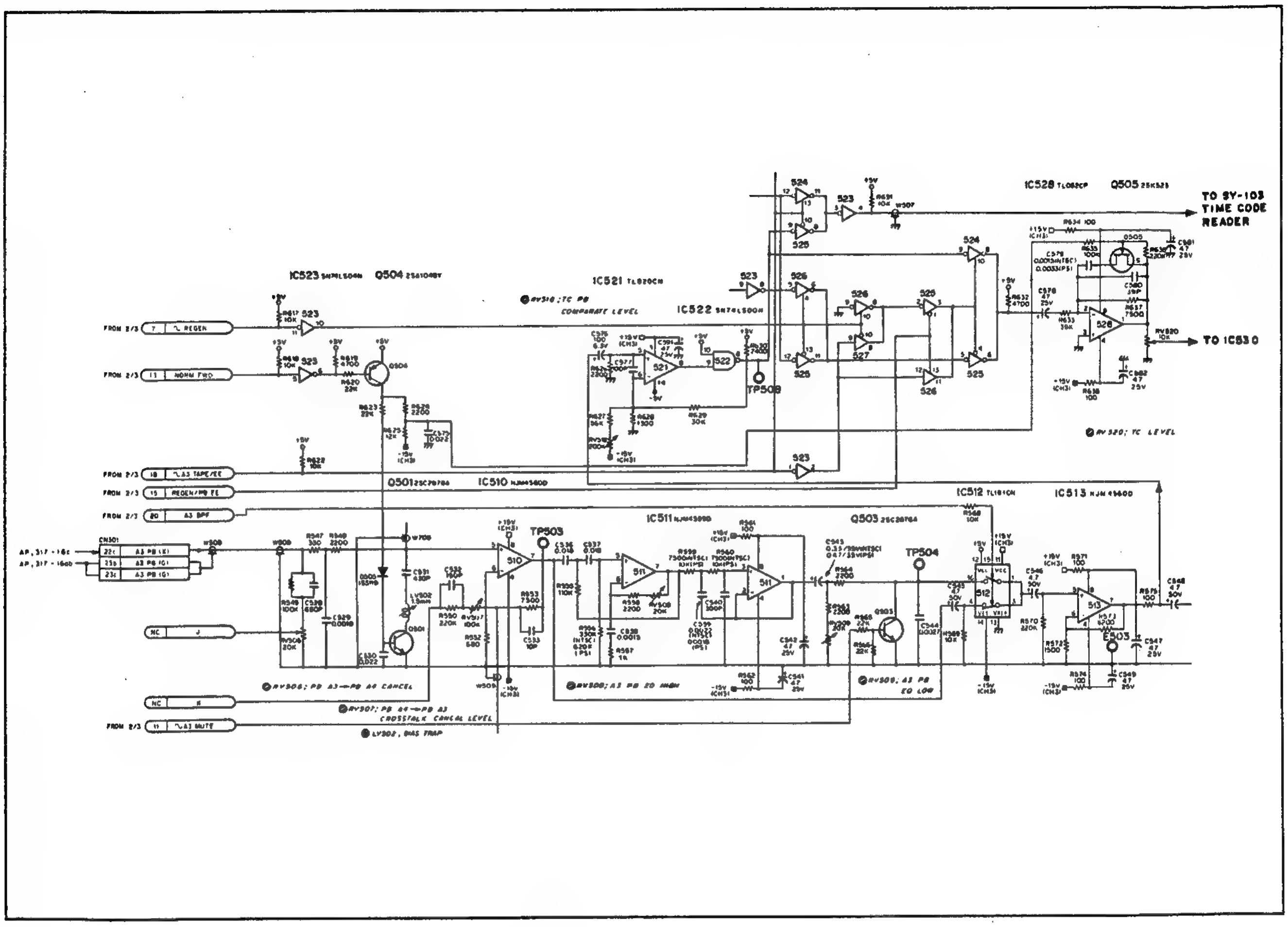


Fig. 4-2-26. Time Code Playback System (AU-88)

4-3. VIDEO SIGNAL SYSTEM

Note 1 : Any references to the sync channel in the description below apply only to the model BVH-3000 and not to the model BVH-3100.

Note 2 : Reference should be made to Section 4-4 for details on the TBC section.

4-3-1. Outline of Video Signal System

The video signal system circuitry is composed of five circuit boards whose names and functions are listed below

1. VO-16 board : Modulator, RF equalizer, demodulator
2. RP-32 board : REC/PB amplifier (for R/P head)
3. VS-30 board : I/O buffer/monitor output amplifiers
4. VR-51 board : REC level/PB equalizer control
5. DR-13 board : PB amplifier/strain gauge amplifier (for PLAY head)

The video signal input to the VIDEO INPUT terminal is supplied to the VO-16 board via the buffer amplifier on the VS-30 board. On the VO-16 board, the level of the video signal is first adjusted by the DC voltage from the REC level control on the front panel and then it is frequency-modulated. The frequency-modulated RF signal is amplified by the RP-32 board, supplied to the R/P head and then recorded onto the tape.

During playback, the signal recorded on the tape is played back by the R/P head or PLAY head. The RF signal from the R/P head is supplied to the VO-16 board via the RP-32 board, and the RF signal from the PLAY head is supplied to the VO-16 board via the DR-13 board inside the upper drum. The VO-16 board is responsible for the differential gain, differential phase and frequency response compensation and other such equalizer processing and also for the demodulation of the RF signal.
The demodulated video signal passes through the noise suppressor which serves to suppress the switching noise which is generated with video/sync channel switching, it then goes through the TBC section and is output from the VIDEO OUTPUT terminal via the buffer on the VS-30 board.

4-3-2. Video Signal Recording System (VO-16, RP-32 Boards)

The video signal which is input to the VIDEO INPUT terminal is supplied to the VO-16 board through the buffer on the VS-30 board, and its level is adjusted by the DC voltage from the VIDEO level control on the front panel. The adjusted signal is supplied via the pedestal clamp, burst doubler, VITC insertion and pre-emphasis circuits to the modulator where it is frequency-modulated.
The modulator output is supplied to the demodulator as the EE signal, and it is also supplied to the R/P head through the recording amplifier on the RP-32 board and recorded onto the tape.

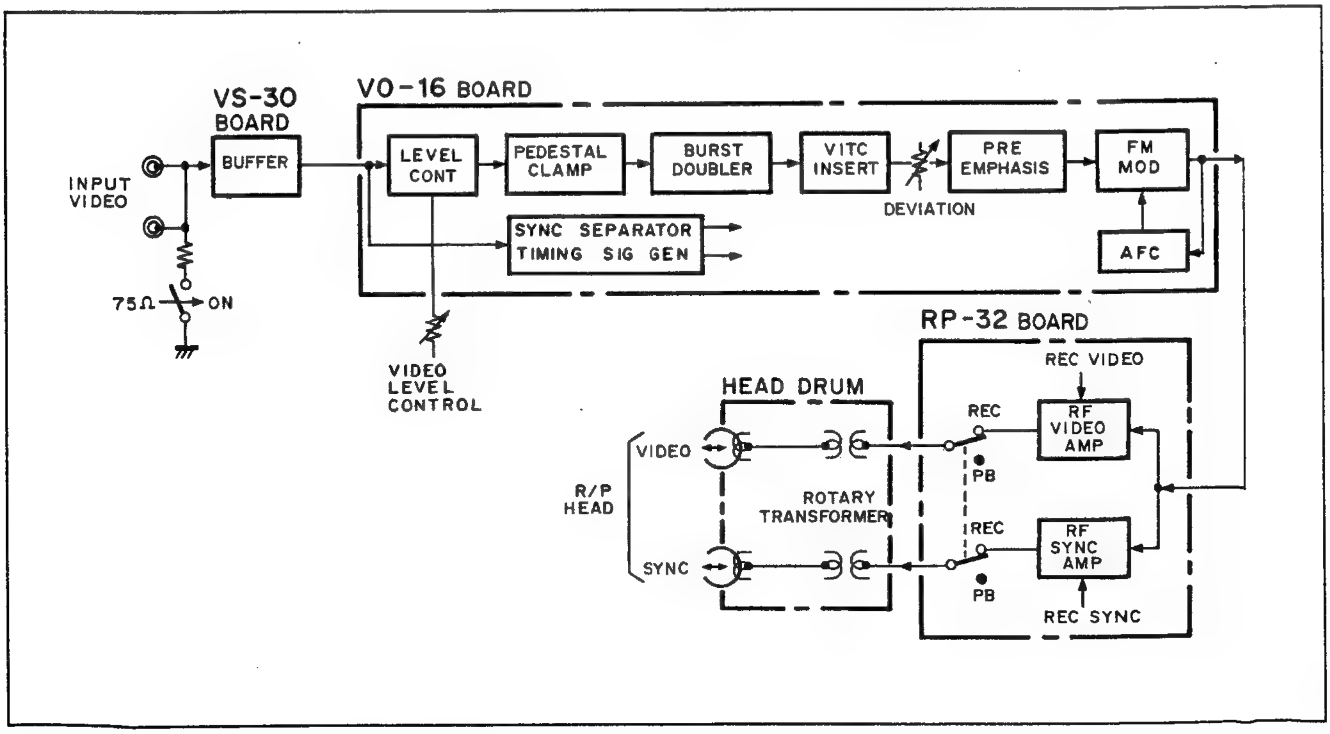


Fig. 4-3-1. Video Signal Recording System

(1) Input level controller (VO-16 board)

The input video signal which has been sent from the VS-30 board to the VO-16 board passes through buffer amplifier IC1 and its level is controlled by IC2. The control signal controls the inverted input (−input) impedance of video amplifier IC2 by the DC voltage (TP4) which has been sent from the VR-51 board.
The control range is from −6dB to 3.5dB. In other words, the signal can be controlled to the same level as that of the normal input video signal in the event of no termination or double termination. The video signal whose level has been controlled is sent to the pedestal clamper circuit.

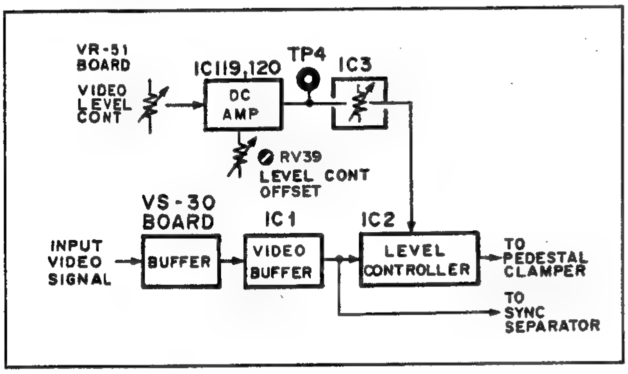


Fig. 4-3-2. Input Level Controller (VO-16)

(2) Sync separator/timing signal generator (VO-16 board)

One of the input buffer outputs passes through the low-pass filter composed of R98 and C146, it is amplified 2-fold by IC42 and it enters sync separator IC43.
The sync separation output is produced from pin 4 of IC43 and the TTL level is provided by R104 and R105. The signal is then supplied to the IC44 and 45 monostable multivibrators to produce the timing signals with the required phase and pulse width.
The TP2 output pulse is sent to the pedestal clamper, burst doubler and AFC circuit while the TP3 output pulse is sent to the AFC circuit.

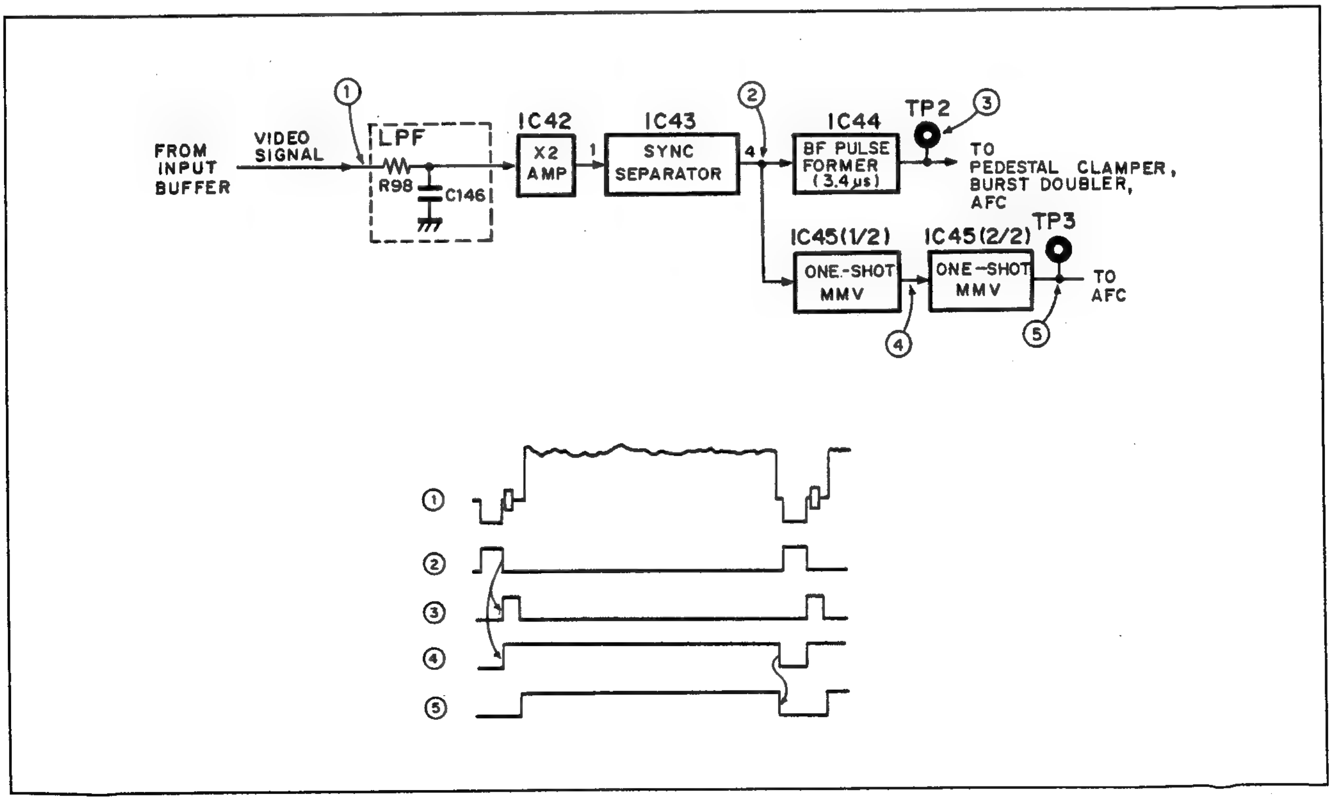


Fig. 4-3-3. Sync Separator/Timing Signal Generator (VO-16)

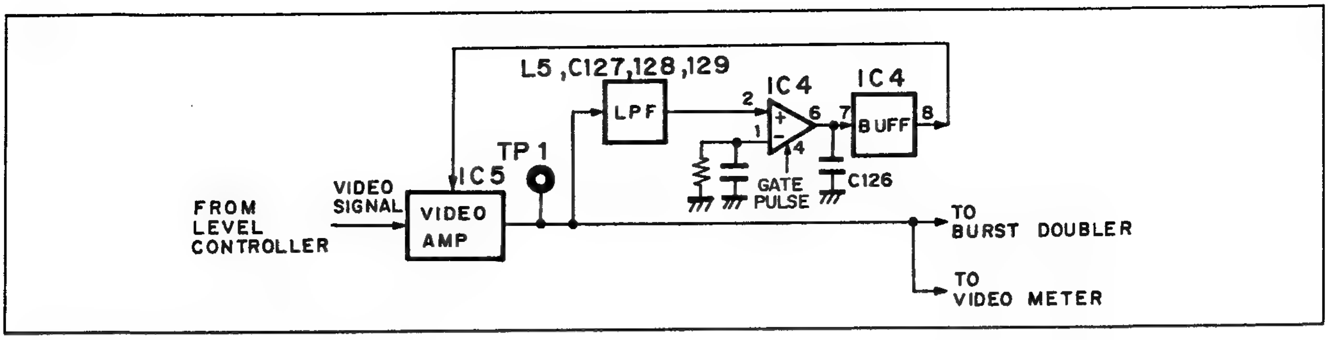


Fig. 4-3-4. Pedestal Clamper (VO-16)

(3) Pedestal clamper (VO-16 board)

The input video signal whose level has been controlled by IC2 is supplied to the pedestal clamper which is configured by IC4 and IC5. This circuit fixes the back porch portion of the video signal at DC 0V in order to stabilize the operation of the later stage circuitry when video signals with a fluctuating APL are supplied.
The video amplifier IC5 output (TP1) passes through the low-pass filter composed of C127, 128, 129 and L5, and it is supplied to pin 2 of IC4.
IC4, which is configured as shown in the figure, is a sample and hold circuit which charges the difference in level between pins 1 and 2 into C126 when the gate pulse is supplied to pin 4 and which outputs the signal as a DC voltage from pin 8 through the buffer amplifier. The video signal (TP1) whose pedestal level has been clamped is now supplied to the burst doubler and video level meter circuit.

(4) Burst doubler (VO-16 board)

The recording level of the burst signal is amplified 2-fold by the burst doubler in order to improve the signal-to-noise ratio of the burst signal during playback. The pedestal-clamped input video signal is amplified 2-fold by video amplifier IC6 and it is split into two. One signal is supplied to pin 6 of analog switch IC8 after its level is divided down to one-half by resistors; the other signal is supplied directly to pin 8 of analog switcher IC8. A video signal whose burst level is amplified 2-fold can be produced by switching the switcher using the TP2 burst gate pulse.

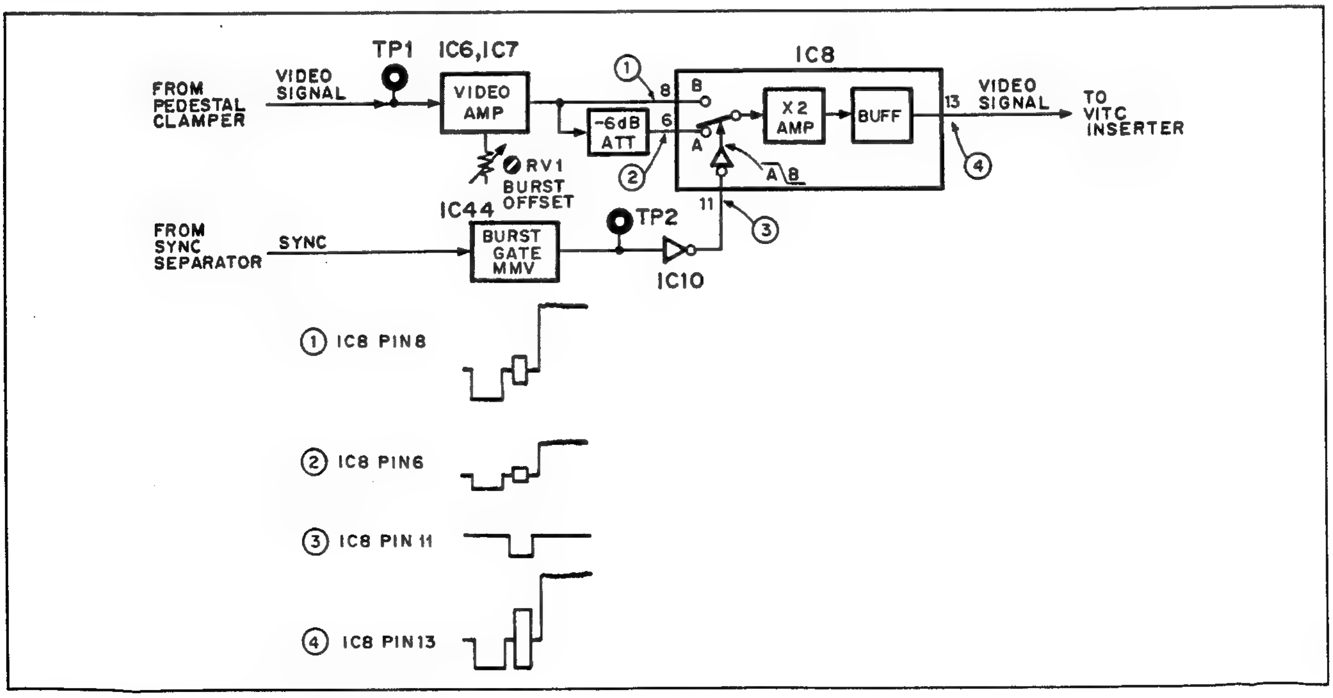


Fig. 4-3-5. Burst Doubler (VO-16)

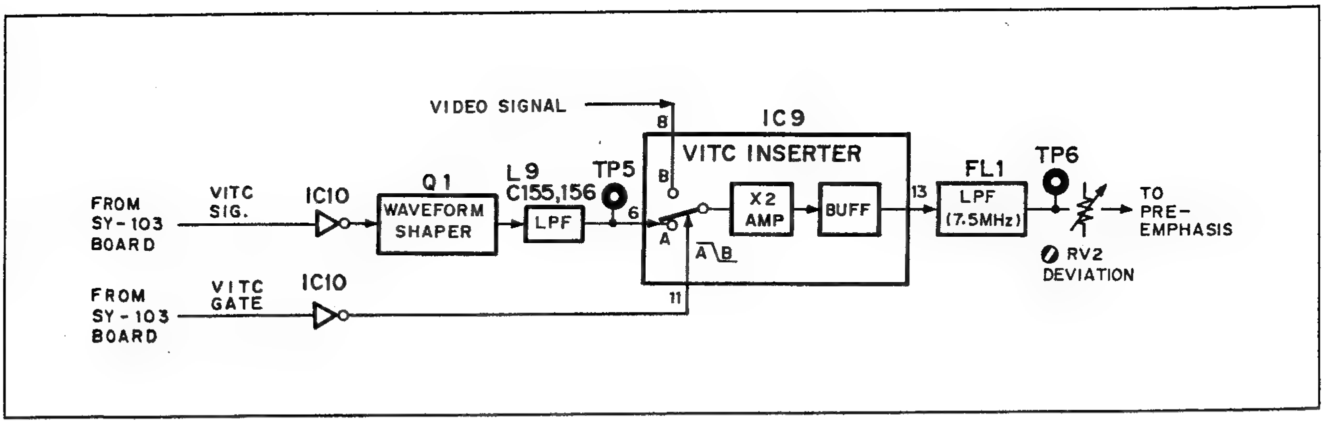


Fig. 4-3-6. VITC Inserter (VO-16)

(5) VITC inserter (VO-16 board)

This circuit serves to insert the VITC signal, which is supplied from the SY-103 circuit, into the input video signal.
The VITC signal (TP5), which has been waveform-shaped by Q1, is inserted into the video signal line by the VITC gate signal. The VITC gate signal is also sent from the SY-103 circuit. The VITC inserter circuit also functions as a circuit for inserting the time code characters into the video signal to be recorded and it does this for off-line editing purposes. Initial setup menu [160. CHARACTER RECORD] is usedto select the character recording mode. The next-stage low-pass filter has characteristics of 7.5MHz/−3dB and it has been inserted in order to improve the signal-to-noise ratio and reduce the amount of switching noise during operations involving the burst doubler and VITC inserter. The low-pass filter output is sent to the pre-emphasis circuit through the variable resistor (RV2) used to adjust the deviation.

(6) Pre-emphasis and FM modulator (VO-16 board)

R37-40, C131 and C132 represent the emphasis constants. Based on these constants, the emphasis is 8dB (or 10.6dB for the PAL/SECAM system) and the center frequency is 420kHz (or 480kHz for the PAL/SECAM system). The output (TP7) of the pre-emphasis circuit provides the multivibrator with current drive and generates frequency modulated waves.
When there is any deterioration in the symmetry of the output waveforms of the multivibrator, this is accompanied by an even-numbered order of higher harmonics, and beat interference known as moire is generated. The balance of the modulator is adjusted by RV3 in order to improve the symmetry of the output waveforms. A balanced output type of oscillator is used in order to improve the symmetry of the output waveforms and to cancel out leakage into the RF signals from the video signal.

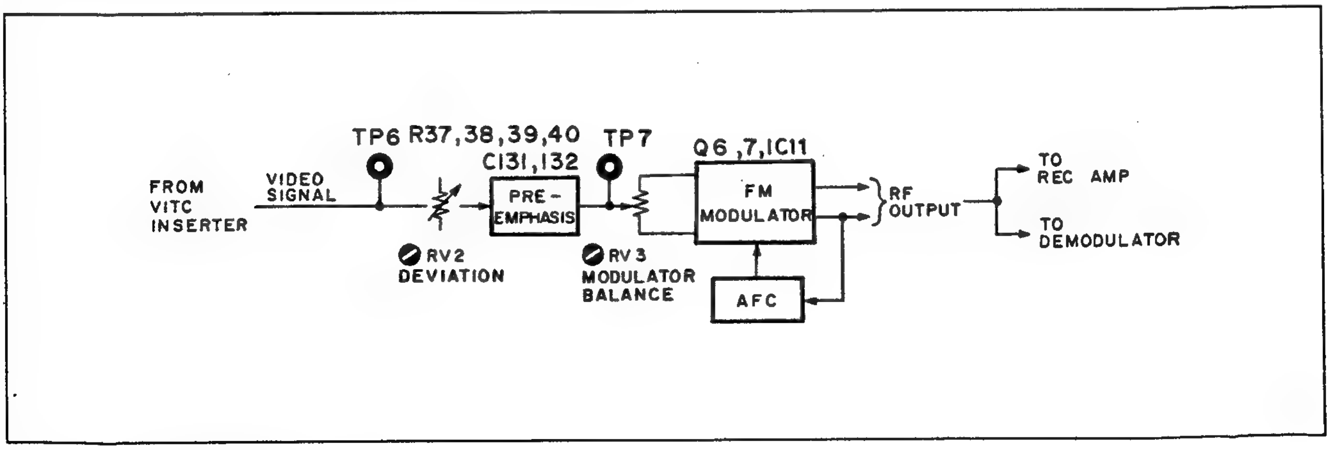


Fig. 4-3-7. FM Modulator (VO-16)

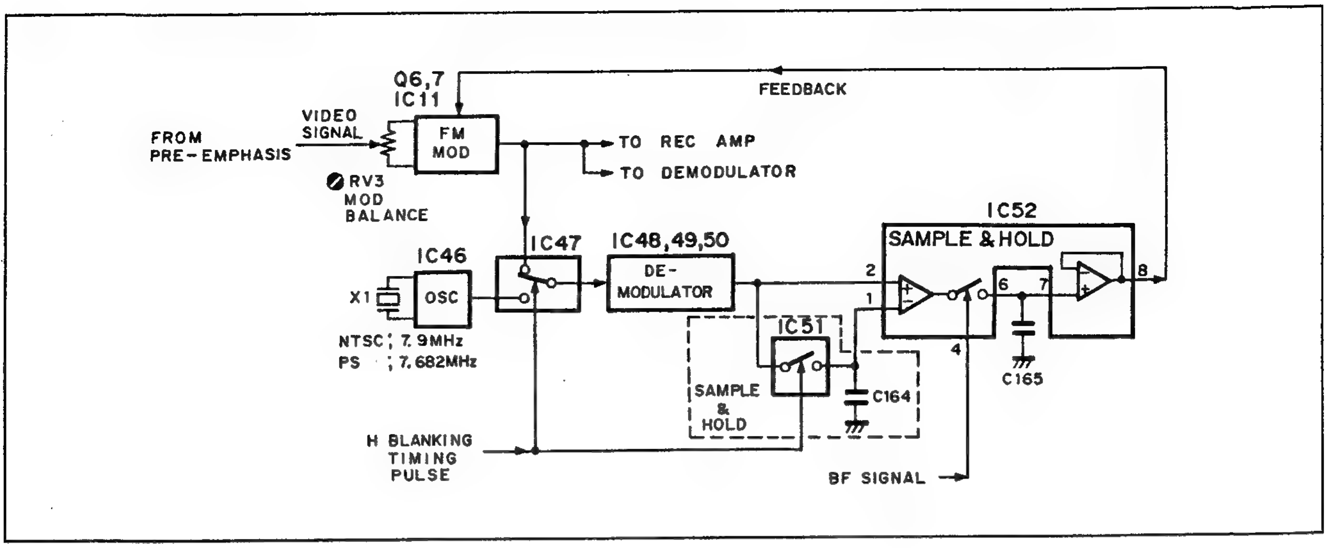


Fig. 4-3-8. AFC/FM Modulator (VO-16)

In order to stabilize the oscillation frequency of the FM modulator, the frequency of the pedestal portion of the modulator output is compared with the 7.9MHz (or 7.682MHz for the PAL/SECAM system) output frequency of the crystal oscillator and the resulting output is fed back to the modulator. The modulator output of the horizontal blanking period and the output of the crystal oscillator are multiplexed in IC47 by the TP3 timing signal. This is then demodulated into the video signal by IC48, 49 and 50 and by the low-pass filter.
The level of the horizontal blanking portion in the demodulated video signal is sampled and held by IC51 and C164, and this level is compared with the level produced by demodulating the crystal oscillator output. The comparison output is then sampled and held again by IC52 and C165 and fed back to the modulator in the form of a DC voltage. As a result, the FM modulator is controlled so that the oscillation frequency of the pedestal portion tallies with the frequency of the crystal oscillator.
The FM modulator output is sent to the recording amplifier as the recording signal and to the demodulator as the EE signal.

(7) Video recording amplifier (VO-16, RP-32 boards)

The equalizer circuit on the VO-16 board functions to compensate the frequency response, differential gain and differential phase of the FM modulator output. The same circuit also functions to adjust the recording current level. The equalizer output is sent to the recording amplifier on the RP-32 board.
On the RP-32 board, the signal passes through buffer amplifier Q1 and is distributed to the video channel and sync channel recording amplifiers. The respective recording amplifiers function as differential amplifiers in order to reduce interference of noise, and the only adjustment made here relates to the balance of the differential input circuit. The recording current is turned on and off by the initial stage unbalanced-balanced converter section.

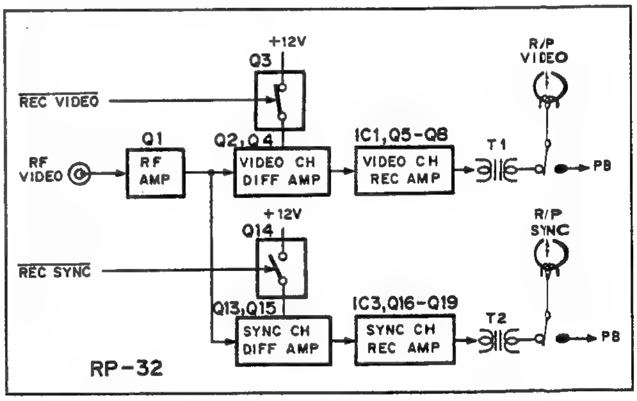


Fig. 4-3-9. Video Recording Amplifier (RP-32)

(8) Rotary erase circuit (RP-32 board)

Erase oscillators are provided both for the video channel and sync channel. The respective oscillator outputs drive the video and sync erase heads through the rotary transformers. The only adjustments made relate to the tuning between the heads and the levels.

4-3-3. Video Signal Playback System (RP-32, DR-13, VO-16 Boards)

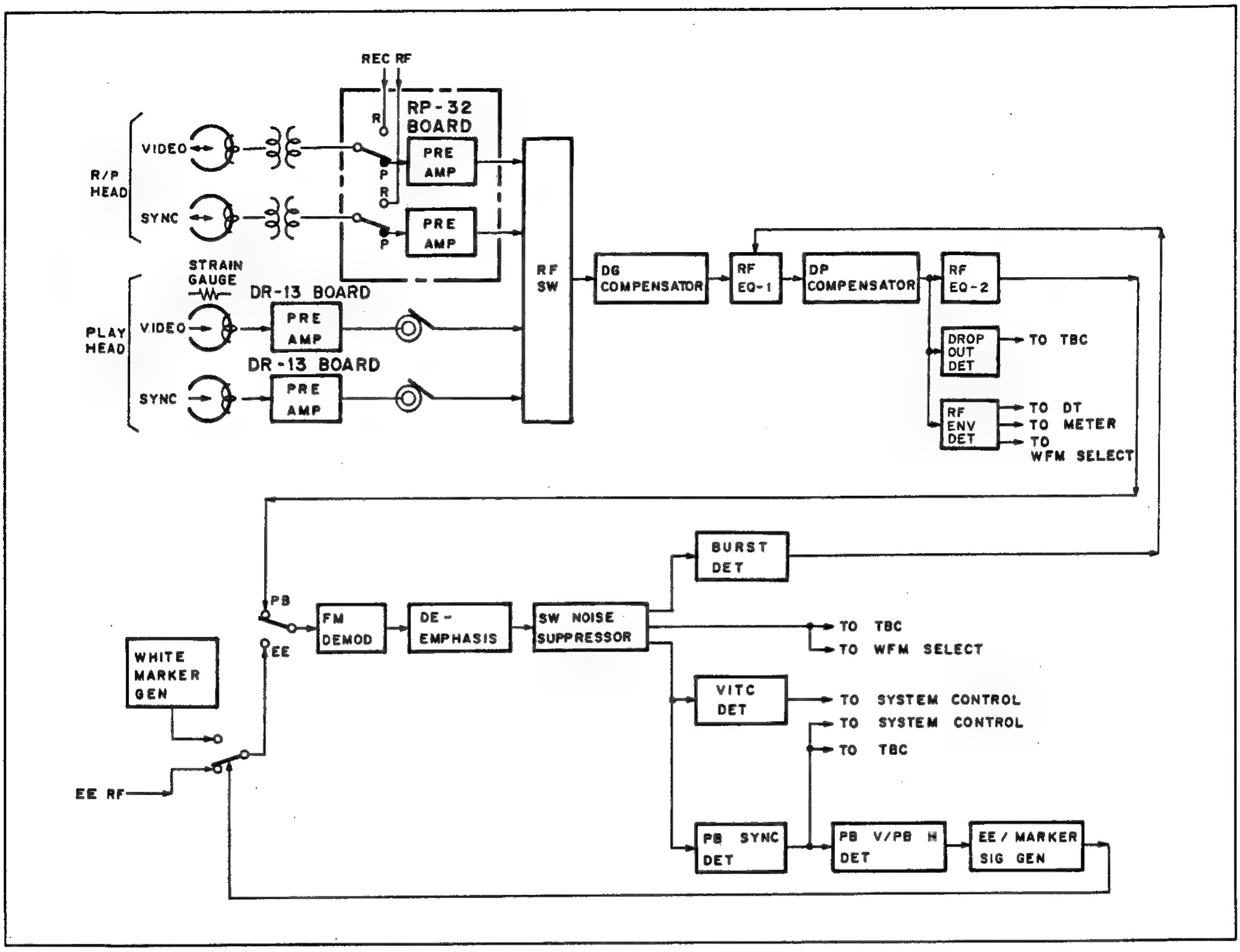


Fig. 4-3-10. Video Signal Playback System (VO-16)

(1) Preamplifiers (RP-32, DR-13 boards)

The preamplifiers for the video head and sync head are composed of a BX1156B hybrid IC for each channel, and their gain is approximately 46dB.
The R/P head preamplifiers are located on the RP-32 board ; the PLAY head (DT head) pre-amplifiers are located on the DR-13 board inside the upper drum.

(2) RF switcher (VO-16 board)

The R/P video and R/P sync RF signals from the RP-32 board as well as the PLAY video and PLAY sync RF signals from the DR-13 board are selected by controller IC15 and 16 and by switcher IC17, 18, 19 and 29.
When the EE mode has been selected, all the switchers are off. The level of the switcher output (TP16) is 100mVp-p.

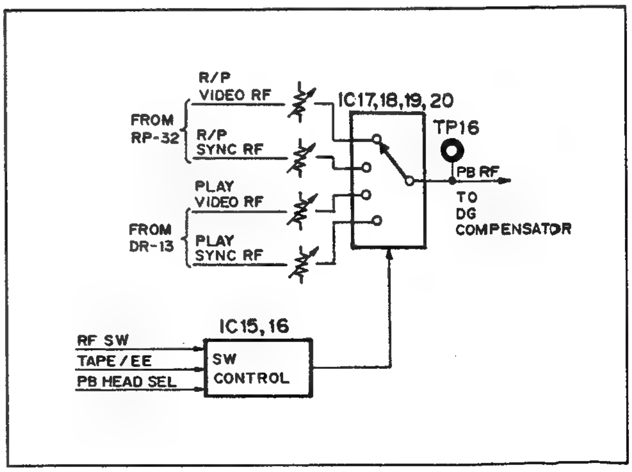


Fig. 4-3-11. RF Switcher (VO-16)

(3) DG compensator (VO-16 board)

The differential gain is compensated by varying the Q of the resonator circuit which is composed of R291, L19, C444 and Q9.
During playback by the PLAY heads, this gain is compensated by the value produced by superimposing the compensation value for the PLAY head onto the compensation value for the R/P head.

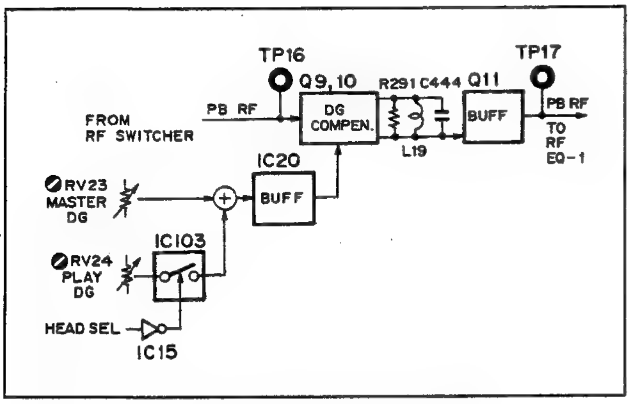


Fig. 4-3-12. DG Compensator (VO-16)

(4) RF equalizer 1 (VO-16 board)

Using a cosine equalizer configuration, the amplitude characteristics are changed without changing the phase characteristics, and the amplitude characteristics of the lower side band of the RF signal are compensated.
The input end of delay line DL1 is impedance-matched but the output end is unmatched with a high impedance. This means that the RF signal is configured as a reflected wave at the output end, that it returns to the input end and that it is superimposed onto the input signal.
If it is assumed that the delay time of the delay line is "t_d" and that input signal "e_a" at point A is "$\sin \omega t$," then signal "e_b" at point B will be equal to "$\sin \omega (t-t_d)$."
Since signal "e_c" at point C is a signal produced by superimposing the input signal and the reflected wave, it is equal to "$\sin \omega t+\sin \omega (t-2t_d)$" which, in turn, is equal to $2\sin \omega (t-t_d) \cos \omega t_d$.
If signal "e_d" at point D is given an attenuation factor of K, then it is equal to $2K\sin \omega (t-t_d) \cos \omega t_d$.
Circuit output "e_o" is the difference between the "e_b" and "e_d" signals and so :

$$e_o=\sin \omega (t-t_d) -2K\sin \omega (t-t_d) \cos \omega t_d$$
$$= (1-2K\cos \omega t_d) \sin \omega (t-t_d)$$

The output amplitude is $1-2K\cos \omega t_d$ and its characteristics are proportionate to the cosine waves.

When attenuation factor K is changed, It is possible to adjust and compensate the amplitude without affecting the group delay response (t_d=constant).
It is possible to select the auto mode in which a DC voltage corresponding to the burst level is fed back in order to keep the burst level of the video signal in the demodulator output constant or the manual mode in which adjustment is made using the equalizer control on the level control panel.

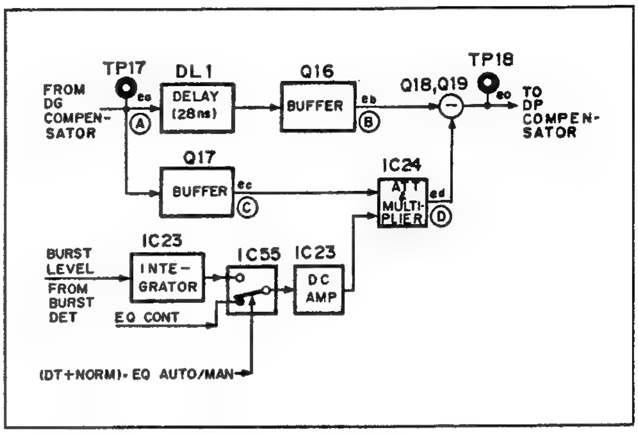


Fig. 4-3-13. RF Equalizer 1 (VO-16)

(5) DP compensator (VO-16 board)

The RF equalizer 1 output (TP18) enters the DP compensator.
The circuit is a phase equalizer composed of differential amplifier IC21 as well as C447, L20, R357 and RV25 and 26. It compensates the differential phase by varying only the phase characteristics without changing the amplitude characteristics. The RF signal whose differential phase has been compensated is then sent to the RF equalizer 2 and RF envelope detector circuit.

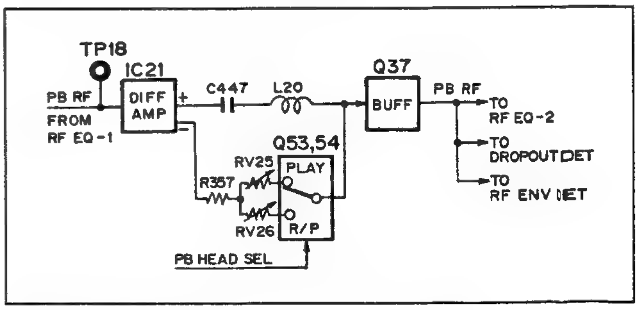


Fig. 4-3-14. DP Compensator (VO-16)

(6) RF equalizer 2 (VO-16 board)

This is the second stage RF equalizer and its configuration does not differ in any significant way from the first stage RF equalizer. It is here that the equalizer adjustments for the R/P head (RV28) and PLAY head (RV27) are made.

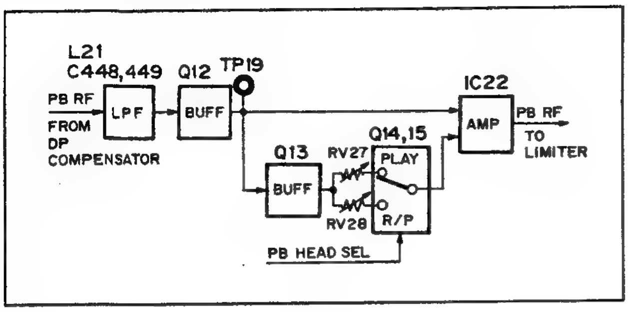


Fig. 4-3-15. RF Equalizer 2 (VO-16)

(7) RF envelope detector (VO-16 board)

One output from the DP compensator enters the RF envelope detector where its peak is detected. The peak detection output signal (TP20) is divided so that 3 separate signals are formed : the RF ENV signal (TP22) for the DT circuit, the RF LEVEL signal (TP23) for the RF meter and the RF ENVELOPE signal (TP24) for the waveform monitor output.
The RF ENV signal for the DT circuit is produced by passing the peak detection output through the buffer amplifier. The RF LEVEL signal for the RF meter is produced by sampling and holding the peak detection output field by field. The RF ENVELOPE signal for the waveform monitor output is produced by inserting a 0V DC voltage using a 9.5 μ sec pulse created from the horizontal sync pulse into the peak detection output.

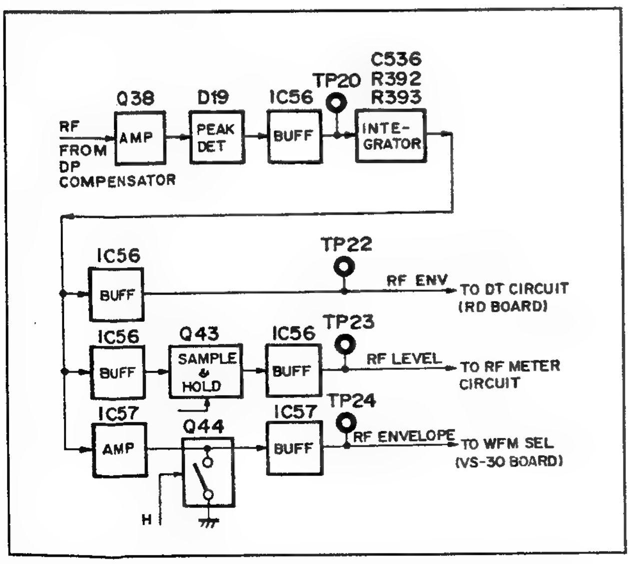


Fig. 4-3-16. RF Envelope Detector (VO-16)

(8) Dropout detector (VO-16 board)

Due to marks, damage or dust on the tape, the level of the playback RF signal may fall sharply and drop below the threshold level of the demodulator. When these variations occur, they are called dropouts and they appear as noise in the demodulator output. The dropout detector circuit serves to detect drops in the level of the RF signal and also to detect the length of the period (dropout width) during which the level has dropped.
The RF signal which has arrived from the DP compensator has its frequency response compensated by Q39 and it is then supplied to the inverted input pin of voltage comparator IC61. Meanwhile, the peak detection output of the RF signal is integrated with the long time constant of R395×C454 (approximately 50msec) and supplied to the non-inverted pin. Any reduction in the RF signal level is detected by comparing these two input levels.
Next, retriggerable monostable multivibrator IC62 is triggered by this voltage comparator output. If the next trigger pulse arrives within the time constant of the monostable multivibrator, the Q output (TP21) level of IC62 is kept high. If it takes a long time before the next trigger pulse arrives or, in other words, if the RF signal is missed, the Q output level is set low. The detection time constant for the dropout length (width) is selected by the operating mode of the VTR. In the FAST BIDIREX mode the time constant is extended while in other modes it is reduced. The DO pulse created in this manner is sent to the CK board and to other boards as well.

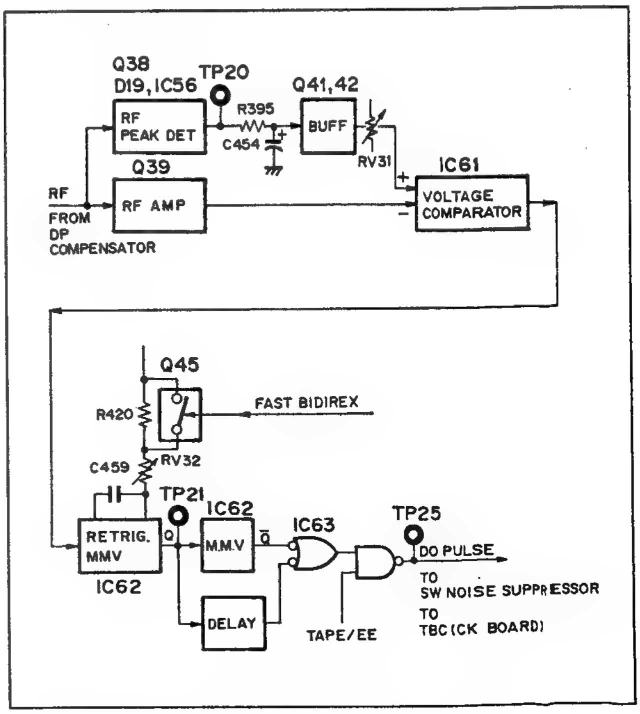


Fig. 4-3-17. Dropout Detector (VO-16)

(9) White reference marker inserter (VO-16 board)

In order to facilitate the deviation adjustment of the modulator, a circuit is provided which inserts the output of the crystal oscillator, whose frequency (10MHz for NTSC ; 8.9MHz for PAL／SECAM) corresponds to 100% white, into the EE RF signal. The insertion of this white reference marker is turned on／off by the select menu [S82. WHITE REFERENCE]. The insertion line is designated by the initial setup menu [I81. WHITE REF INS LINE].

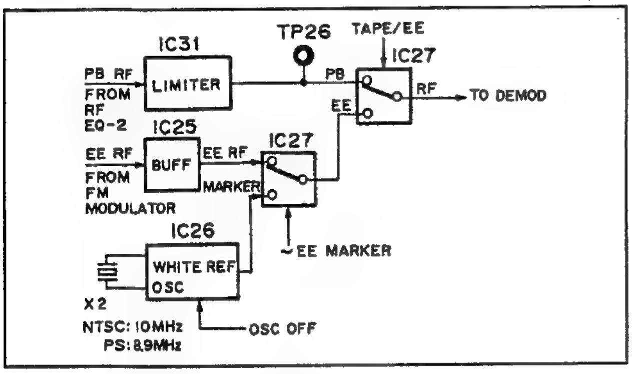


Fig. 4-3-18. White Reference Marker Inserter／EE-PB Selector (VO-16)

(10) EE／PB selector (VO-16 board)

In IC27, the EE signal which has passed through the white reference marker inserter and the PB RF signal (TP26) which has been ECL converted by IC31 serving as a limiter are selected by the TAPE／EE signal.

(11) FM demodulator (VO-16 board)

The configuration of the FM demodulator is described below. One part of the balanced input RF signal passes through a buffer amplifier ; another part passes through delay circuit IC32, they are connected in a wired OR format, the (+) and (−) sides are AND-ed and an output is provided. If it is assumed that the amount of delay provided by the delay circuit is "td," then the RF signal is converted into a pulse train with pulse width "td" and with a frequency which is double the input frequency. This output is demodulated into the video signal by passing it through low-pass filter FL3.

In this process, the carrier frequency is doubled and separated from the video band and so this facilitates separation. The output is taken out by a balanced circuit which uses a charge pump and so the basic frequency components of the carrier can be canceled out.

One part of the low-pass filter output (TP28) is supplied to the AGC feedback circuit which is composed of IC36 and 38. This circuit serves to detect the DC level of the pedestal portion in the demodulated video signal and to control the delay time "td" of the delay circuit in the demodulator so that the DC voltage is always 0V.

Another part of the low-pass filter output (TP28) is supplied to the switching noise suppressor circuit via the video amplifier composed of Q31-35 and the de-emphasis circuit composed of Q40, R500-503, RV41, C479 and C480.

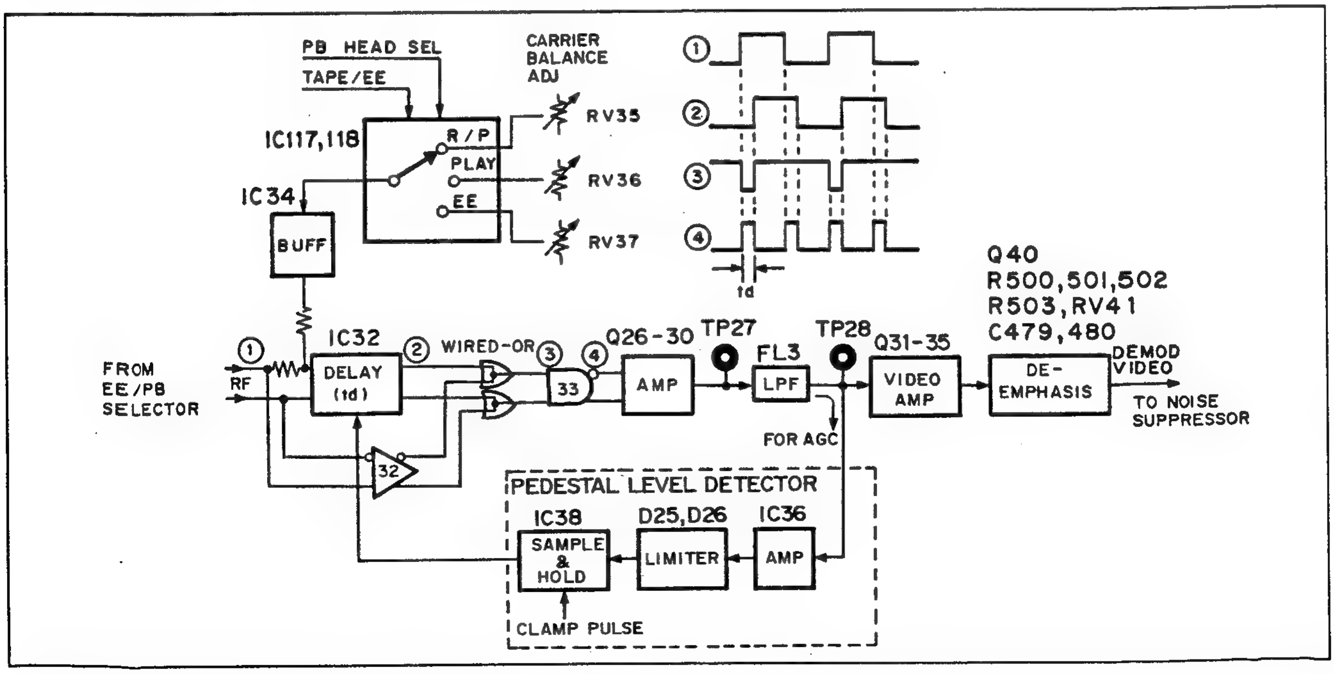


Fig. 4-3-19. FM Demodulator／Carrier Balancer (VO-16)

(12) Carrier balancer (VO-16 board)

One factor which results in the generation of moire is the deterioration in the symmetry of the RF signal waveforms due to non-linearity in the circuit, and this gives way to carrier leak in the modulator output. The carrier balancer circuit functions to DC shift part of the balanced input of the demodulator, control the symmetry of the RF signal waveforms and suppress any carrier leak in the demodulator output.

The DC voltages which have been respectively set at the R/P head side (RV35), the PLAY head side (RV36) and EE mode (RV37) are selected by the analog switchers IC117 and IC118, they pass through buffer amplifier IC34, and they are added to one of the demodulator's balanced inputs by resistors.

(13) Switching noise suppressor (VO-16 board)

The de-emphasized video signal enters the switching noise suppressor circuit where the various types of switching noise listed below and dropouts are replaced by the DC level (pedestal level) determined by RV15.

- Switching noise generated when the PLAY head is selected
- Switching noise generated when the RF signal is selected by the TAPE/EE signal
- Switching noise generated when the white reference marker insertion is selected on/off.
- Dropouts

To deal with the switching noise, 1.9 μ sec pulses are created by IC71 and their period is replaced by the DC voltage.

The noise suppressor output is supplied to 6dB amplifier IC37 and its gain is adjusted by RV16. The video signal then passes through buffer amplifier IC39 and low-pass filter FL2 (TP30) which is mainly designed to improve the signal-to-noise ratio, and it is sent to the two output buffers, IC40 and IC41.

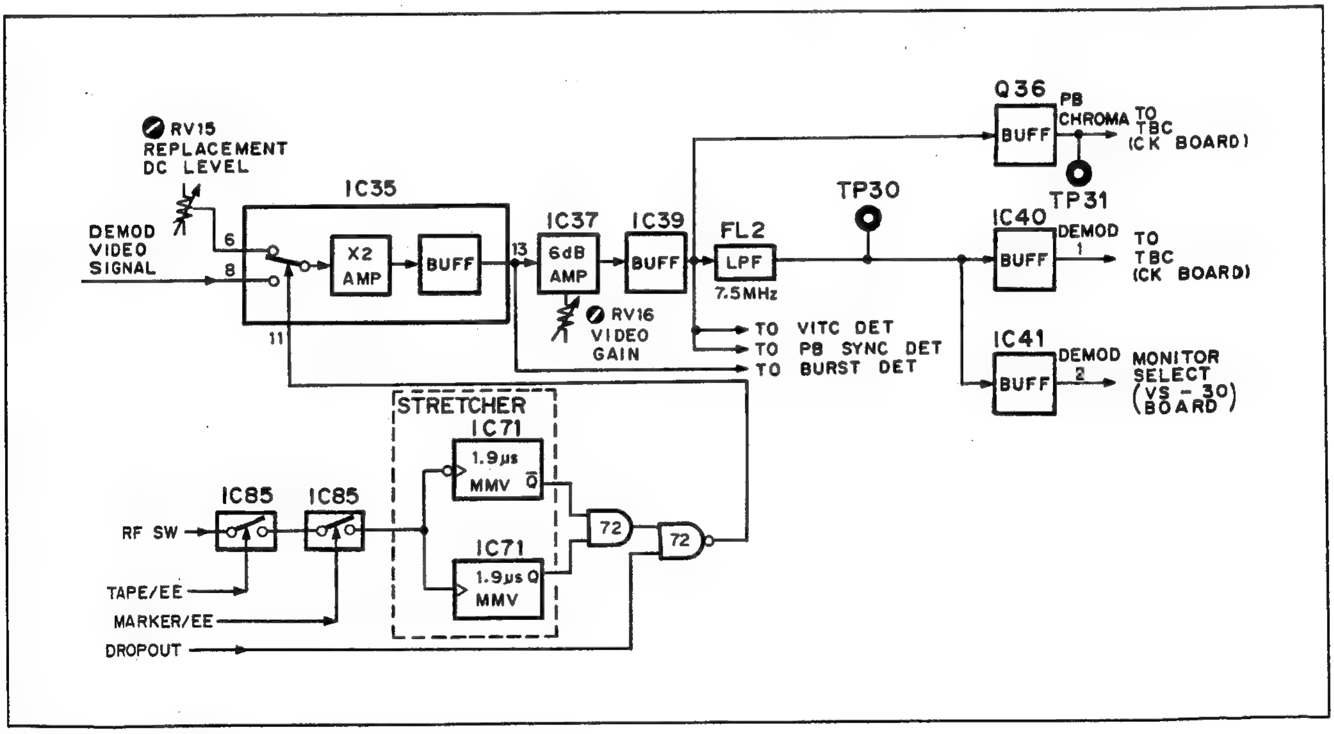


Fig. 4-3-20. Switching Noise Suppressor (VO-16)

(14) PB sync detector (VO-16 board)

The PB sync signal is an important signal which is used as a reference for the servo system and TBC write clock pulse generator, and so careful attention has been paid to how it is detected.
The PB VIDEO signal, which has been output from the 6dB amplifier of the switching noise suppressor, passes through buffer amplifiers IC67 and 68, and through the low-pass filter composed of L13 and C260 where its high-range components are filtered out.
IC69 performs a rough form of sync separation and a positive sync pulse is output. IC111-3, IC70-4 and IC73-12 configure a circuit which rejects half H pulses.
In IC75, the PB VIDEO signal is sampled and heldby the leading and trailing edge pulses of the sync-separated signal, and the sync tip level and pedestal level are both detected. The PB sync signal is produced by comparing in IC76 the voltage of the PB VIDEO signal with that of exactly one-half of the sync tip to pedestal level. This method enables an accurate PB sync signal, which is detected at the half level between the pedestal and sync tip, to be produced even if when such factors as APL fluctuations in the input signal, bounce or defective clamping by the modulator or demodulator are present.

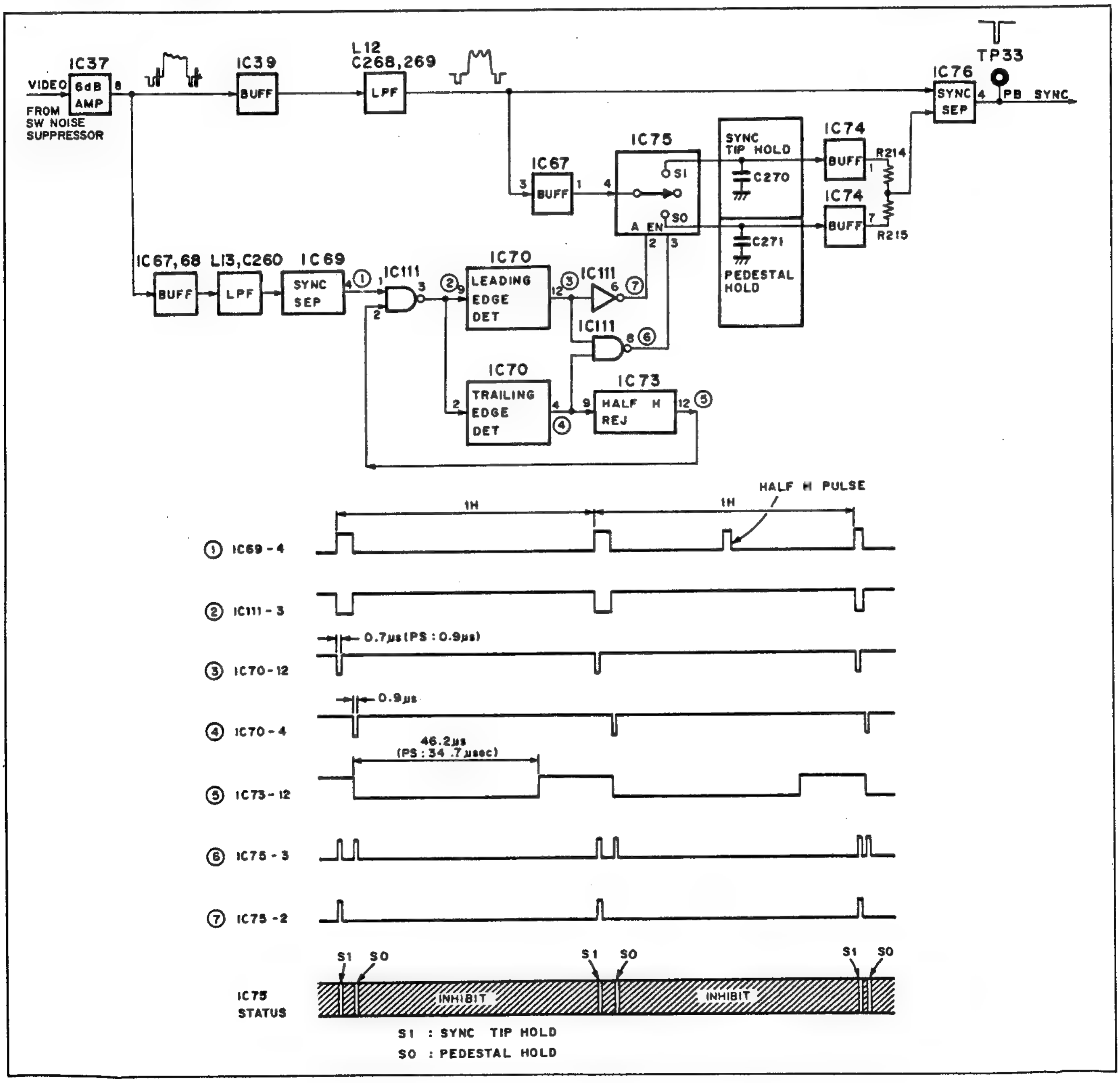


Fig. 4-3-21. PB Sync Detector (VO-16)

(15) VITC detector (VO-16 board)

This circuit serves to create a level corresponding to 40IRE (or 300mV with PAL/SECAM) from the sync tip level and pedestal level which were detected by the PB sync detector, and to compare its voltage with that of the PB video signal. The figure of 40IRE (or 300mV with PAL/SECAM) corresponds to virtually the center level of the VITC signal.

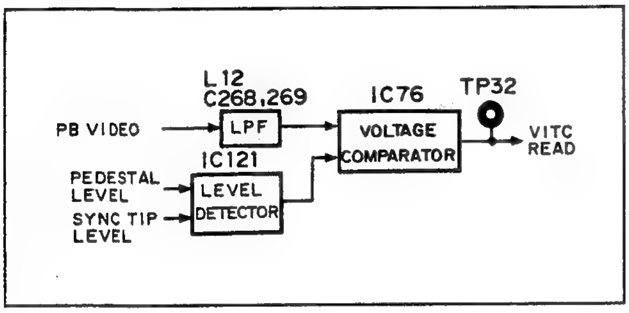


Fig. 4-3-22. VITC Detector (VO-16)

(16) Burst detector (VO-16 board)

This circuit serves to detect the burst level which is used to control the auto equalizer and to detect whether the burst is present or not. The PB video signal which is output from the noise suppressor has its level adjusted by RV17 and its chroma components are separated by the bandpass filter which is composed of L14-16 and C272-274. The envelope of the chroma signal is detected by IC77 and 79. IC80 samples the burst portion of the envelope detection output (TP34) using the clamp pulses generated by the PB sync detector circuit. The sampled signal passes through buffer amplifier IC79 and is sent to the RF equalizer section as the burst level signal (TP35).
This burst level signal detects the level in the vicinity of 0.75V using voltage comparator IC82 and it triggers retriggerable monostable multivibrator IC81 with its pulse width of 15msec. If the burst signal is present in the PB video signal or, in other words, if the PB video signal is the color signal, the IC81 output level is set high.

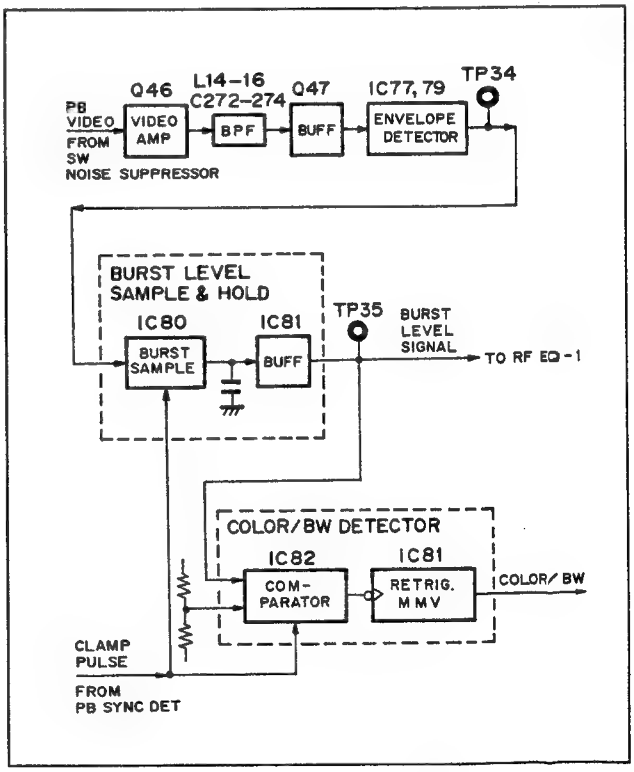


Fig. 4-3-23. Burst Detector (VO-16)

(17) PB V/PB H detector (VO-16 board)

These circuits serve to detect the PB V and PB H signals from the PB sync signal. Their outputs are used to determine the position where the white reference marker is to be inserted and they also serve as the servo reference signal.
In the PB V signal detector circuit, first IC87, 88, 89 and 105 are used to detect the trailing edge of the equalizing pulse before and behind the V sync pulse. A window is applied by the pulse which has a 1/4V width and which is created from the PB V signal for the signal that was detected at the trailing edge of the equalizing pulse, and only the first and second equalizing pulses are taken out.
Next, the second equalizing pulse is detected. Using the first monostable multivibrator IC90 output (pulsewidth of 3/4H), the effective period of the second monostable multivibrator IC90 trigger pulse is limited to a range within 3/4H from the first equalizer pulse, and only the second equalizing pulse is made to serve as the effective trigger. As a result, the PB V signal, which has a width of 1.55msec (approx. 24H) and which has been triggered by the second equalizing pulse, is produced from pin 4 of IC90.
The PB H signal detector circuit is composed of 2-stage monostable multivibrator IC95 which is triggered by the PB sync signal. The first stage functions to reject the half H with pulses having a width of 50.8 μ sec. The second stage functions to create pulses with a width of 4.8 μ sec and to output them as the PB H signal.

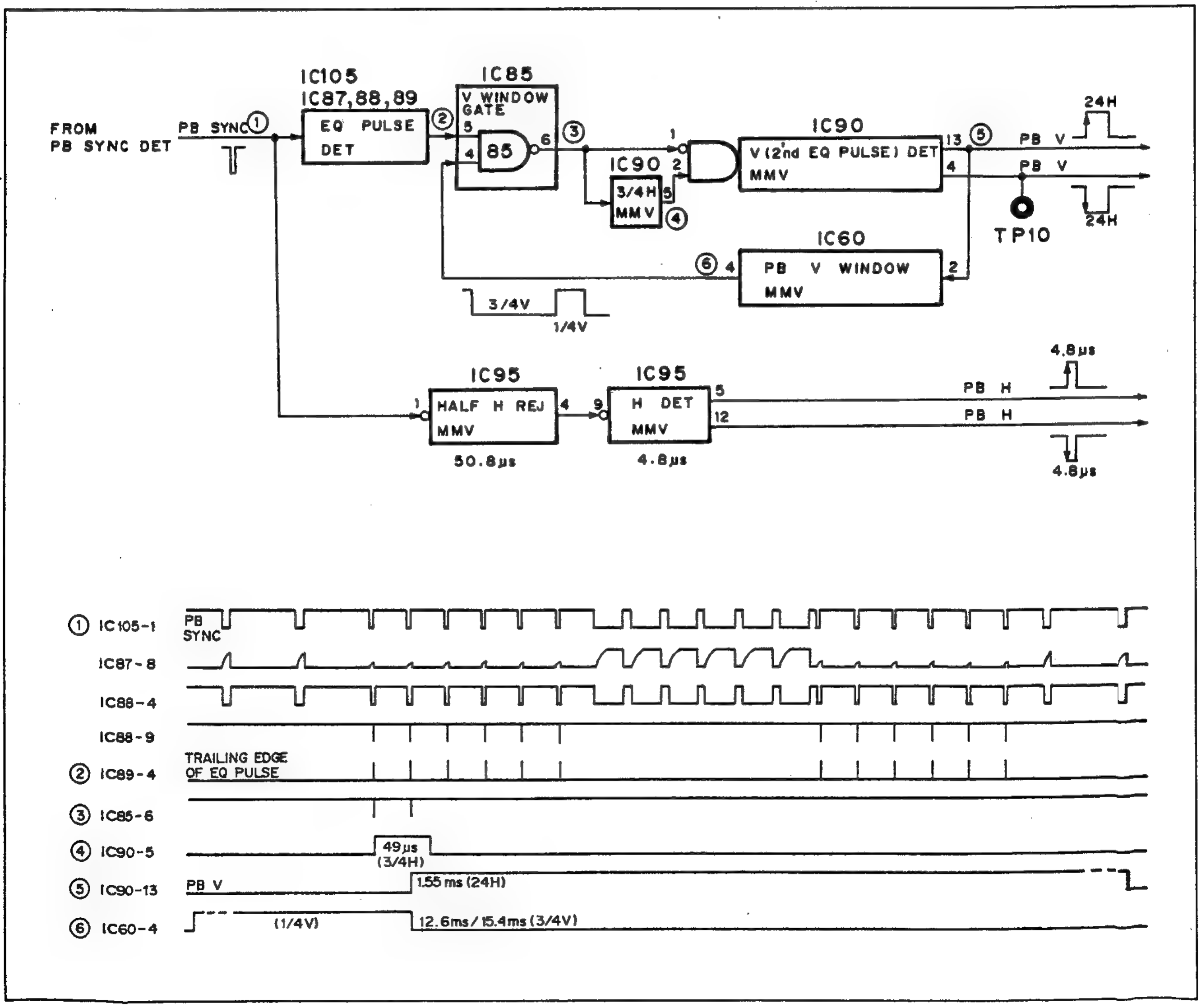


Fig. 4-3-34. PB V/PB H Detector (VO-16)

(18) EE/MARKER signal generator (VO-16 board)

This circuit generates the signal which determines the insertion line and insertion position for the white reference marker which is inserted into the EE signal. The command signal for inserting the white reference marker is sent from the CPU on the SV-90 board to the VO-16 board via the SV bus. Serial-parallel conversion is performed by I/O expander IC99 so that the signal is converted into 8-bit parallel data corresponding to the respective lines, and the signal is then sent to the S0-S7 input pins of multiplexer IC93.

IC92 is a binary counter which is driven by the PB H signal and its output selects one of the S0 through S7 input pins of the multiplexer. The starting point for the count is the starting point for the insertion of the white reference marker and so the timing signal for the insertion starting point is created by IC106 and IC91 from the PB V signal, and this is sent to the enable pin of the counter. As a result, the S0-S7 pins of IC93 correspond to every 2 lines from line No.10 through line No.25 (or line No.6 to 21 and No.319 to 334 in the PAL/SECAM system). IC94 and 96 function to prohibit the marker from being inserted in the horizontal blanking area and to control marker OFF.

(19) I/O expander (VO-16 board)

I/O expander IC99 communicates with the main CPU on the SV-90 board through the SV bus. It converts the time-shared 8-bit serial signals into parallel signals. With parallel ports, the I/O can be freely designated. In this case, 4 ports (PD0, 1, 2, 3) are secured for input applications and 24 ports are secured for output applications.

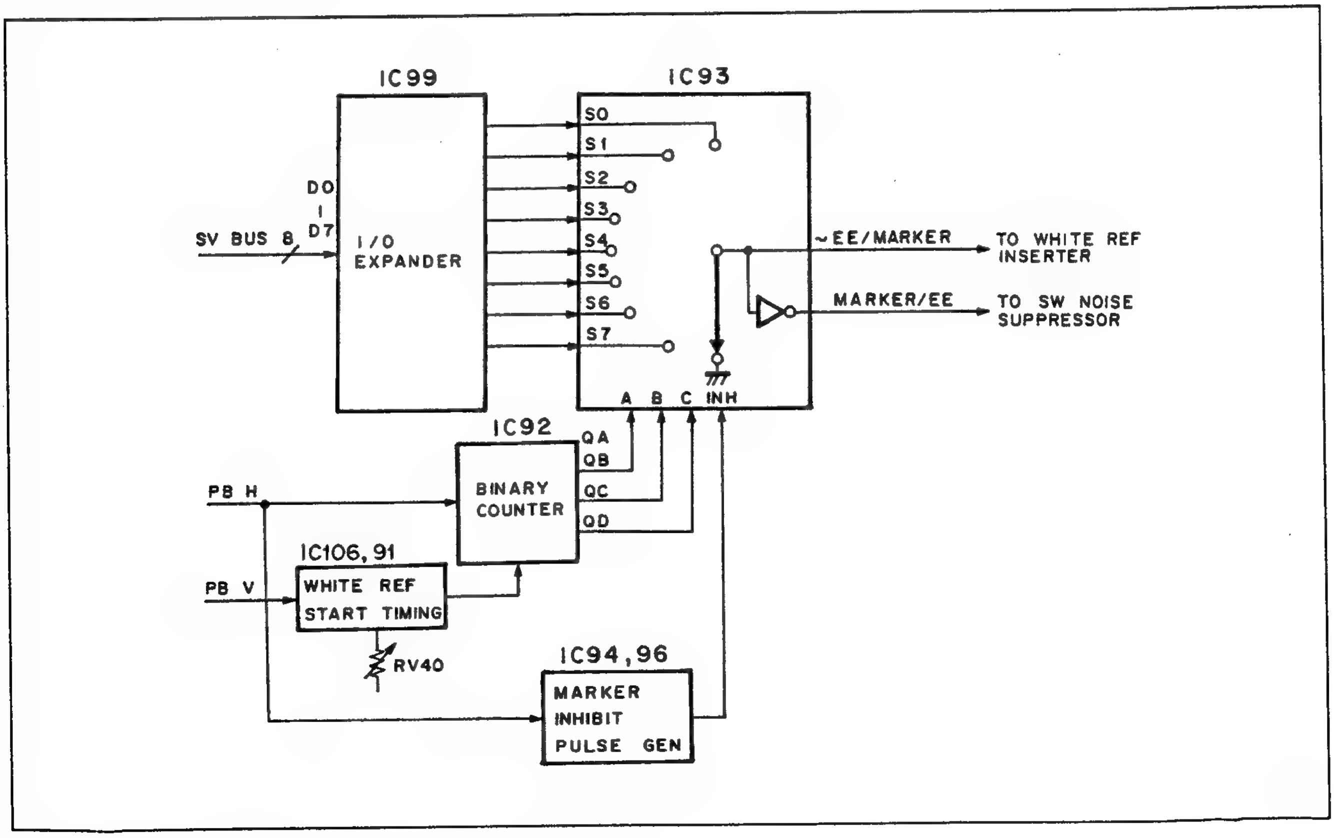


Fig. 4-3-25. EE/MARKER Signal Generator (VO-16)

4-4. TBC SYSTEM

4-4-1. Outline of TBC System

(1) Outline of circuit boards

The TBC system in both the BVH-3000PS and BVH-3100PS is composed of following circuit boards.
- CK-27 board
- RD-7 board
- PR-92 or PR-98 board (BKH-3020 or BKH-3060)

The user selects whether the standard processor PR-92 board/BKH-3020 or the high-quality processor PR-98 board/BKH-3060 is to be used.

(a) CK-27 board

The demodulated playback video signal is supplied to the CK-27 board where it is converted from analog into digital signals, its time base error is corrected and where freeze processing is undertaken. The time base error in the video signal which is caused by the tape/head system is corrected by first writing this signal into the 32-line main memory by the write clock (W CK) signal which is synchronized with the sync signal and the burst signal (the sync signal for the SECAM signal) of the playback video signal and then reading it out by the read clock (R CK) signal which is synchronized with the sync and the burst signal (the sync signal for the SECAM signal) of the reference video signal. The read clock (R CK) signal is generated on the RD board and the write clock (W CK) signal is generated on the CK board. The tape SC-H phase of the PAL signal is also detected on the CK board.

Freeze processing refers to the process of writing the digital video signals, which have been read out from the main memory, into the field memory (4M bits) and reading them out when necessary. This function is used for the following 3 objectives.
- When the still picture mode is specified, the tape tension is released and the field data stored in the memory are read out and then output as a still picture. This eliminates any head-to-tape contact and protects both the tape and the heads.
- While the drum is rotating, the field data stored in the memory are read out and output as a freeze picture to the monitor.
- When the STOP button is pressed in the play mode or DT playback mode, the image applying during the instant when the STOP button was pressed is output as a freeze picture. In the shuttle mode, the image applying during the instant when the tape has stopped is output as a freeze picture only when the PLAY head has been selected.

(b) RD-7 board

The RD-7 board serves to generate the read clock (R CK) signal for reading out the data from the main memory, the reference clock signal for decoding/encoding and the reference signals which are synchronized to the reference video signal, such as the blanking signal, sync signal and burst signal which are replaced by the PR board after D/A conversion. The reference SC-H phase of the PAL signal is also detected on the RD-7 board.
Besides the circuitry which generates the TBC reference signals, the RD-7 board also contains the servo reference circuit and DT control circuit.

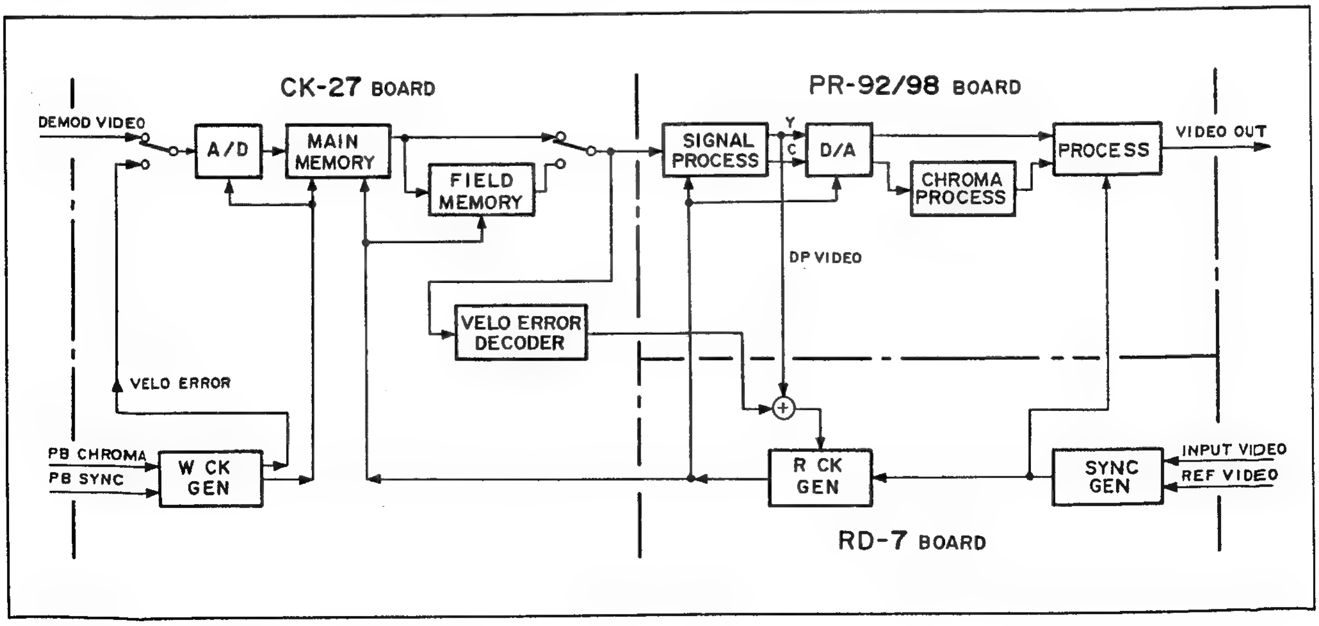


Fig. 4-4-1. Configuration of TBC System

(c) PR-92 board (BKH-3020)

The digital data read out from the main memory and field memory, on the CK-27 board are supplied to the PR-92 board. After the digital data have completed the dropout compensation and Y line adding processes, they are D/A converted and sent to the analog processor circuit.

The analog processor circuit serves to ensure that the chroma signal has the correct phase vis-a-vis the reference burst signal phase during variable speed playback. Also, it replaces the sync signal and burst signal with the sync and burst signals which have been synchronized with the reference video signal. The video level, chroma level and black level (PAL system only) can be adjusted, and dark clipping is also undertaken.

(d) PR-98 board (BKH-3060)

Although the basic circuit configuration of the PR-98 board is identical to that of the PR-92 board (standard processor : BKH-3020), a new Y-line adding and a dropout compensation system which employs adding lines before and after are featured. In particular, the picture quality in the DT mode is greatly improved as a result.

(2) Outline of video signal system

The playback video signal is supplied via the pre-filter on the CK-27 board to the A/D converter which converts it into 8-bit data at a sampling frequency of 4Fsc ($1135F_H$ for the SECAM signal). The converted digitial data are written into the 32-line main memory and read out by the 4Fsc ($1135F_H$ for the SECAM signal) clock signal of the reference system. The data which have been read out are output to the PR board. The PR board performs such operations as Y/C signal separation, dropout compensation and line adding, it replaces the pedestal level with a constant value and converts the data into an analog signal using its D/A converter. The chroma level and the black level (for PAL only) are controlled, the reference sync signal and burst signal (ID signal for the SECAM signal) supplied from the RD-7 board are added to the signal, and the resulting signal is the BVH-3000PS/3100PS output signal.

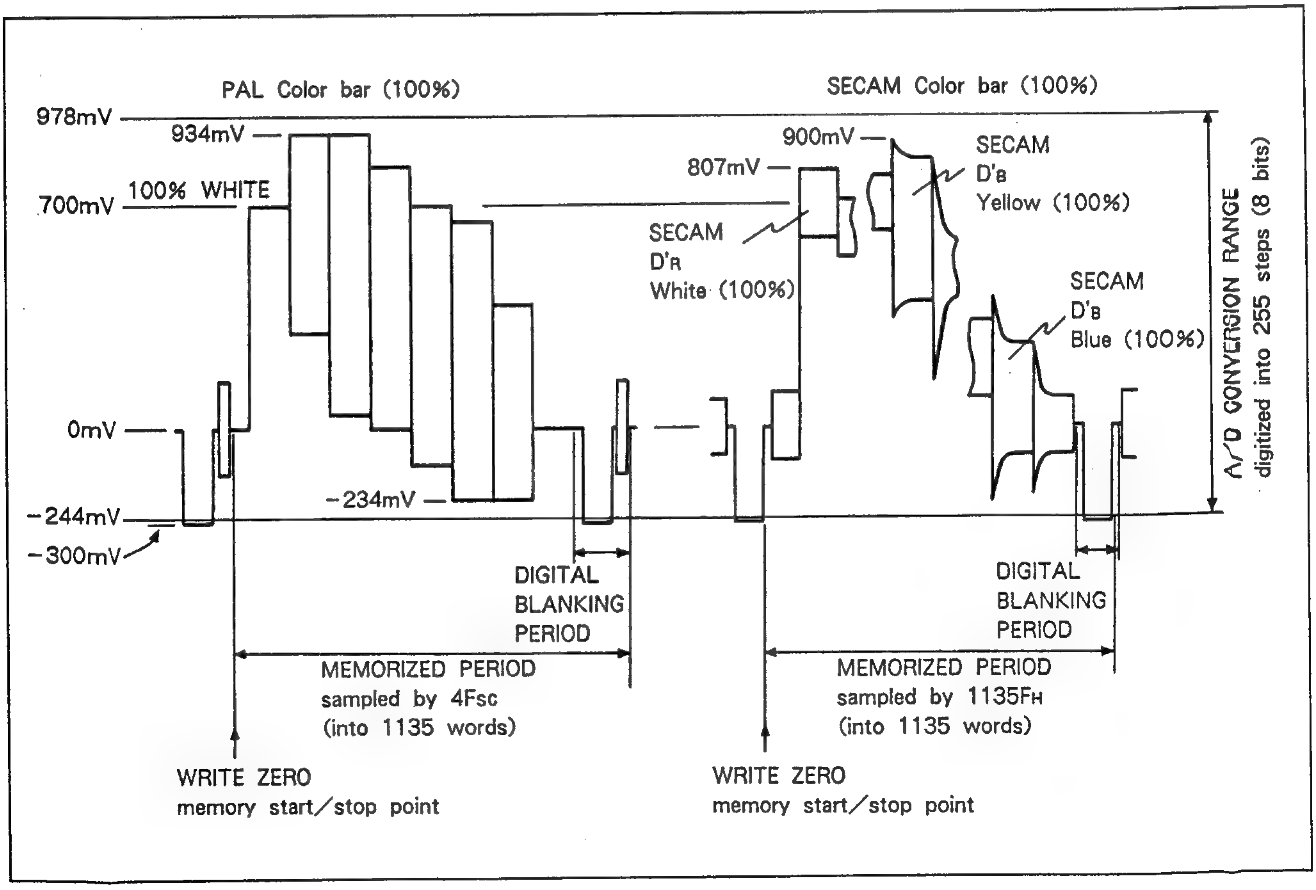


Fig. 4-4-2. TBC Processing of Video Signal

(3) Outline of control signal system

In the case of the PAL signal, the 4Fsc write clock (W CK) signal is generated by the APC system which uses the burst phase of the playback signal as the reference, and this is employed for A/D conversion and for memory writing. In this machine, the time base of the DT playback signal as well as the normal playback signal is corrected. Consequently, the W CK frequency is locked by the AFC to the PB sync signal so that it can be made to track the frequency fluctuations of the playback signals. This generation system enables the W CK signal to be color-locked to the playback signals which are played up to a a maximum of 8 times faster or slower than the normal tape speed. In the case of the SECAM signal, the 1135FH W CK signal is generated by the APC system which uses the PB sync signal as the reference.

The write zero (W ZERO) signal which indicates the start of main memory writing is always generated at a constant timing from the edge of the H sync signal. It is synchronized with the subcarrier frequency W SC signal (produced by dividing the W CK frequency by 4) at the write side. When this synchronizing occurs, the phase of the W SC signal is inverted every 2 lines so as to safeguard against a shift every 2 lines in the timing of the W ZERO signal equivalent to a half cycle of the subcarrier.

In the case of the PAL signal, velocity errors are compensated. The velocity error is detected through phase comparison of the W SC signal with the signal which has the phase of one subcarrier wave near the center of the playback burst signal. The detected error voltage is inserted in the horizontal blanking period of the playback video signal prior to A/D conversion, it is sent to the read-out side via the main memory and the phase of the R CK signal is modulated by means of second order approximation. This provides highly accurate velocity error compensation and reduces the residual phase error during the color processing to less than ±3 nsec.

The R CK signal used for D/A conversion and memory readout is created by multiplying 4-fold the subcarrier which is phase-locked to the burst signal of the video signal selected as the TBC reference signal in the RD-7 board. The TBC reference signal can be specified independently from the servo reference signal. For the PAL signal, the phase of the R CK signal is modulated for both velocity error compensation and DP compensation, and it can be controlled externally so that the burst-chroma phase can be adjusted.

The read zero (R ZERO) signal indicating the read start of the main memory is created at a constant point from the horizontal sync signal, as with the W ZERO signal. The phase of this signal as opposed to the phase of the horizontal sync signal can be adjusted across a 5-step range, with 1 step serving as a subcarrier cycle. This enables the TBC output video phase to be shifted up to a maximum of ±0.45 μ sec. The phase of the subcarrier at the readout side for synchronizing the R ZERO signal is inverted 2-line by 2-line so as to accommodate the phase inversion of the W SC signal. The main memory write address (W ADDRESS) signal and read address (R ADDRESS) signal are created from the W CK and R CK signals. A total of 2k words are allocated to 1 line in the main memory and approximately 1135 words are addressed.

Dropouts are compensated for on the main memory read-out side PR board. The digital video data (WD2ⁿ) before being written in the main memory are replaced by "1" (FFH) while the DO pulse is input so that the DO pulse which is the signal that indicates the dropouts in the playback video signal is stored in the memory. The "1" (FFH) existing in the original digital video data is replaced with "FEH." The DO pulse is written into the main memory along with the W N/I and W O/E signals which indicate the line inversion of the subcarrier phase on the write side. As with the video data, the written data are read out by the R CK signal of the reference system. The pulse widths and delays of the Y DO signal and C DO signal are adjusted and these signals are used as the timing signals for dropout compensation.

The sync generator is provided on the RD-7 board and this generates the TBC reference sync signals (TBC SYNC, TBC VD) as well as the blanking and burst flag signals. Either the signal supplied to the REFERENCE VIDEO INPUT connector or the signal supplied to the VIDEO INPUT connector is selected and this is input as the external sync signal to the sync generator. The "S86 : TBC REF SELECT" select menu decides which of the two signals is selected. In addition, any line from line 7 (320) to line 22 (335) can be selected as the vertical blanking line. The "I80 : BLANKING LINE" setup menu decides which line is selected.

The PAL reference video signal and off-tape video signal SC-H phase are respectively displayed by the LEDs on the meter panel.

4-4-2. Input Circuit, A/D Converter and Memory Circuit (CK-27 Board)

(1) Input circuit and A/D converter (CK-27 board)

The DEMOD 1 video signal which has been played back is supplied through R1 to pre-filter LPF1. The output impedances of the VO-16 board is approximately 50 ohms and so the 100 Ω R1 resistance is added here for LPF1 impedance matching. The level of the LPF1 output is first adjusted by RV1 and then the signal is amplified 6 dB by ICB21.
Fixed bias is applied by RV2 to the ICB21 output and pedestal clamping is provided by IC3, B19 and B17. The pedestal level is determined by RV3.
The pedestal-clamped signal enters the ICC17 A/D converter where it is converted into 8-bit digital data by the 4Fsc write clock signal, and then its ECL level is converted into the TTL level by ICF17 and E17.

Fig. 4-4-4 shows the A/D conversion range. In the case of the PAL signal, the velocity error (an analog voltage) is inserted into the horizontal sync section. Switch IC3 is used to switch between the velocity error signal and the main signal line. As described in the following section, the Y DO, C DO, W N/I (PAL system only) and W O/E (or line identification with SECAM system) information is added to the digital video data which have just been A/D converted.

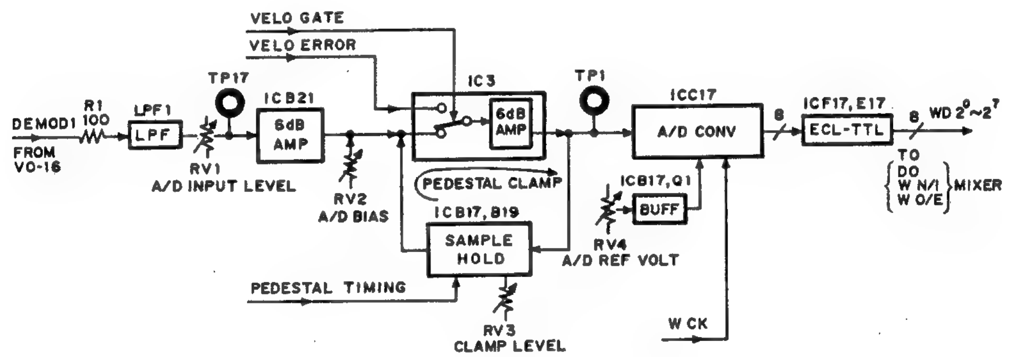


Fig. 4-4-3. Input Circuit and A/D Converter (CK-27 Board)

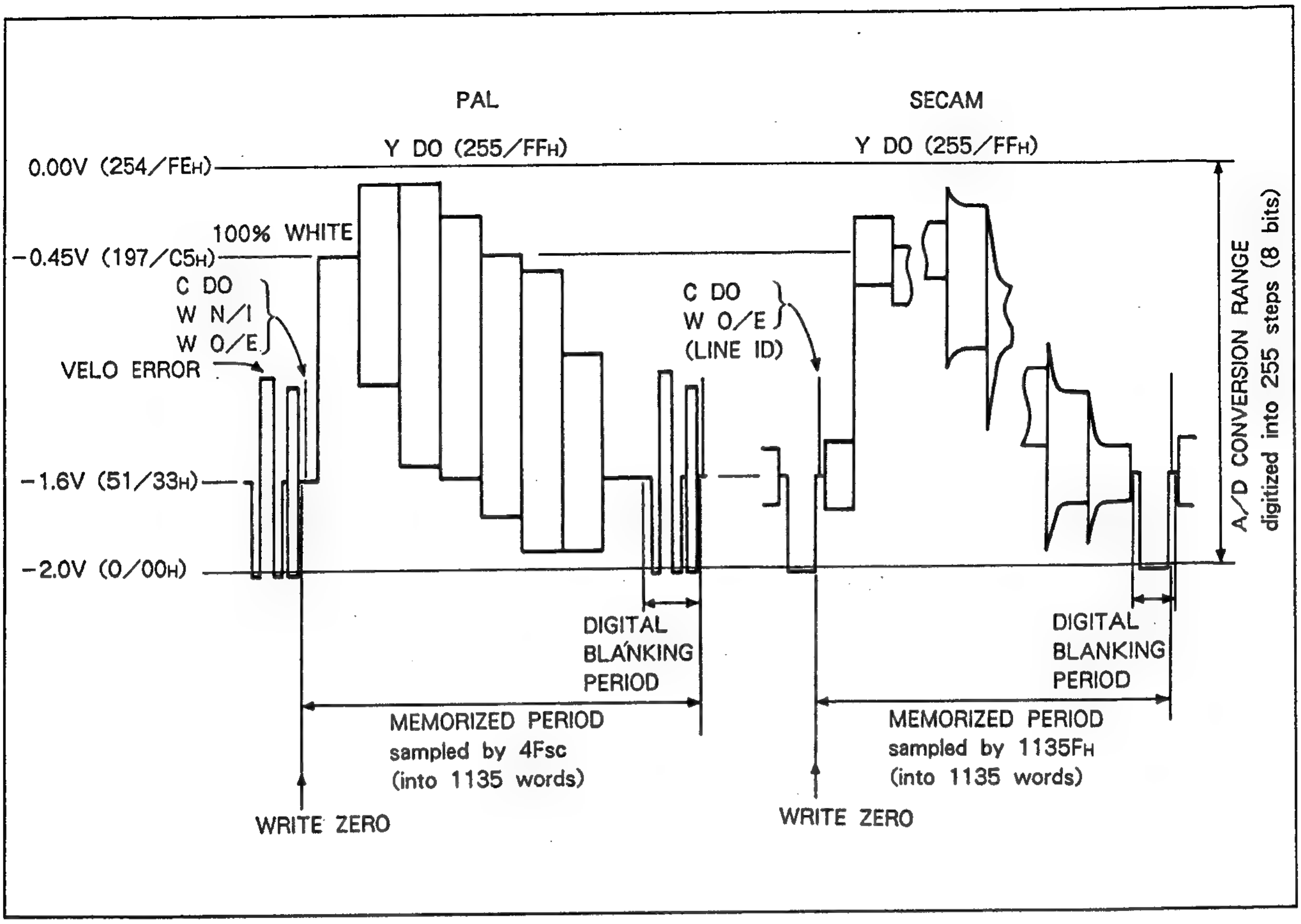


Fig. 4-4-4. A/D Conversion Range (TP1/CK-27)

(2) DO pulse, W N/I and W O/E mixer (CK-27 board)

It is here that the following signals are added to the 8-bit digital video data.

- Y DO (Y dropout pulse)
- C DO (chroma dropout pulse)
- W N/I (write normal/invert signal) : PAL system only
- W O/E (write line odd/even signal with PAL system ; DR' /DB' line ID signal with SECAM system)

The Y DO signal is added as FFH so as to accommodate the video data with the clock rate. Therefore, when FFH is in the video signal, it is treated as the DO pulse and so it is clipped to FEH so that it does not exist in the video data. The clipper is configured by ICF16 and ICJ12. ICF14 and ICF15 together replace the Y DO pulse with FFH and also add the C DO, W N/I and W O/E signals by means of the timing pulse. The C DO, W N/I and W O/E signals are 1-bit information per 1H and they are added at a position which is delayed by an amount equivalent to 2 clock pulses from the W ZERO signal.

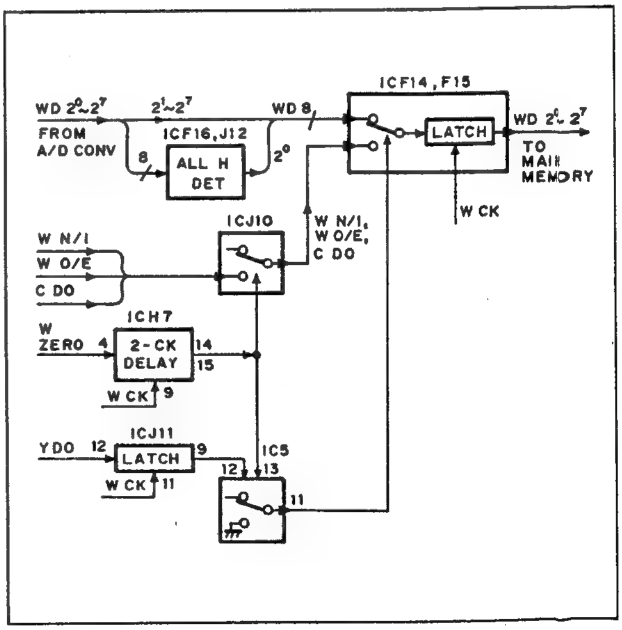


Fig. 4-4-5. Y DO, C DO, W N/I, W O/E Mixer (CK-27)

(3) Main memory (CK-27 board)

ICE14 and E11 (CXD1020Q) are a 1-8-1 serial-parallel-serial (S-P-S) converter. Eight MB8464 8k×8-bit SRAMs are used for the memory for a total size of 31 lines.
This section features a configuration which takes into account the fact not only that the write and read systems are not synchronized but also that the frequencies change.

The 30 Hp-p window is given to the memory since it is convenient for a ± (7H+ α) memory window to be provided even during DT playback at speeds ranging from +3 to −1 of the normal tape speed. Furthermore, during playback at +50 normal tape speed, the write clock signal has a frequency of approximately 27 MHz and sufficient access time to the memory is provided by the 8-phase serial-parallel-serial conversion.

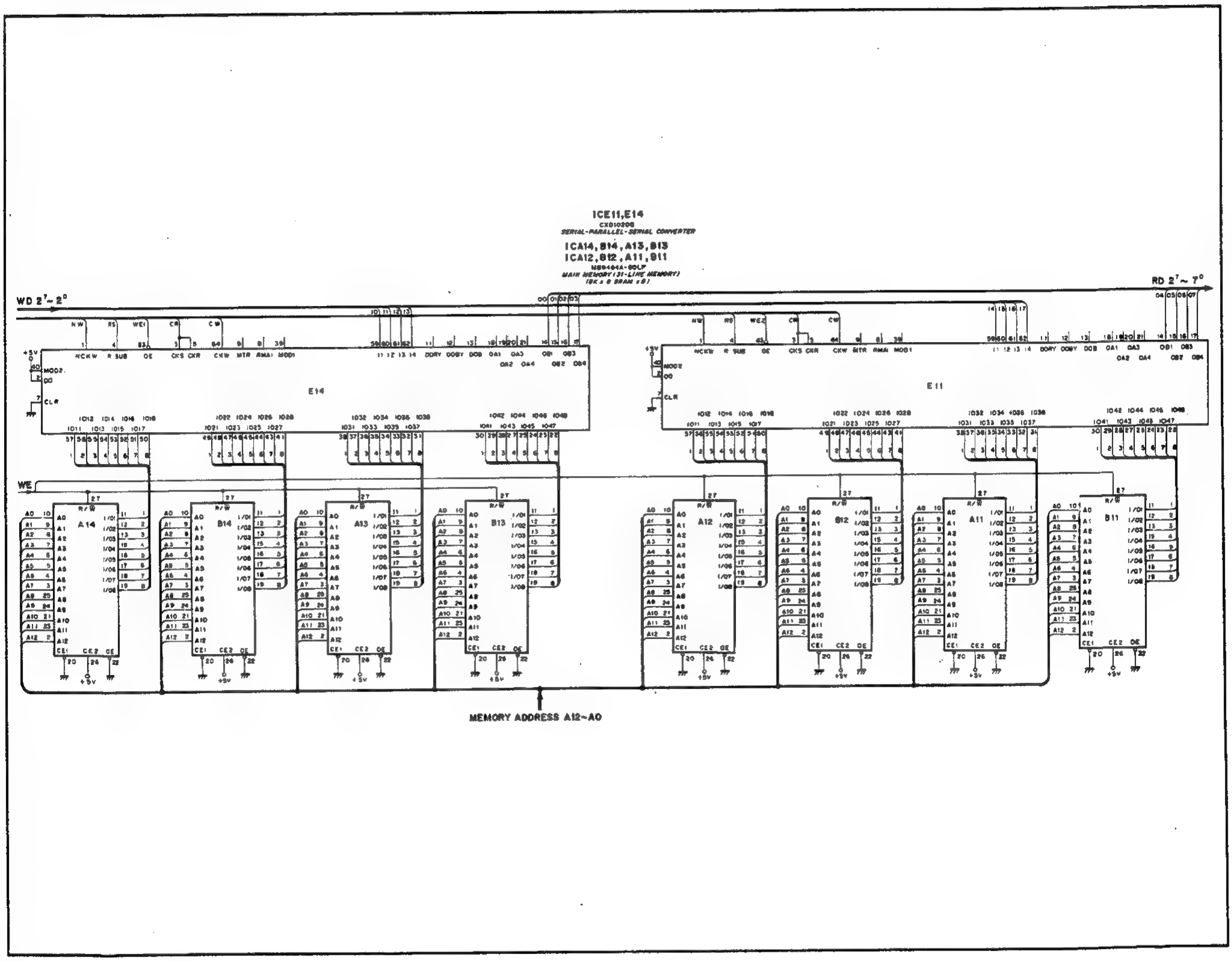


Fig. 4-4-6. Main Memory (CK-27)

Memory control is outlined below.
The 11-bit counter is configured by ICG7, G8 and G9 and 00 0000 1000 is loaded with each R ZERO signal. This is how the read addresses are created. Since an 8-phase drive is featured, the upper 8 bits form the read address which is set in address 1 by loading 00 0000 1000.

The write addresses are created by ICH9, H10 and H11. As with the read addresses, they are composed of the upper 8 bits. NCKW which is created by ICJ9, and J12 is the timing pulse for the serial-parallel conversion of serial-parallel-serial converter ICE14 and E11.

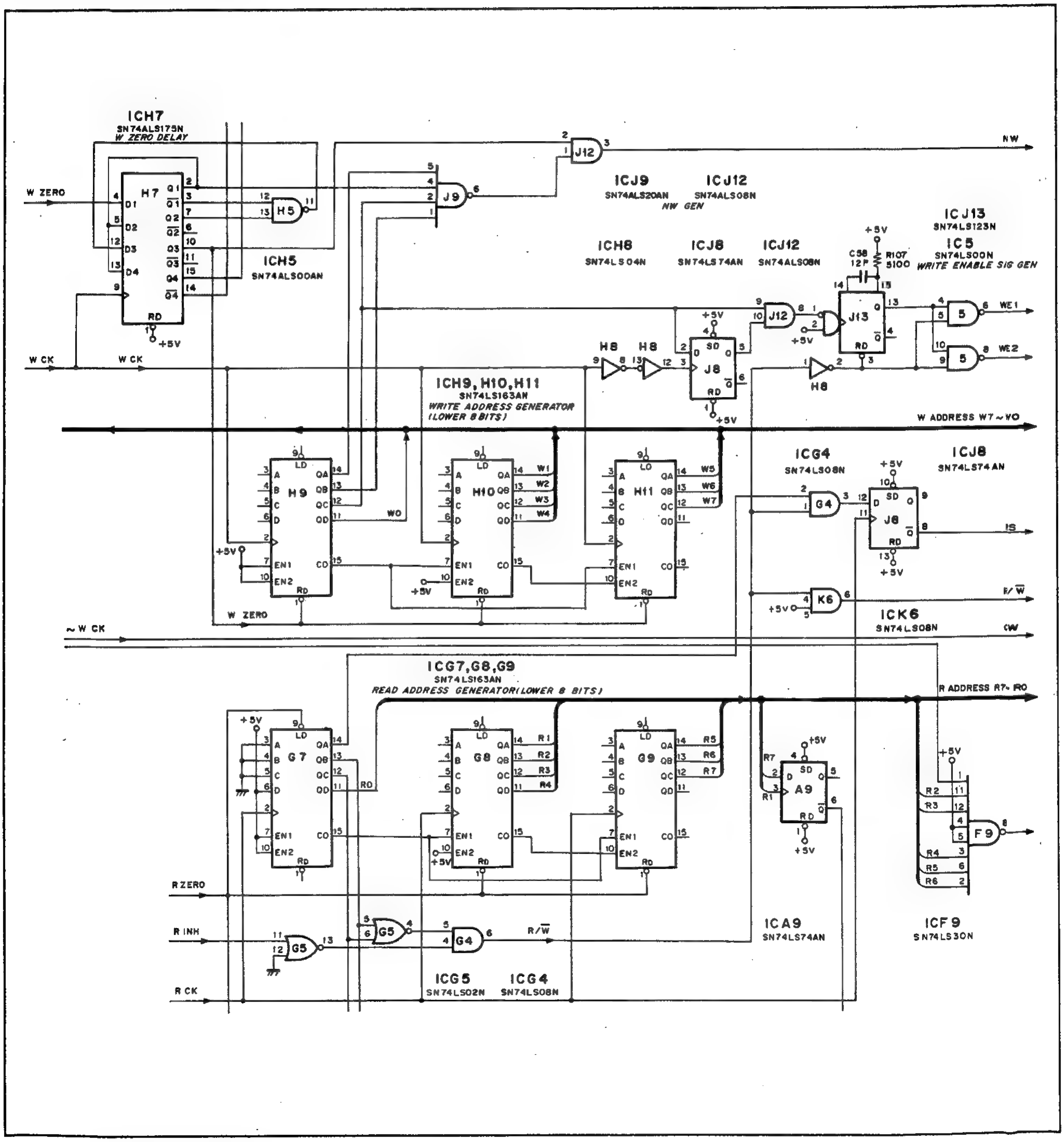


Fig. 4-4-7. Address Generator and Memory Control (CK-27)

The significant point of the memory control is the WE (write enable) signal generator which is configured by ICJ8, J12, J13 and IC5. The main memory circuit performs 3 read/write operations per one cycle by 8-phase.
The WE signal generator decides whether writing is possible or not and when it is possible, it outputs the WE signal. This is shown in Fig. 4-4-8. Since the write and read systems are not synchronized, this figure shows 3 different cases. In case 1, an attempt is made to trigger monostable multivibrator ICJ13 at pin 8/ICJ12 but since pin 2/ICH8 (read cycle) is low, the WE signal (pins 6 and 8/IC5) is not set low. Instead, the monostable multivibrator is triggered at the pin 2/ICH8 rise and the WE signal is output (set low) after the read cycle has been completed. In case 2, at times when the read cycle has arrived after the WE signal has been output, WE is output again upon completion of the read cycle. In such cases, writing is done twice. In case 3, it is not possible for writing to be done twice. When the second WE signal is incomplete, the writing will not be done properly the second time even if it is done properly the first time. In order to avoid this, a pulse with a width enabling the W cycle is output from pin 8/ICJ12 and the monostable multivibrator is not triggered at the pin 2/ICH8 rise.
The lower 8 bits of the memory address are obtained by switching between the read address and write address by means of ICF10 and F11 using the R/W signal. The lower 8 bits are the address inside 1 line. The memory addresses are composed of the lower 8-bit address and of the higher 5 bits which determine the line address. The higher 5 bits represent the V LOCK and memory jump controlled address.

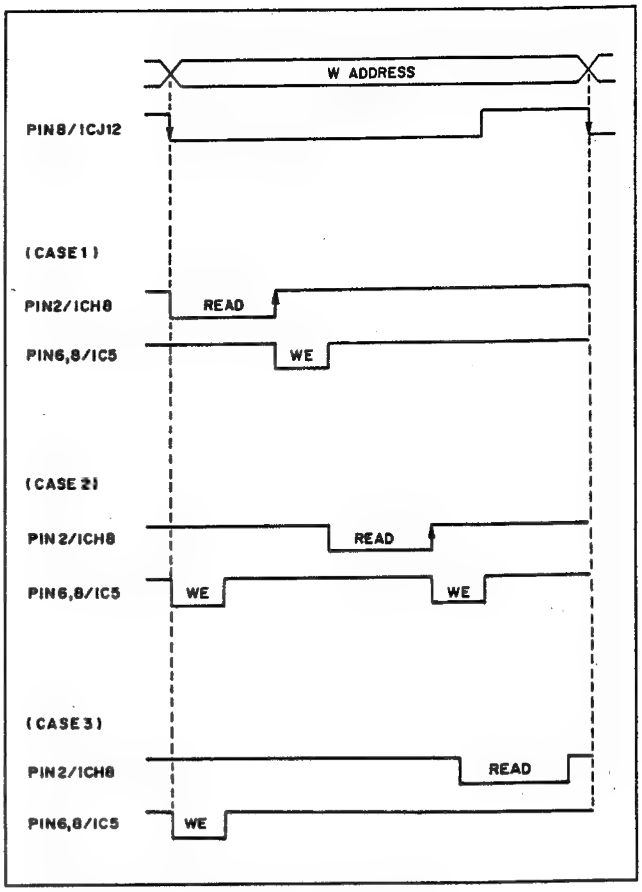


Fig. 4-4-8. WE Timing Chart (CK-27)

(4) V lock and jump control (CK-27 board)

ICG15 and H14 are the write line address generator and ICG14 and H15 the read line address generator. ICH13 and J15 provide memory jump control. ICF12 and G12 are the line address selector. The value of the write line address is latched by ICJ14 at the SEL PB V timing and this is then loaded in ICG14 and H15 by the SEL REF V timing. As a result, the read line address generated by ICG14 and H15 is locked to V. In order to read out from 2H before the velocity error which has been inserted into the sync section, ICF13 adds 2 to the read line address in this section.

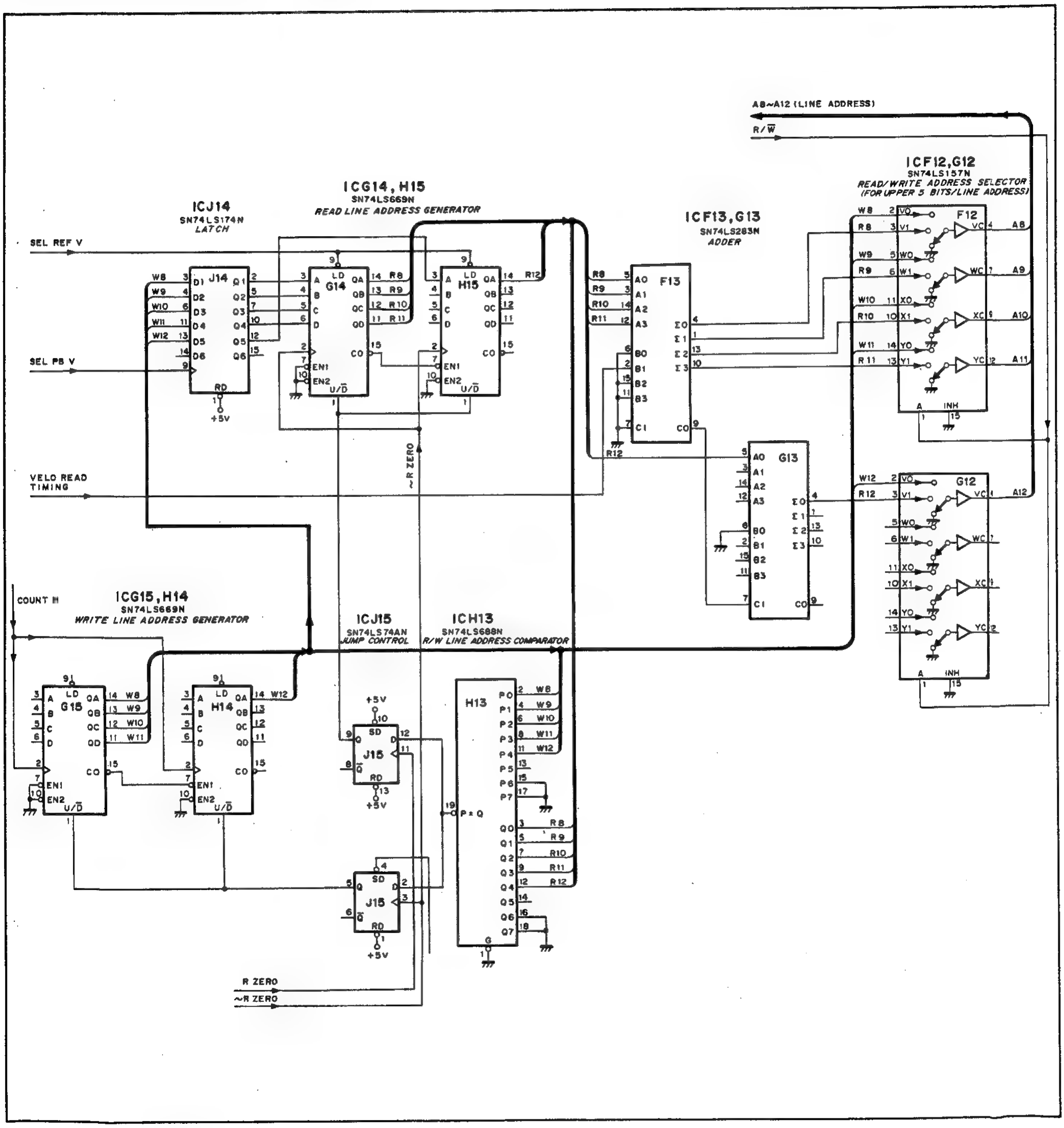


Fig. 4-4-9. Line Address Generator and Address Selector (CK-27)

The process described next is "jump control". When there is no time base error, the digitized video signal is written into the main memory at a timing which is 16H ahead of the readout timing. In other words, the write address is normally 16H ahead of the read address, as shown in Fig. 4-4-10, but in the variable speed play, it may advance by a further 16H and catch up with the read address or, conversely, it may be delayed and the read address may catch up with the write address. At times like these, the picture will shift by 32H. In order to safeguard against this, the address which has caught up is returned to 1H before when either the write or read address has caught up with the other.

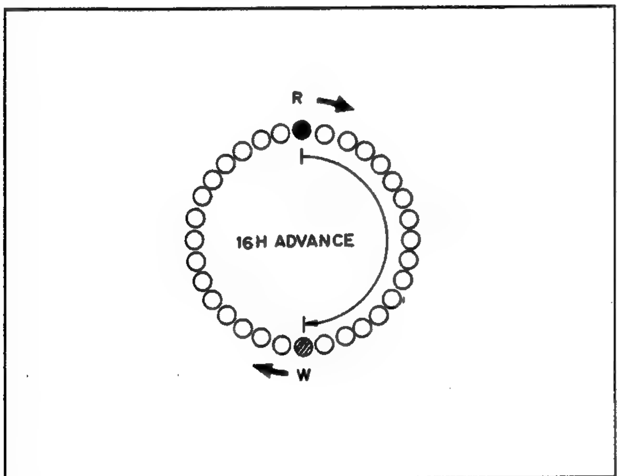


Fig. 4-4-10. Write/Read Phase

ICJ15 serves to judge whether the write address or read address has caught up with the other. Fig. 4-4-11 is a timing chart. When, as shown in the figure, the write address is behind the read address, the comparator ICH13 output is set low after the read address, it is latched at the timing of the trailing edge of the R ZERO signal and pin 9/ICJ15 is set low. In this case, the U/D (up/down) input of the ICG14 and H15 read address counter is set low and the read address is returned to 1 before. Conversely, when the write address is ahead of the read address, the ICH13 output is set low before the read address, it is latched at the timing of the leading edge of the R ZERO signal and pin 5/ICJ15 is set low. The U/D input of the write address counter is set low and the write address is returned to 1 before.

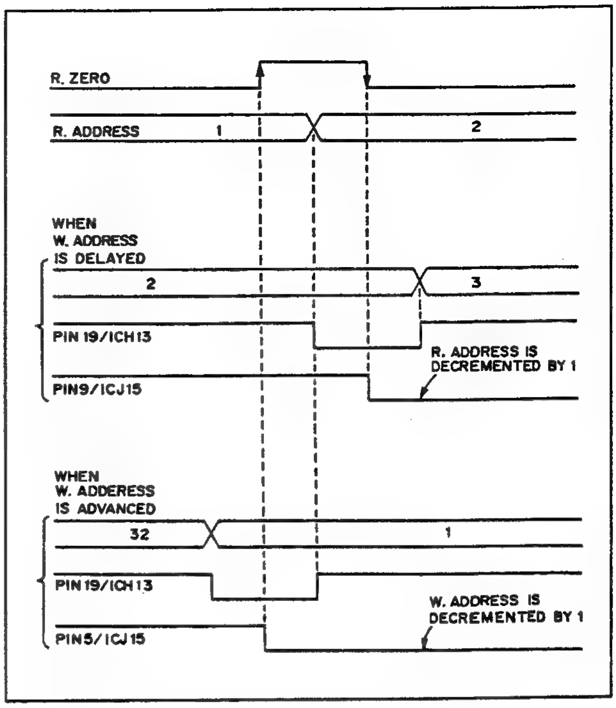


Fig. 4-4-11. Jump Control Timing (CK-27)

The V lock operation is now outlined. This determines the V phase of the TBC output picture, and 16-line locking applies with the BVH-3000PS/3100PS. The 16-line locking means that the 16-line write address of the playback signal is latched at the SEL PB V timing and then loaded at the SEL REF V timing into the read address corresponding to 16 lines of the reference signal.

ICJ1 is the SEL· REF V signal selector which exercises control in two different ways. One way is V locking in the zero advance state which means that the vertical phase is delayed by 4H when the PB signal (including EE) is not in advance of the reference signal. The second way is used for vertically shifting the picture for the V SHIFT mode and Y ADD mode during DT playback. 0, −1H and +1H control is exercised by the RD CONT 1 and RD CONT 2 signals sent from the PR board.

RD CONT 2	RD CONT 1	DELAY
0	0	0H
0	1	−1H
1	0	+1H
1	1	0H

ICK2 is the SEL PB V signal selector. The PB V signal is mostly correct and the DT V signal is in its correct phase during ×1 speed playback (NOR mode) and during DT playback, which means that the DT V (rise) signal is selected in the EE or NOR DT mode and that the pulse created from the REF VD signal is selected during bidirex playback since the DT V signal cannot be relied upon.
ICK3 controls the freeze memory V phase. As with ICJ1, it is controlled by the RD CONT 1 and RD CONT 2 signals. This operation is coupled with Y ADD on/off and the same picture quality is achieved in the DT still picture and freeze modes.

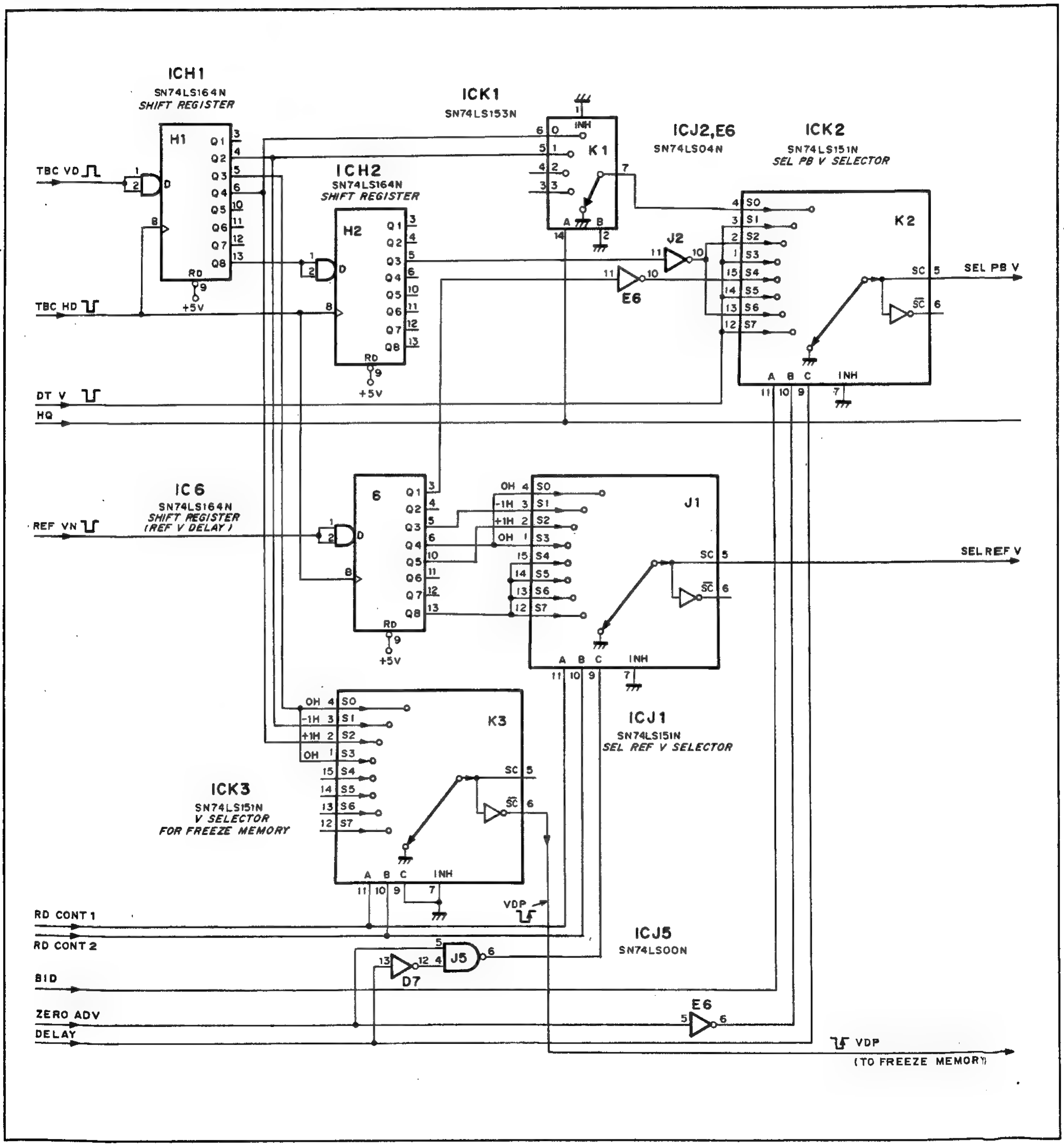


Fig. 4-4-12. V Lock Timing Signal Generator (CK-27)

(5) Freeze memory (CK-27 board)

The data whose time base error has been removed in the main memory are sent to the main signal line circuit and freeze memory circuit.
ICD2 and D5 are a 1-8-1 serial-parallel-serial (S-P-S) converter. Sixteen MB81464 64k×4 DRAMs are used for the memory to store the data of one field. One line is configured with 1135 samples but because of its memory size the freeze memory stores only 1024 samples. The remaining 111 samples (6.26 μ sec) are allocated to part of the blanking period and they are replaced when output from TBC. In the case of the SECAM signal, the start of the data writing into the memory is before the burst signal and this burst signal is also stored. In the case of the PAL signal, the start of the writing is after the burst signal.

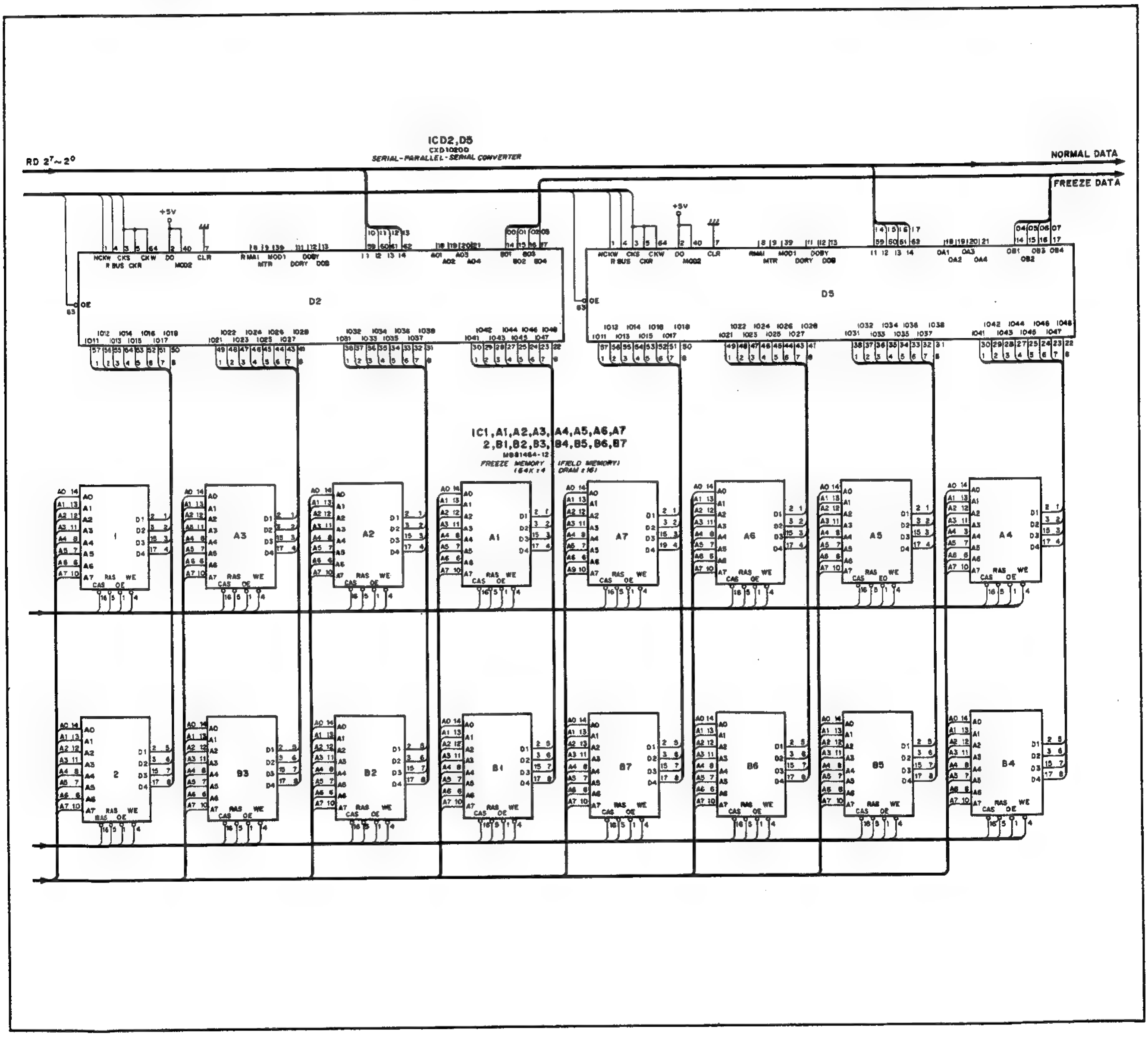


Fig. 4-4-13. Freeze Memory (CK-27)

ICD8, D9 and D10 generate the address within 1 line and this becomes the lower 8-bit address. ICC10 (or ICC8, C9 and C10 with a CK-27 board bearing the -11 suffix) generates the line address and this becomes the upper 8-bit address. ICB9 and B10 configure the RAS/CAS address selector of the DRAM. In order to obviate the need for DRAM refreshing, the lower address is set to RAS and the upper address to CAS.

The reason why the FREEZE signal is input to the D preset pin of address generation counter ICD8 is so that the data will be read out 1 address earlier and so that the delay in the freeze memory output will be reduced. This operation is the same as that for the main memory in that during write operations the data are written not from address 0 but from address 1.

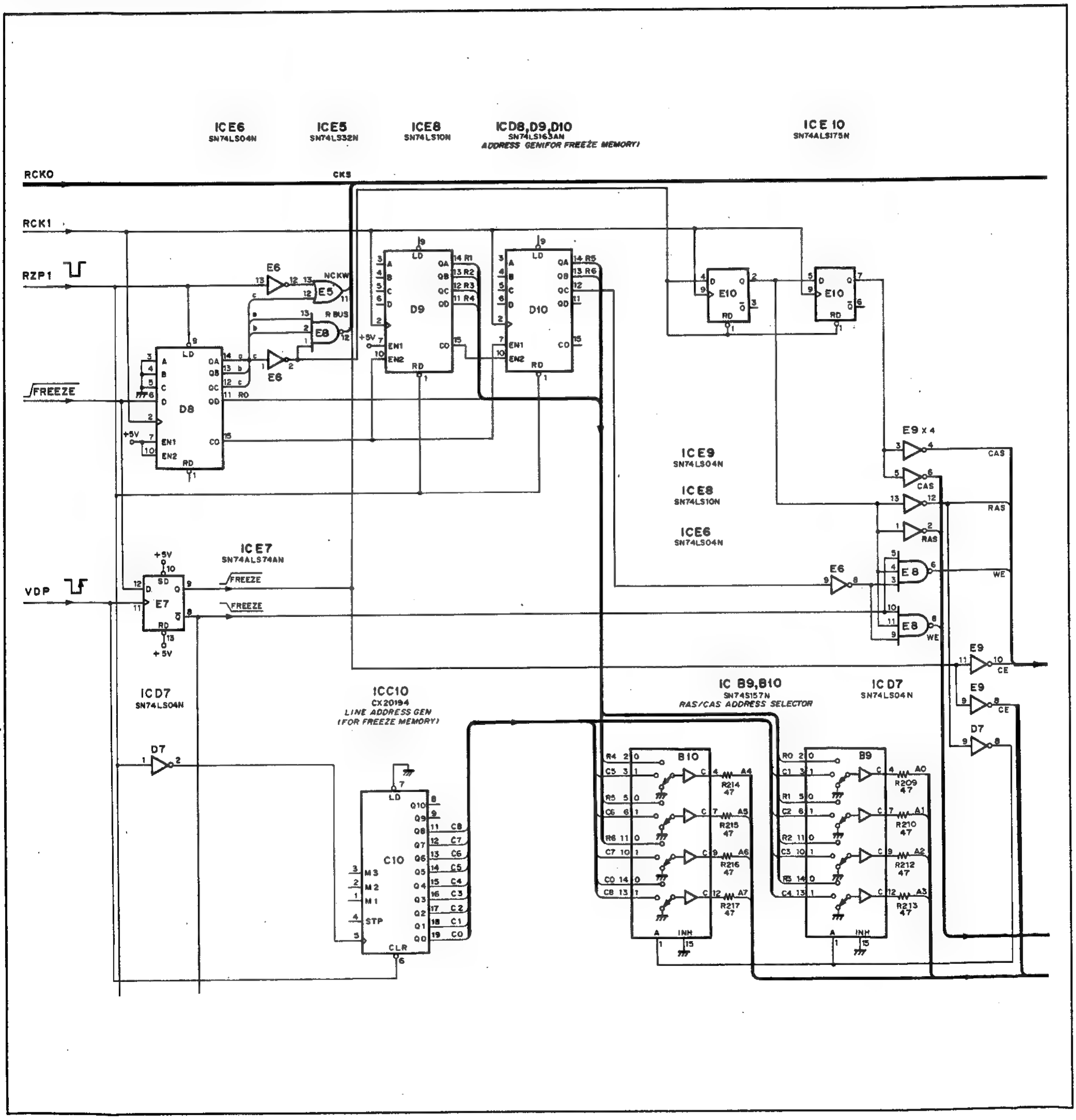


Fig. 4-4-14. Freeze Memory Address Generator (CK-27)

(6) Y DO, C DO, W N/I and W O/E decoder (CK-27 board)

Either the normal data or the freeze data are selected by ICF5 and F6. ICF8 and F7 provide the normal data with a 7-clock pulse delay so that the data will be matched with the delay in the freeze memory.
After having passed through the NORMAL/FREEZE selector, the 8-bit data sent to selector IC102 and 103 which determines whether they are to be delayed by 1H in ICF4 (μ PD41102C) or whether they are to bypass this IC. In the normal playback mode, the 1H delayed data are selected by the RD CONT 3 signal when there is mismatching in the write side and read side odd field/even field.
The Y DO pulse inserted as FFH is decoded by the ICE4 NAND gate, latched by ICG2 and output to the PR board. Pin 4 of ICG2 is a guard which prevents an incorrect Y DO pulse from being output due to a data error in the vicinity of the W ZERO signal. The C DO pulse has been inserted in the section at the start of each line of the data 2^2 and so it is decoded by the signal delayed from the W ZERO signal and output to the PR board.
The 8-bit data selected by IC102 and 103 are 1H delayed by IC101, latched by ICF1 and then output to the PR board. The 1H delay provided by IC101 is supplied for SECAM dropout processing. If there are any dropouts in the Y signal in the case of the SECAM signal, the chroma signal of the whole line is replaced with the chroma signal in the previous line. Thus, the read data are 1H delayed by IC101, the Y DO signal is detected from the data prior to the delay and this is made the C DO signal.
The W N/I and W O/E signals, which were inserted into data 2^1 and 2^0, are similarly decoded and output to the PR board.

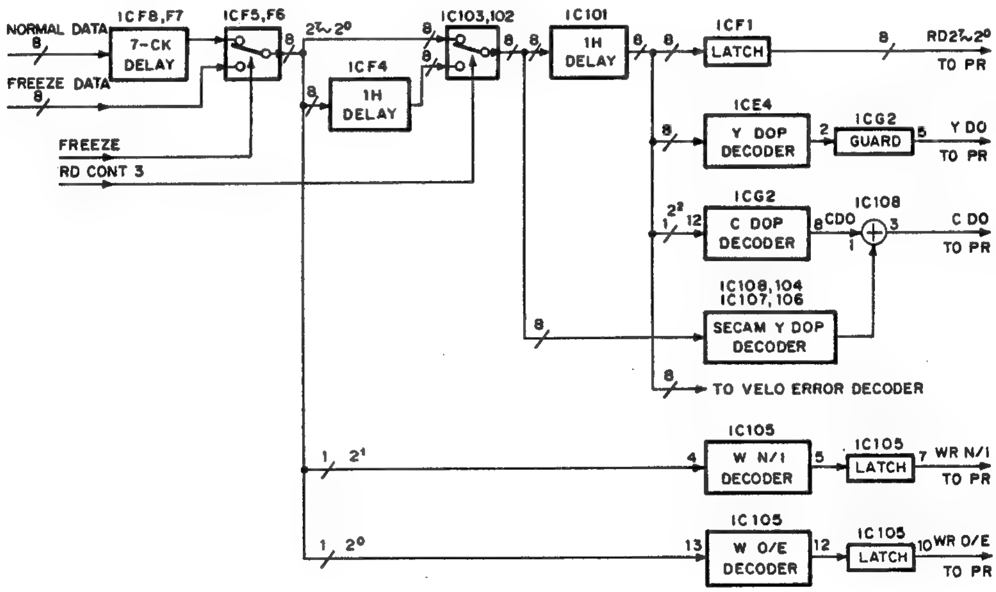


Fig. 4-4-15. Y DO, C DO, W N/I and W O/E Decoder (CK-27)

(7) Velocity error decoder (CK-27 board)

The velocity error inserted into the main signal line sync section is decoded by ICE3 and after its timing is adjusted by ICE2, it is D/A converted by ICE1 and output as analog data.
Since the velocity error data inserted into the video data are delayed 2H behind the video data, they are read out 2H ahead by this decoder.

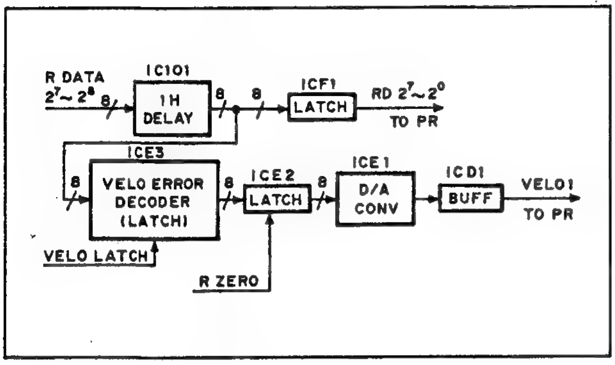


Fig. 4-4-16. Velocity Error Decoder (CK-27)

4-4-3. Write Clock Generator (CK-27 Board)

The 4Fsc write clock signal of the PAL signal is generated by the APC based on the burst signal which is taken out from the PB CHROMA signal and on the 4Fsc signal which is generated by the AFC from the PB SYNC signal.
In the case of the SECAM signal, the 1135FH write clock signal is generated by the AFC and APC with the PB SYNC signal serving as the reference.

(1) PH (PAL H) generator (CK-27 board)

The purpose of this circuit is 3-fold: (1) in the case PAL signals, to remove the PAL offset from the H pulse period so that the AFC frequency locked to the horizontal sync is not 1135FH but 1135FH + 100 Hz, (2) to identify any pulses with a width below 3.6 μ sec from the PB SYNC signal as noise and to remove this noise, and (3) to reduce the burden placed on the W ZERO loop in the color mode during variable speed playback and to reduce the range which must be tracked.
Sawtooth waveforms with a 1V/μ sec ramp are generated by C40, Q10, Q9 and ICL19 from the PB SYNC signal fall timing. The TAPE SPEED signal (a tape speed of ±50 times normal tape speed is equivalent to ±4.5V with the TAPE SPEED signal) which is supplied to the Q9 and ICL19 constant current source serves to control the current in accordance with the changes in the PB SYNC pulse width and to make the amplitude of the TP8 sawtooth waves constant. During variable speed playback, this has the effect of eliminating the same amount of noise as that during normal speed playback and of reducing the burden placed on the W ZERO loop.
The sawtooth waves generated in this way are sliced by DC 3.6V (TP9) in the ICK19 comparator. As a result, PB SYNC pulses below 3.6 μ sec are eliminated.
In the case of PAL signals, the PB CF adjustment voltage and V rate sawtooth waves are added to the slice voltage of the comparator in order to eliminate the PAL offset from the H pulse period. The value of the PB CF adjustment voltage is based on the PRESET (DC 0V), LOCAL (RV9) or remote control setting. It is selected on the [S88. PB CF DET MODE] select menu. ICM21 is an integrator which generates the V rate sawtooth waves by discharging the integrating capacitor with the V pulses. By adding the sawtooth waves generated by ICM21 to the slice voltage, the leading edge phase of the H pulse in the comparator output is modulated and the PAL offset is eliminated from the H pulse period.
In the case of SECAM signals, the integrating capacitor is shorted and ICM21 outputs a constant voltage.
The comparator output is supplied to the ICG19 D-type flip-flop. The PB SYNC signal guarded by the DO pulse is supplied to the ICG19 clear pin and ICG19 removes the dummy sync which is present in the slow bidirex mode. The leading edge of the ICG19 output is the reference timing of the latter stage circuitry and its trailing edge is reset by the trailing edge of the PB SYNC signal. The signal which is output from ICG19 is known as the PH (PAL H) signal.

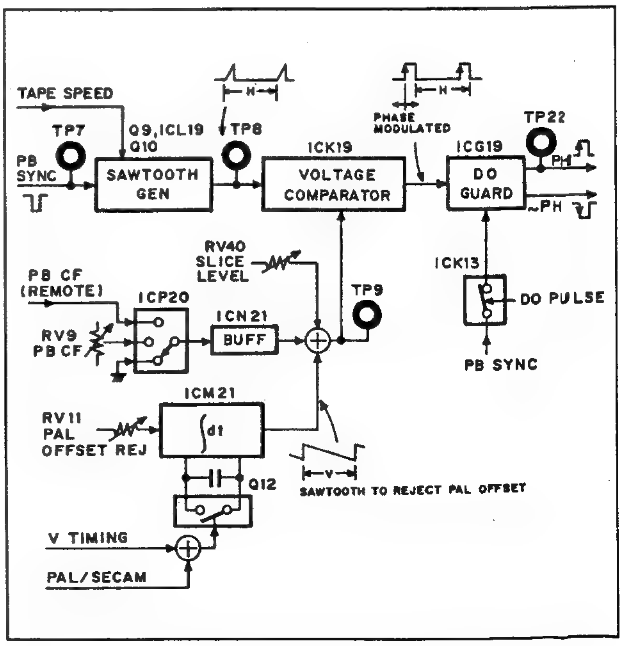


Fig. 4-4-17. PH Generator (CK-27)

(2) SELECT H circuit (CK-27 board)

This circuit focuses on the periodicity of the sync signals, it removes as noise the discontinuous pulses among the PH pulses (PB H signal) which is output from the PH generator circuit, and it prevents the AFC operation from being disturbed by noise. Conversely, in the fast bidirex mode (more than ±8 times normal tape speed), this circuit is bypassed so that as many PB SYNC signals as possible are obtained even if the AFC is disturbed. Fig. 4-4-18 is the SELECT H circuit block diagram and Fig. 4-4-19 is its timing chart. A pulse with a width of approximately 42 μ sec is generated by the ICN11 monostable multivibrator from the fall of the ~PH pulse, and a pulse with a width of approximately 21 μ sec is generated by ICN10 (pin 13) from its fall. A 0.8 μ sec pulse is created by ICN10 pin 5 from the fall of the ICN10 pin 13 output, and the phases of the fall of this pulse and the ~PH pulse fall are compared by ICM8. The widths of the pulses generated by these two monostable multivibrators (ICN11, N10) are controlled by the ICM8 output so that the ICM13 pin 5 pulse will approach the PH pulse which is to arrive next. Only the PH pulses appearing within the ICM13 pin 5 pulse range are output as the SELECT H signal. The ICM13 pin 5 pulse width is about 1.6 μ sec and any pulses with a width exceeding ±0.8 μ sec from periodic signals are not output as the SELECT H signal.

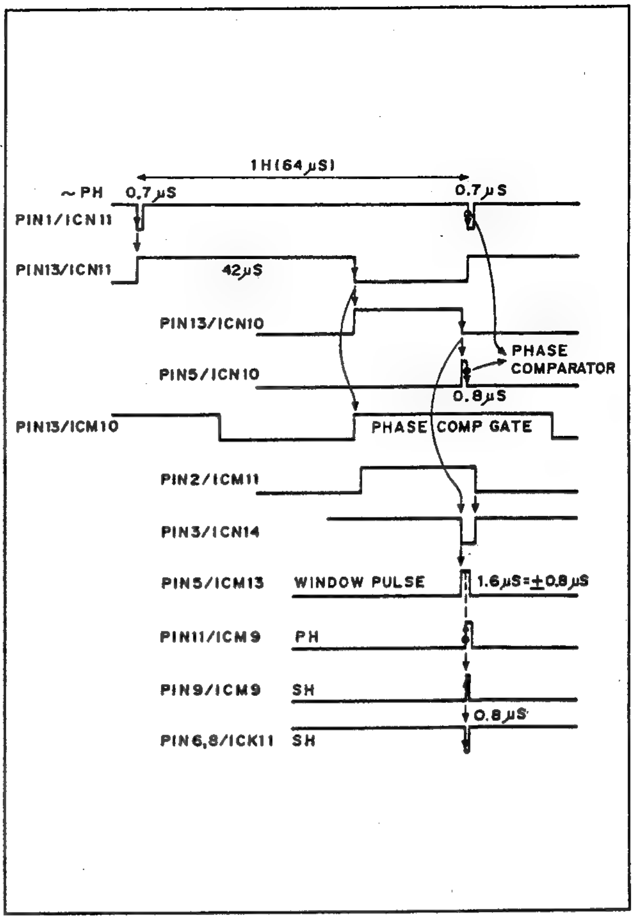


Fig. 4-4-19. SELECT H Timing Chart (CK-27)

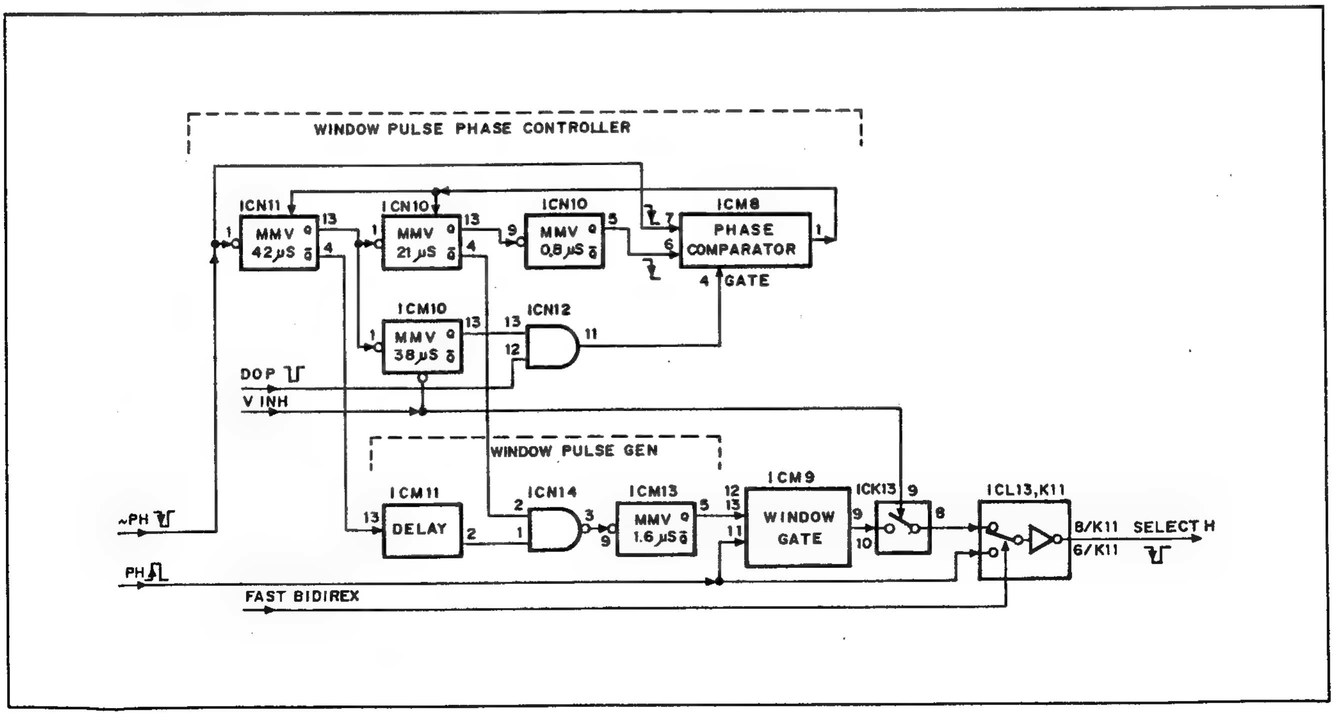


Fig. 4-4-18. SELECT H Generator (CK-27)

(3) AFC (CK-27 board)

The AFC circuit is driven by a pulse which has a width of approximately 450 nsec and which is created from the SELECT H signal. As shown in Fig. 4-4-20, it is composed of a closed loop (ICN14 →M19→M18→P18→P13→P7→P12→N14) and an open loop based on the TAPE SPEED signal supplied to ICM18.
In order to accelerate the AFC pull-in during the shuttle mode or when skew has arisen, this AFC resets the counter under any deviation from the window of approximately ±220 nsec. The range for the change in the VCO frequency is from 8 to 26 MHz. The VCO is controlled so that it oscillates at a frequency which is equivalent to 1135 times that of the SELECT H signal. With a PAL system, the phase of the SELECT H signal is modulated by the PH generator circuit and so the VCO center frequency is 1135FH + 100 Hz.
Fig. 4-4-21 is a timing chart of the various sections. The pulse, which has a width of approximately 400 nsec and which is created by monostable multivibrator ICN11 from the SELECT H signal, is supplied to ICN14 and ICM19 which configure a phase comparator. In order that the TP11 (ICP12 pin 14) fall timing will be locked at the intermediate point of the 450 nsec pulse, VCO ICP18 is controlled by the ICM19 error voltage, and the VCO output drives counter ICP7. When the SELECT H signal (ICN11 pin 5) is supplied within the range of the window created by ICP5 (pins 1, 2 and 3), the counter is not reset ; when it deviates from the window, ICM9 pin 5 is set high, the reset pulse is generated at ICN14 pin 11 and counter ICP7 is reset. ICP7 is reset not to zero but to "11." As a result, the next window after resetting appears at the proper position.

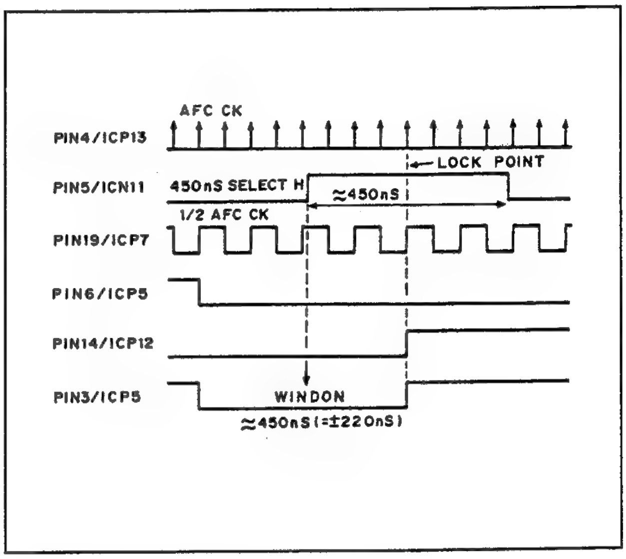


Fig. 4-4-21. AFC Window (CK-27)

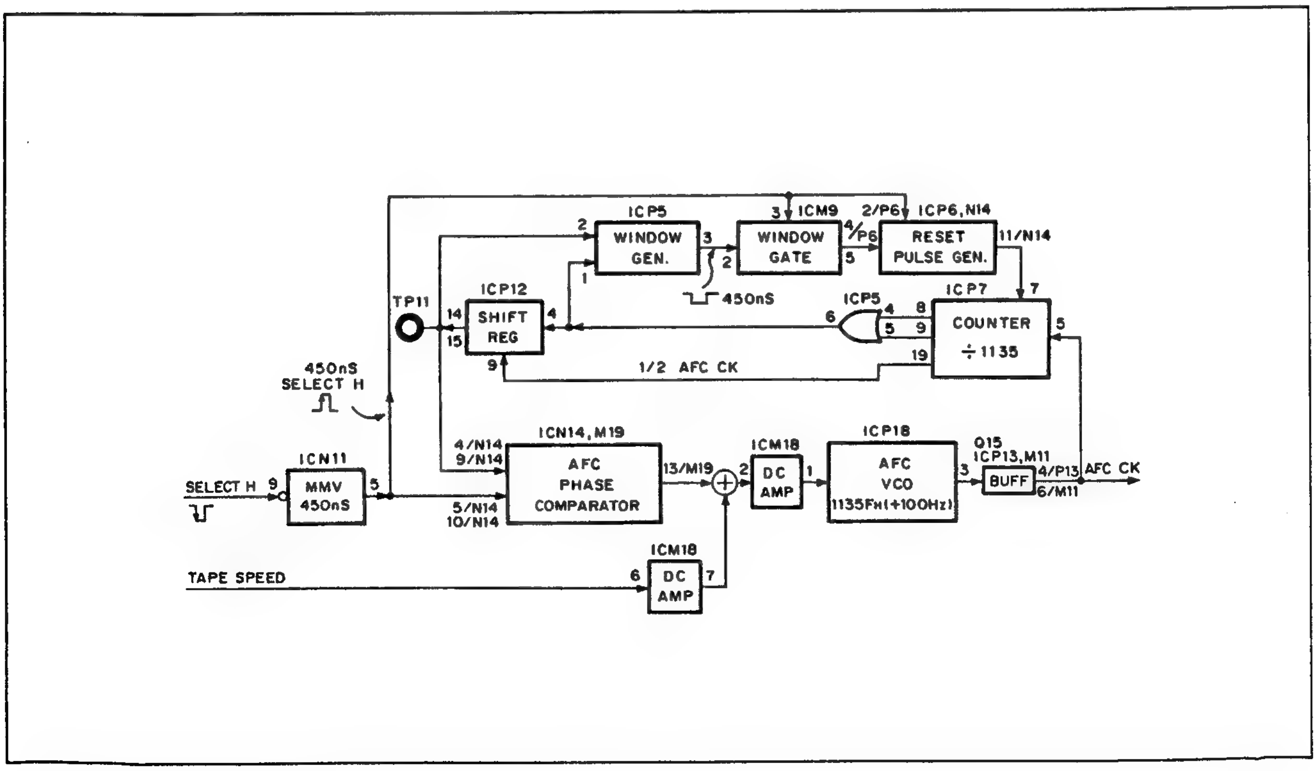


Fig. 4-4-20. AFC (CK-27)

(4) Burst signal detector (CK-27 board)

This circuit takes out the burst signal from the PB CHROMA signal. The bandpass filter (FL1 and LV1) with its center frequency of 4.43 MHz takes out the chroma signal from the PB CHROMA signal which contains the Y components and which has been supplied from the VO-16 board. Next, the burst signal is separated from the chroma signal by ICK21. The TTL level burst signal is then output from ICK21.

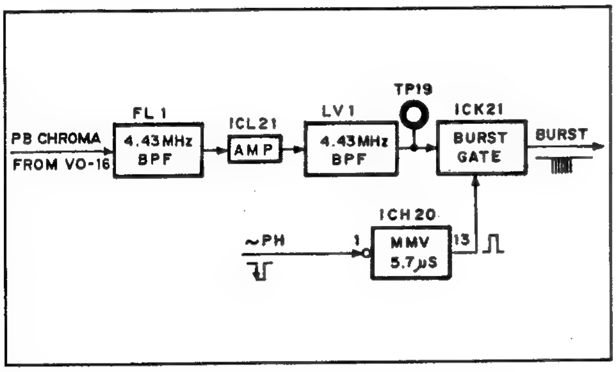


Fig. 4-4-22. Burst Signal Detector (CK-27)

(5) APC start pulse generator (CK-27 board)

This circuit serves to take out one wave of the burst signal from the burst signal which has been converted to the TLL level in the burst detector and to trigger monostable multivibrator ICG18 (pin 10). Which wave is taken out depends on the pulse width of the reset signal (TP4) of the ICG21 shift register. When the TP4 pulse width has been adjusted to 2.7 μ sec, the sixth wave is taken out. The ICG18 (pin 5), K13 and E21 loop is configured so that the width of the monostable multivibrator output pulse is aligned accurately with one burst wave. The pulse generated here is the start pulse for starting and stopping the oscillation of the APC VCO.

ICG18 (pin 13) and G19 detect the continuity of the one burst wave and when it is discontinuous, the start pulse is not allowed to be output. The start pulse is created from the one burst wave only in the PAL color mode. The burst signal cannot be detected in the SECAM, black-and-white and fast bidirex modes and so, in this case, the pulse created from the ~PH signal by ICH21 is supplied to ICG18 (pin 9) to generate the start pulse.

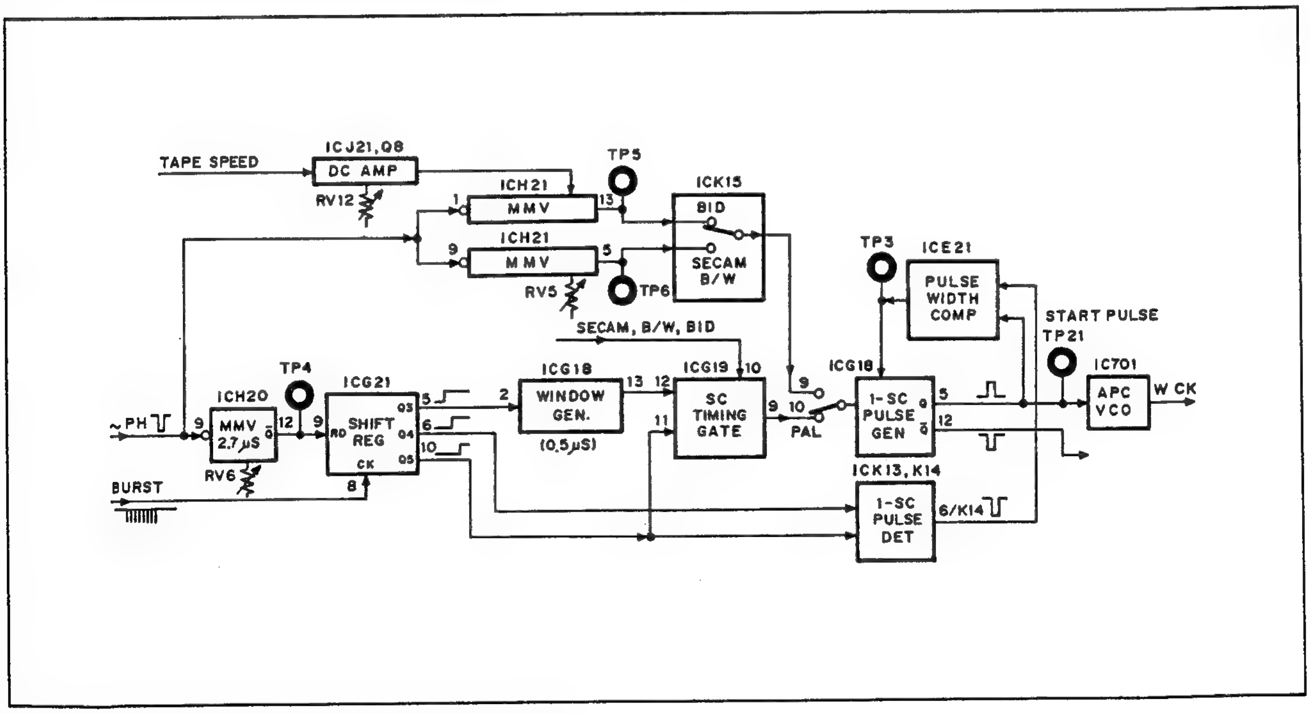


Fig. 4-4-23. APC Start Pulse Generator (CK-27)

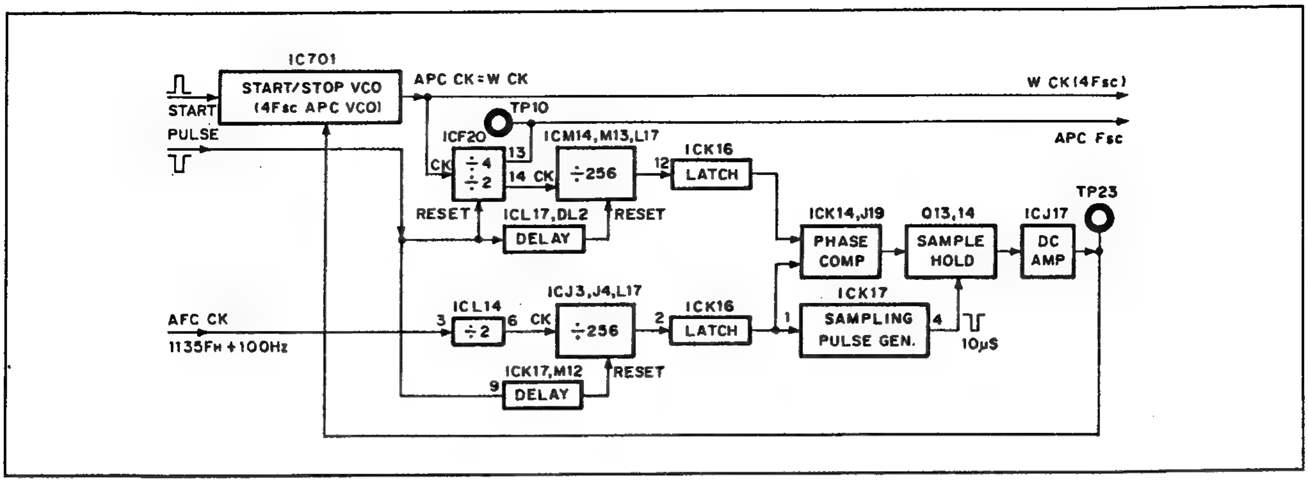


Fig. 4-4-24. APC and AFC Locking (CK-27)

(6) AFC and APC locking (CK-27 board)

The APC start/stop VCO oscillates at a frequency of 4Fsc and its phase is locked to the phase of the burst signal by the start pulse.
By means of comparison with the AFC VCO frequency, the APC VCO frequency is controlled so that it is matched with the AFC VCO frequency. The range across which the APC VCO frequency can be varied extends from 8 MHz to 26 MHz. The APC CK pulse output from the APC VCO is the W CK (write clock) pulse.
The frequency of the 4Fsc APC CK signal is first halved by ICF20 and then the resulting signal enters the 256 counter which is composed of ICM14, M13 and L17. When this counter executes a 256 count, the counting will stop until the counter is next reset. The reset pulse is generated from the APC start pulse and so this means that the counter output is an H rate pulse with a duty ratio of approximately 45%.
An H rate pulse with a duty of 45% is also simultaneously generated from the AFC CK pulse. By comparing the phases of the two pulses in ICK14 and J19 and by controlling the APC VCO with the resulting error voltage, the APC VCO frequency is matched with the AFC VCO frequency.

(7) W O/E detector and velocity error detector (CK-27 board)

The W Fsc signal is locked to the burst signal line by line, and the PAL system line O/E is detected by latching the W Fsc signal by the burst signal of the next line.
The velocity error voltage is created by using a charge pump to T/V convert the difference in the phases of the W Fsc signal and of the burst signal in the following line. The phase difference is detected by ICE19 (pins 11 and 12) and F18 (pins 6 and 3) and converted into a voltage by ICD19. The velocity error voltage is reset line by line using Q4. The level of this voltage is then shifted and inserted into the H sync section of the video signal prior to A/D conversion.

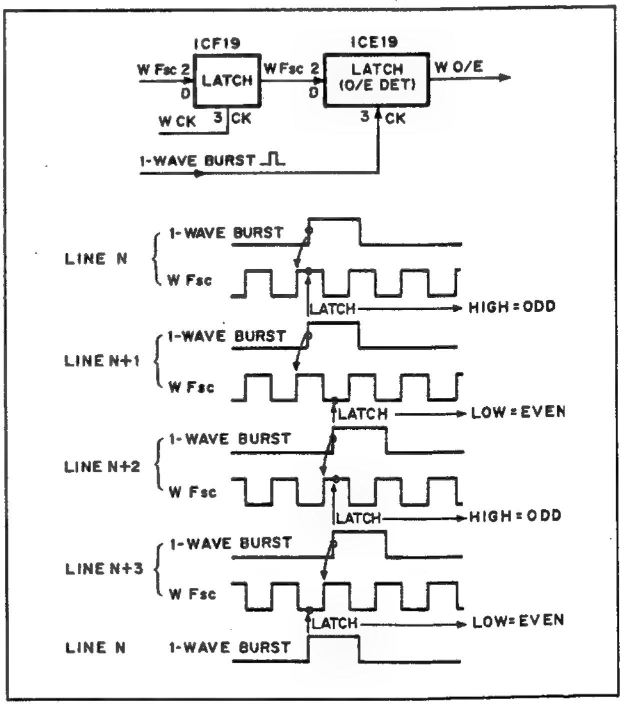


Fig. 4-4-25. W O/E Detector (CK-27)

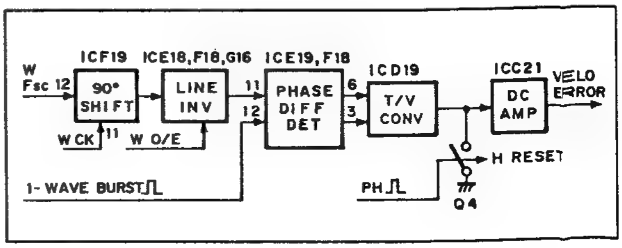


Fig. 4-4-26. Velocity Error Detector (CK-27)

(8) W ZERO generator (CK-27)

It is vital that the W ZERO (write zero) signal, which is the memory write start signal, be output at a high degree of stability and reproducibility with the same phase no matter what happens to the SC-H phase.
The PH pulse phase is compared by IC11 with the phase of the H pulse output from the AFC, and the delay in the PH pulse is controlled by the resulting error voltage. The time constant of the phase comparator is configured with a large-capacity capacitor (C109) and so the ICN9 and IC11 circuit functions as a kind of low-pass filter which does not track high phase fluctuations.
After its noise components have been filtered out by the low-pass filter, the H pulse now triggers the variable-width monostable multivibrator (ICP9) in the W ZERO loop. The output of this multivibrator is first latched by SC** (W Fsc which has been inverted by W N/I) and then supplied to the phase comparator composed of ICM5 and N8. The phase error (TP27) is fed back to the variable-width monostable multivibrator (ICP9) to control the pulse width of ICP9. R172 is added to pin 10 so that the pulse width supplied to pin 7 of charge pump ICN8 is made one-half of the width of the pulse supplied to pin 5.
The ICN6 comparator determines the tracking range of the W ZERO loop. This range is approximately ±270° . When the error voltage resulting from phase comparison exceeds the ICN6 threshold voltage, ICN8 is reset and returned to the center voltage.
Comparator ICN5 and M7 detect that the W ZERO loop is in the center of the locking range and they cause the PB CF LED to light up.
The output of variable - width monostable multivibrator ICP9 pin 4 is first latched by ICM6 pin 6, and then it resets ICP15 which is counting the W CK pulses. The ICP15 output is the W ZERO signal. The W ZERO loop circuit enables a timing signal which maintains the phase relationship with W Fsc to be provided no matter what the SC-H phase of the signal supplied may be, and it enables ICP15 to count the W CK pulses correctly. This counter is designed to turn at the 1135 count so that the W ZERO pulses are not missing.
In the bidirex, SECAM or black-and-white mode, the H pulse created from the PH pulses by the APC start pulse circuit serves as the reset pulse for ICP15.

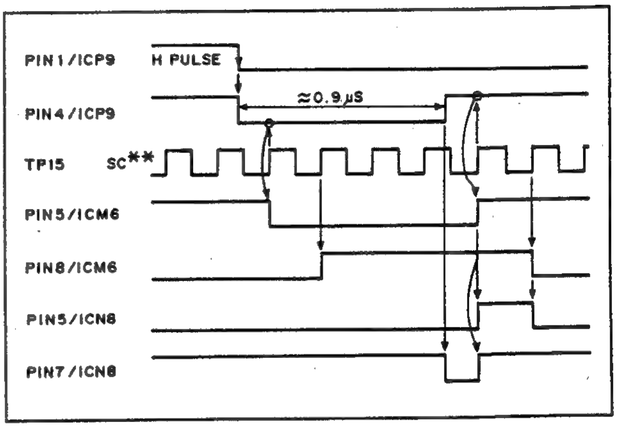


Fig. 4-4-28. W ZERO Loop (CK-27)

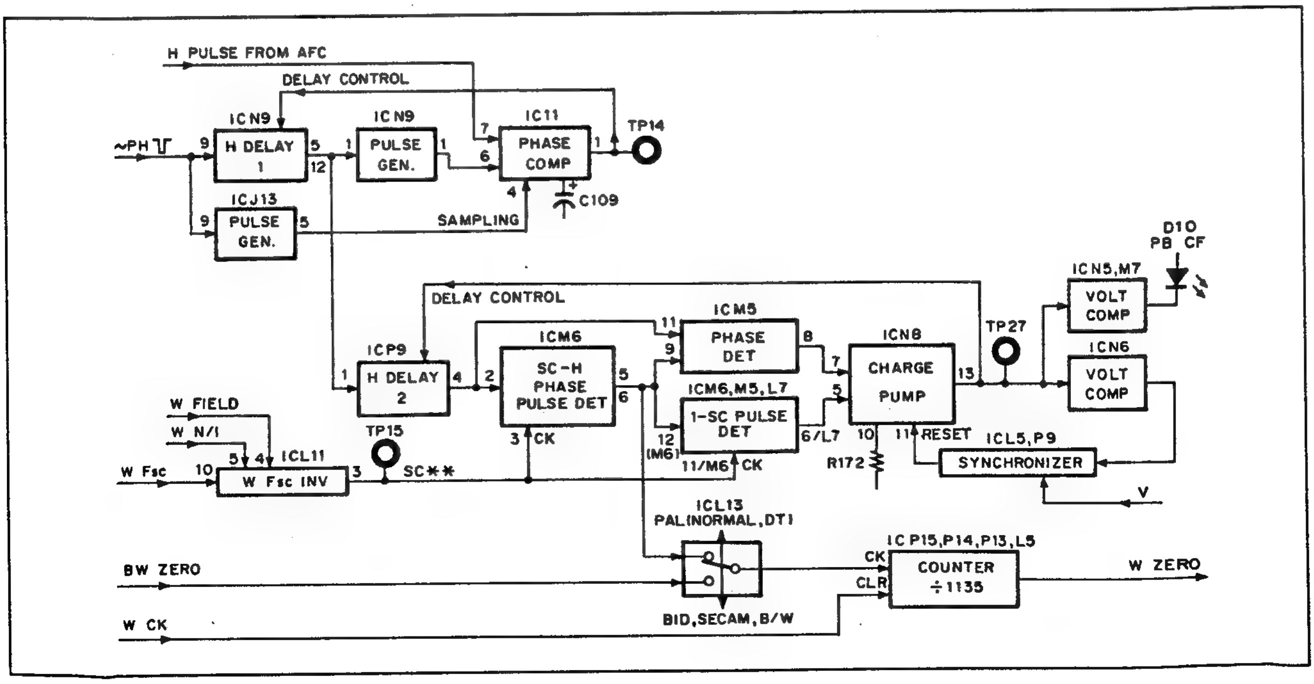


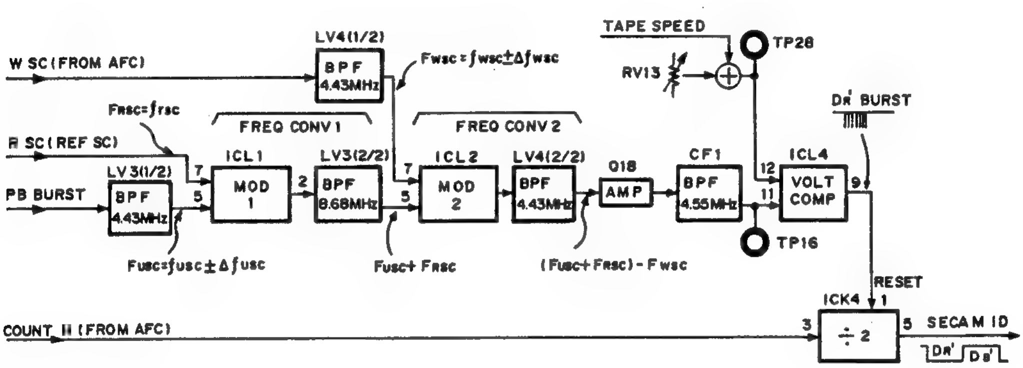
Fig. 4-4-27. W ZERO Generator (CK-27)

(9) SECAM DR' /DB' line ID detector (CK-27 board)

DR' line/DB' line detection makes use of the fact that the frequency of the burst (unmodulated subcarrier) signal which is added to the head of each line of the SECAM signal is switched every horizontal line. The DR' line burst signal frequency is 4.406 MHz and that of the DB' line is 4.250 MHz.

On a CK-27 circuit board which has the number 1-621-749-11 or -12, the effects of the tape speed are first removed from the burst signal frequency using a double-heterodyne system and then the difference in the frequency is converted into a voltage difference by the filter to detect the DR' line.

On a CK-27 circuit board which has the number 1-621-749-13 or higher, the difference in the DR' and DB' line burst signal frequencies is converted into a voltage difference by the FM demodulator and the DR' and DB' lines are detected.



Freq of PB BURST: $F_{USC} = f_{USC} \pm \Delta f_{USC}$ (f_{USC} ; CENTER FREQUENCY, Δf_{USC} ; FREQUENCY DEVIATION)

Freq of REF SC: $F_{RSC} = f_{RSC}$

Freq of W SC: $F_{WSC} = f_{WSC} \pm \Delta f_{WSC}$ (f_{WSC} ; CENTER FREQUENCY, Δf_{WSC} ; FREQUENCY DEVIATION)

Freq of F.CONV 1 OUT: $F_{USC} + F_{RSC} = (f_{USC} + f_{RSC}) \pm \Delta f_{USC}$

Freq of F.CONV 2 OUT: $(F_{USC} + F_{RSC}) - F_{WSC}$

$$= (f_{USC} + f_{RSC}) \pm \Delta f_{USC} - (f_{WSC} \pm \Delta f_{WSC})$$
$$= f_{USC} + (f_{RSC} - f_{WSC}) + (\pm \Delta f_{USC}) - (\pm \Delta f_{WSC})$$
$$= f_{USC}$$

Fig. 4-4-29. SECAM DR' /DB' Line ID Detector (CK-27-11/12)

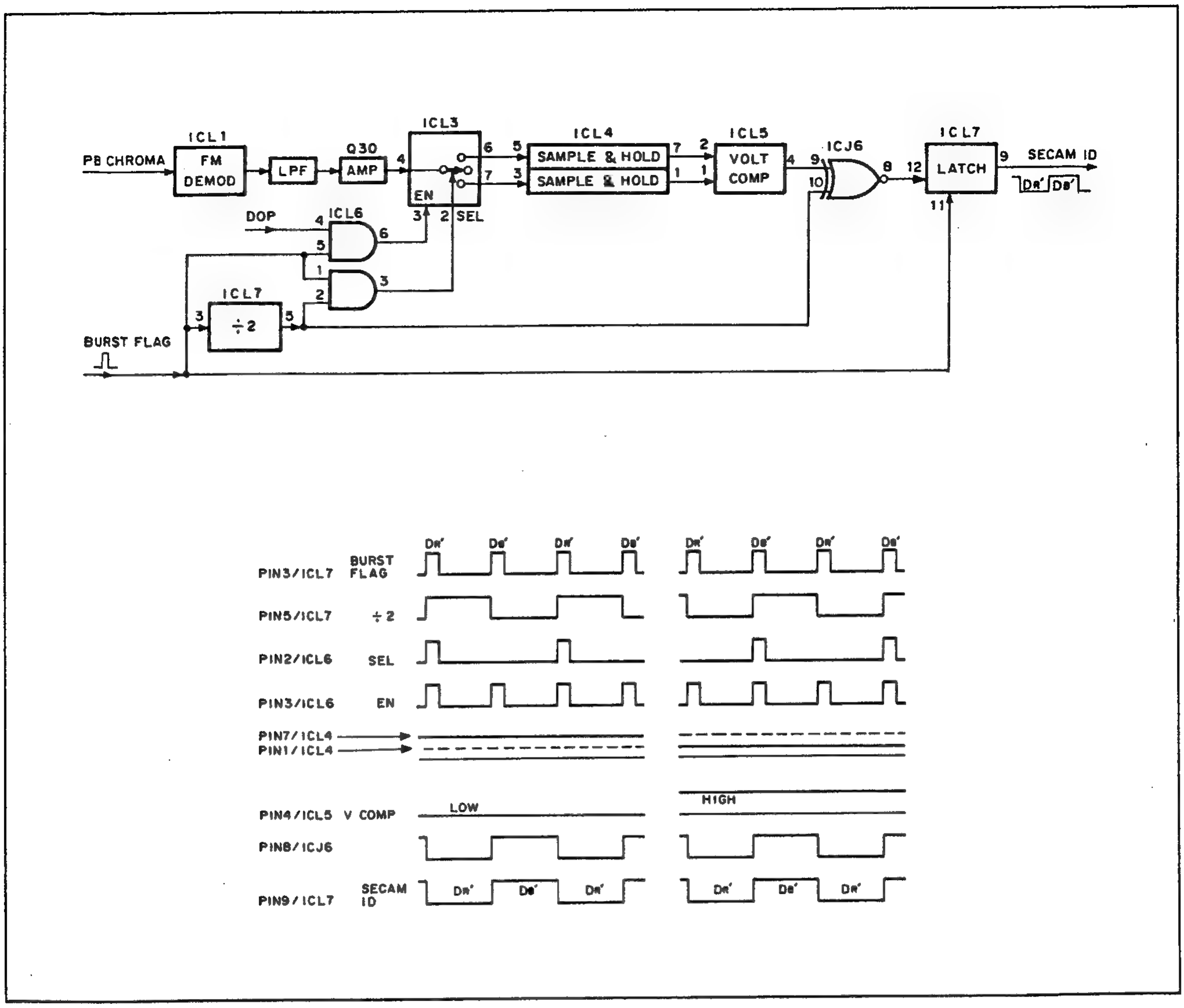


Fig. 4-4-30. SECAM DR' /DB' Line ID Detector (CK-27-13)

(10) W O/E and W N/I generator (CK-27 board)

In the case of the PAL signals, the lines are identified with two types of signals, O/E (odd/even) and N/I (normal/invert), and so a cycle for line identification involves 4 lines. Since a field is composed of 312.5 lines and there is an offset of 3.5H between the tracks on the tape, N/I and O/E are discontinuous when the head jumps to a discontinuous track such as during DT playback. N/I and O/E are therefore corrected by the DT head jump information from the DT control circuit (RD board).
The DT head jump information is supplied to the CK board as the 3-bit parallel data (J STATUS 1, 2 and 3), and it is decoded into the N/I and O/E correction signals at ICK5, H6, K8 (pin 8) and J9 (pin 8).

DT head jump	J STATUS			O/E	N/I
	3	2	1		
3-pitch	0	0	0	INV	
2-pitch	0	0	1		INV
1-pitch	0	1	0	INV	INV
0-pitch	0	1	1		
−1-pitch	1	0	0	INV	
−2-pitch	1	0	1		INV
−3-pitch	1	1	0	INV	INV
not used	1	1	1		

0-pitch jump = normal playback

The output, produced by halving the frequency of the counter (ICK10) signal which uses the COUNT H pulse created by dividing down the frequency of the AFC clock as the clock pulse, is the O/E signal. The ICK10, L8, L9, L10 and G5 loop configures the O/E correction circuit. This circuit has inertia and it functions to prevent O/E from being inverted until the mismatching with the O/E signals provided from the playback burst signal is detected 16 times (16 lines). This is because if O/E is inverted as soon as it has been detected in error, the color will appear on the screen unevenly which makes it hard to see the picture.

Both of the O/E signal (or SECAM ID signal in the case of SECAM signals) detected from the burst signal and the O/E signal produced by halving the frequency of the COUNT H pulse are supplied to the ICL8 exclusive OR circuit. If the O/E signal has been created properly, two O/E signals (ICL8 pins 9 and 10) will have mutually opposing polarities, the ICL8 output (pin 8) will be set high, the ICL9 output (pin 6) will be set low, and the ICL10 error counter will be prohibited from counting. If the O/E signal has not been created properly, the two O/E signals will have the same polarity, the ICL8 output will be set low, and the ICL10 error counter will count the COUNT H pulse. When the counter counts 16 COUNT H pulses, a pulse is output to the CO (carry output) pin. The error counter output is supplied to the ICK10 enable pin and the ICK10 count is stopped once. As a result, the polarity of the W O/E signal is inverted.

The OR signal of the O/E INV signal which has been created from the jump status information and the error counter output signal is supplied to the ICK10 enable pin. When the O/E INV signal is generated from the jump status information, the ICK10 count is stopped regardless of the error counter and the polarity of the W O/E signal is inverted.

The ICL10 error counter is reset with each vertical sync pulse. In the bidirex or SECAM mode, the maximum value of the error counter is changed from 16 to 1 and the O/E signal polarity is inverted with each O/E error.

The W N/I signal is created by halving the frequency of the O/E signal at ICL9 (pins 11 and 9). ICL9 is reset by the output of ICK8 pin 6. The reset pulse is output at the REF 8F and DTV timing and this is the CF reset pulse. As detailed below, the CF reset pulse is generated when the VTR mode is changed.

- BIDIREX

  DT → EE ⇄ PLAY STATUS

  (Servo lock status at ×1 speed)

- In the PLAY STATUS condition,

  CONFI ⇄ $\overline{\text{CONFI}}$

  EDIT PRESET ⇄ $\overline{\text{EDIT PRESET}}$

- When the mode is changed from the no-signal status to the play status
- When the power has been switched on
- When the REF4 signal is disturbed
- When the black-and-white mode has been changed to the color mode

The ICL9 pin 9 output is inverted by ICL8 in accordance with the jump status information of the DT head to form the W N/I signal.

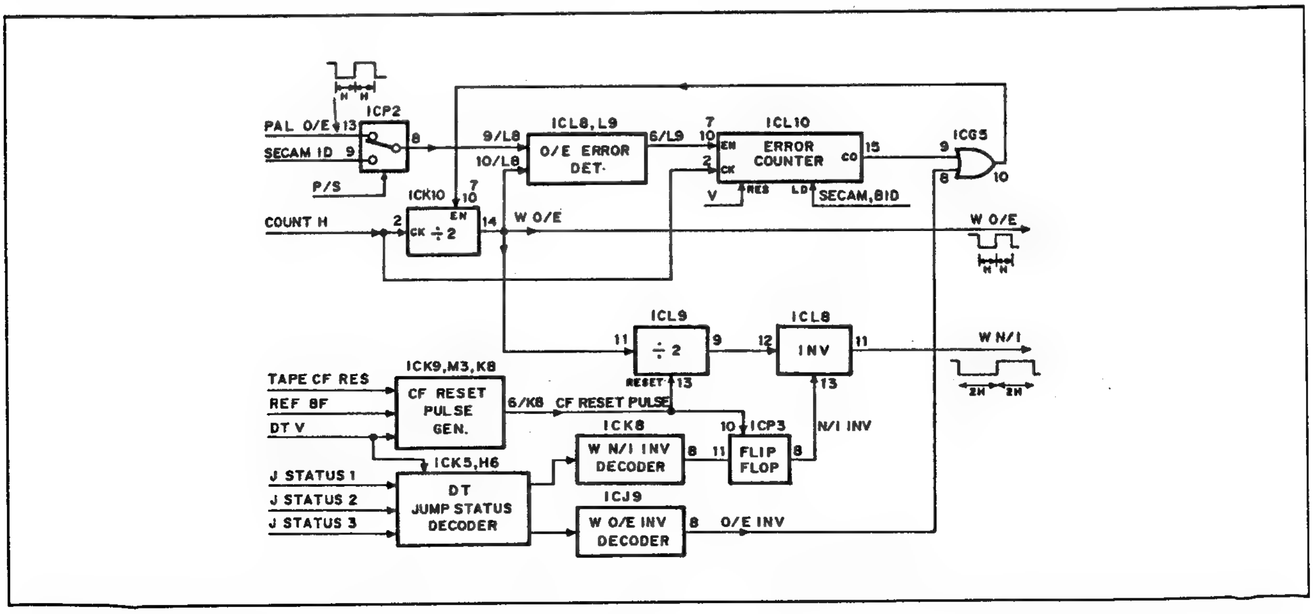


Fig. 4-4-31. W O/E and W N/I Generator (CK-27)

4-4-4. TAPE SC-H Detector (CK-27 Board)

"SC-H" denotes the phase relationship between the sync signal and burst signal. In the case of PAL signals, 8 fields are treated as one cycle for which the sync and burst signals are provided with a phase relationship. The BVH-3000/3100 use LED indication on the front panel to display the SC-H phase and this facilitates SC-H phase control during editing operations. The SC-H phase of the reference video signal is detected on the RD board. The SC-H phase of the playback video signal (or input video signal in the EE mode) is detected by the CK board, A/D converted on the RD board, sent to the front panel by the data bus and displayed by the LEDs.
As with the PH (PAL H) generator, H pulses with a period from which PAL offset has been eliminated are generated by generating sawtooth waves from the PB SYNC signal and slicing these waves with V rate sawtooth waves.
Furthermore, in ICK4, pulses with a width equivalent to the SC-H phase difference are generated by latching the SC* pulse (W Fsc signal whose phase is aligned line by line). This pulse width is converted into a voltage by the ICN17 charge pump and the resulting voltage is sent to the RD board.
ICL16 and L15 serve to narrow the width of the SC* pulse and widen the detection range of the SC-H phase.
In order to reduce the susceptibility to the effects of dropouts and velocity errors, the window comparator composed of ICP16, 301, 302, Q14 and 23 (ICP16, M16, M15, Q24 and 23) removes the SC-H voltage which is not included in the window. The ICN16 low-pass filter eliminates fluctuations from the SC-H voltage.

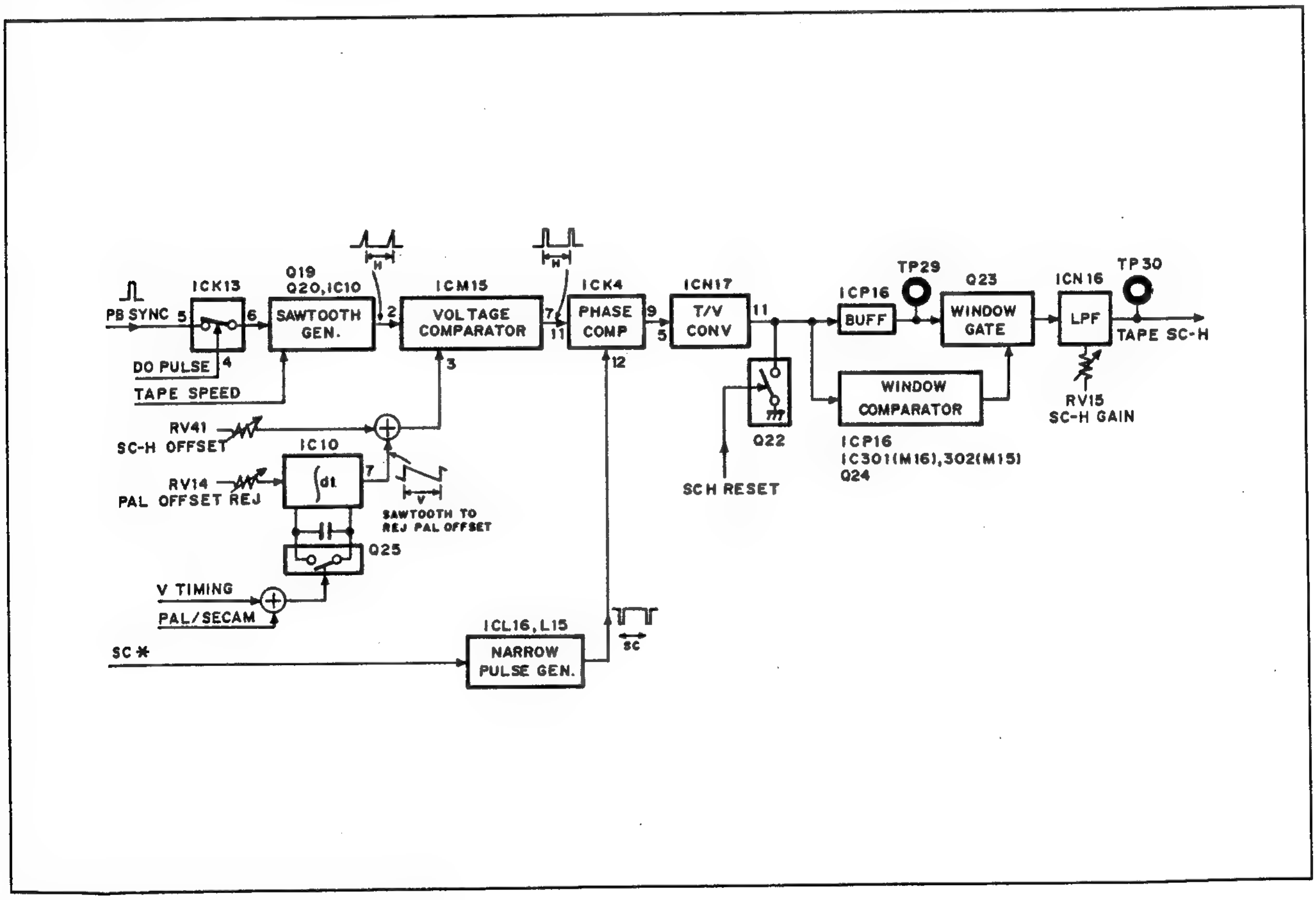


Fig. 4-4-32. TAPE SC-H Detector (CK-27)

4-4-5. CK Board Mode Decoder (CK-27 Board)

Since the switches on the circuit boards have been removed and servicing is performed based on menus, all the mode signals in the BVH-3000/3100 are sent from the SY/SV board by the data bus. The mode decoder circuit serves to decode the signals arriving in the data bus into the mode signals. The CK board functions only to receive the data and because of the low number, the data are decoded by latches.
Shown below are the modes which are decoded by ICN1 and N2.

Pin/IC	Signal	Function
19/N2	PB CF R/L	PB CF adjustment (H : remote ; L : local)
2/N2	ZERO ADV	Zero advance (TBC) (H : other ; L : zero advance)
16/N2	BID	Indicates bidirex mode (H : bidirex ; L : other)
5/N2	PB CF	Indicates PB CF preset (H : other ; L : preset)
15/N2	F.BID	More than ±8 times normal speed (H : fast bidirex ; L : other)
6/N2	B&W	Monochrome (H : B&W ; L : other)
12/N2	DOC OFF	DOC ON/OFF (H : DOC OFF ; L : DOC ON)
9/N2	CF RESET	TAPE CF reset
19/N1	F REW	Indicates fast bidirex in reverse direction (H : other ; L : fast rewind)
2/N1	EE	(H : other ; L : EE)
16/N1	NOT USED	
5/N1	P/S	(H : SECAM ; L : PAL)
15/N1	PLAY STATUS	(H : other ; L : play status)
6/N1	HQ	Indicates HQ PR board (PR-98) (H : HQ ; L : standard)
12/N1	DELAY	1/3V delay with CONF (H : delay ; L : other)
9/N1	FREEZE	Indicates freeze (H : freeze ; L : other)

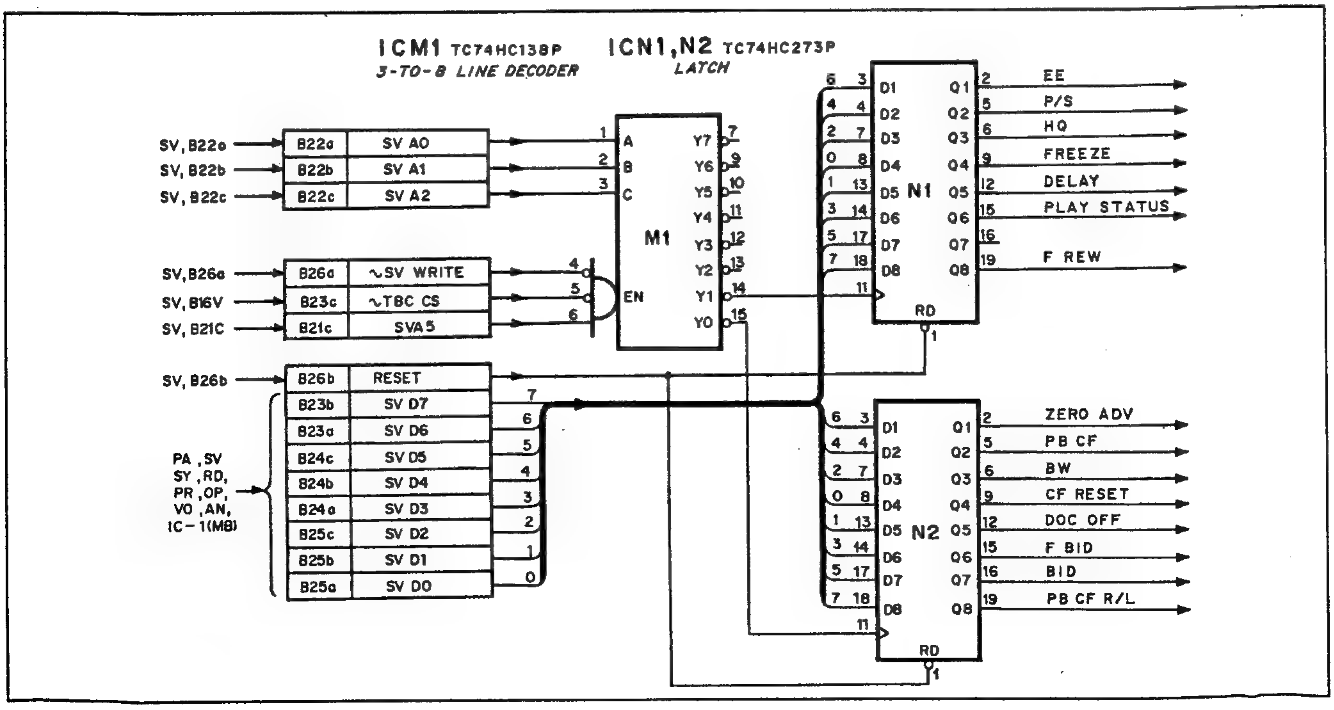


Fig. 4-4-33. Mode Decoder (CK-27)

4-4-6. TBC Reference Signal Generator (RD-7 Board)

The RD-7 board is composed of the TBC reference signal generator, servo reference signal generator and DT control circuit.
The TBC reference signal generator is composed of the four following circuits.

1. **TBC reference video signal selector**
   This circuit selects either the INPUT VIDEO signal or INPUT REF VIDEO signal as the TBC reference signal.
2. **RD CK (read clock) generator**
   This circuit generates the read clock signal which is synchronized with the burst signal in the reference signal. It also provides differential phase compensation and velocity error compensation for the PAL signal.
3. **Sync generator**
   This circuit generates the various signals which are synchronized with the sync signal in the reference signal.
4. **R ZERO (read zero) generator**
   This circuit generates the main memory read timing signals from the H sync signal and from the RD CK signal which has been synchronized with the burst signal.

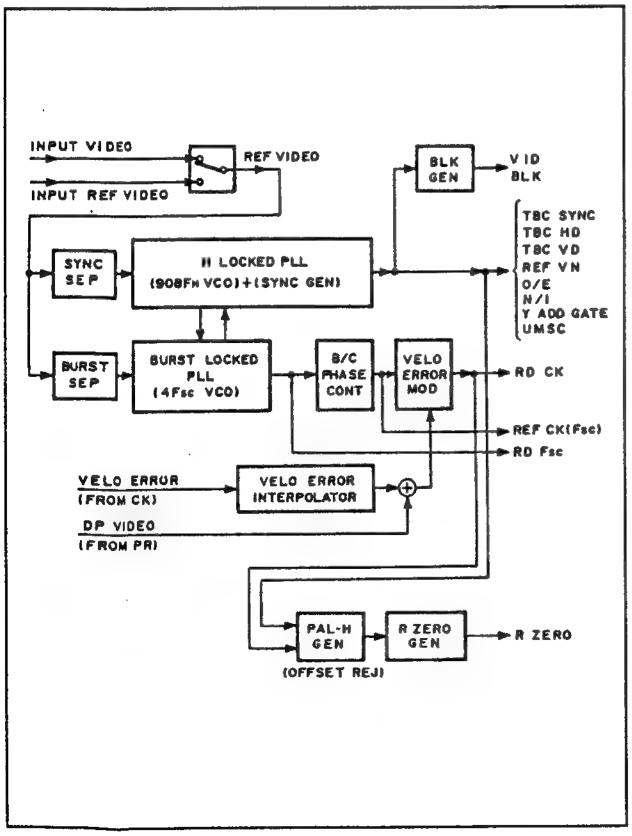


Fig. 4-4-34. Outline of TBC Reference Signal Generator (RD-7)

(1) TBC reference video signal selector (RD-7 board)

This selector circuit functions to select either the INPUT VIDEO signal, which has been supplied from the external source, or the INPUT REF VIDEO signal as the TBC reference signal.
When [EXT REF] is selected on the [S86. TBC REF SELECT] menu, the INPUT REF VIDEO signal is selected ; when [SERVO] is selected, one of the signals designated by the [S40. SERVO REF SELECT] menu shown below is selected.

		S86. TBC REF SELECT: SERVO	S86. TBC REF SELECT: EXT REF
S40. SERVO REF SELECT	EXT REF	INPUT REF VIDEO	INPUT REF VIDEO
	AUTO	Recording: INPUT VIDEO Editing : INPUT VIDEO Others : INPUT REF VIDEO	
	INPUT	INPUT VIDEO	

The video signal supplied to this circuit has a level of 0.5 Vp-p. After the INPUT VIDEO signal or INPUT REF VIDEO signal has been selected by ICF1, it is amplified by ICF1 and F3 to a level of approximately 4.5 Vp-p. The amplified signal is then sent to the reference sync separator and subcarrier generator.

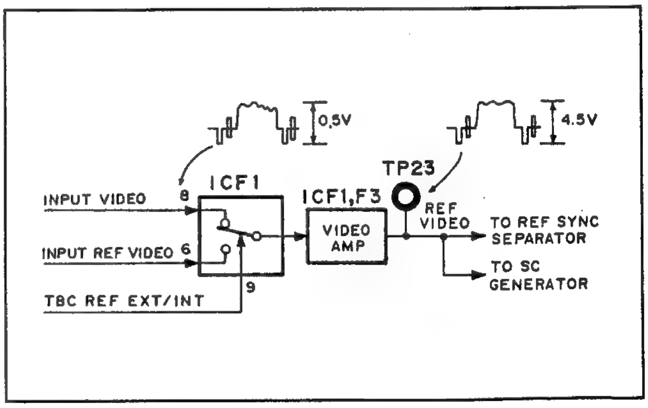


Fig. 4-4-35. TBC Reference Video Signal Selector (RD-7)

(2) **Reference sync separator (RD-7 board)**

This circuit separates the sync signal from the reference video signal which was selected by the TBC reference video signal selector.
The Y component is taken out from the reference video signal by the low-pass filter composed of C118, L12 and C119, and its pedestal level is clamped to 0V by Q9, ICF8 (pin 14), IC1 (pin 1) and IC1 (pin 7). The sync tip is sampled and held by ICF8 (pin 4) and ICF9 (pin 1), and the sync signal level is detected. The level of the detected sync signal is divided by (R243+R391) and R242 to produce a voltage which is one-half of the sync level. The sync signal is separated by a process of comparing in ICF10 the Y signal whose pedestal has been clamped to 0V and the voltage which is one-half of the sync tip level.
ICF8 (pin 10) switches the voltage division ratio of the sync level using R243, R391 and R242. Apart from the leading edge of the sync signal, the voltage which is compared by ICF10 approaches the tip of the sync signal and makes it harder for noise to cause disturbances.
Q8 and ICF6 form the rough sync separator. The pedestal clamp pulse and sync tip sampling pulse are then created from the sync signal, which is separated in this circuit, by ICF7.
The separated reference sync signal is sent to the gen-lock driver of the ICF12 sync generator.

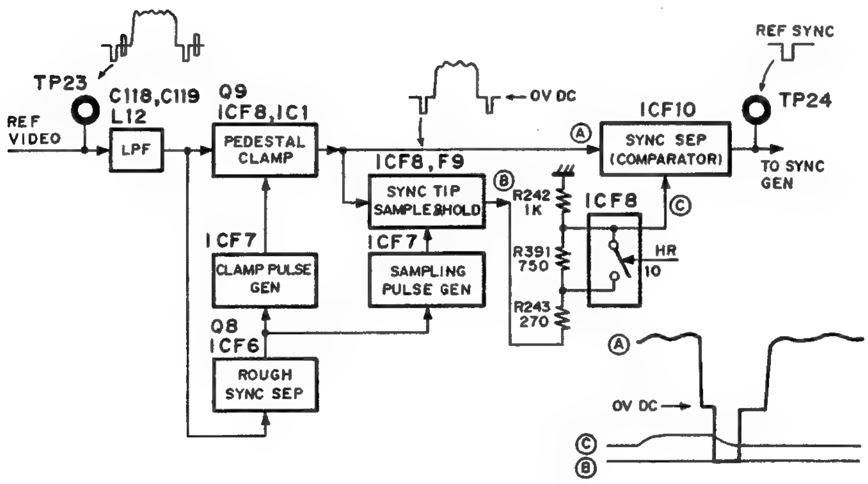


Fig. 4-4-36. **Reference Sync Separator (RD-7)**

(3) Sync and subcarrier locking (RD-7 board)

After it has been separated, the REF SYNC signal is supplied to the sync generator which is composed of the gen-lock driver IC (ICF12 : CX7903), sync generator IC (ICG17 : CX773B), 908FH VCO (X3) and sync phase controller (ICG15). This sync generator serves to generate various sync pulses and the HCK (908FH) pulse which is synchronized to the REF SYNC signal.
The subcarrier generator is composed of the 4.43 MHz bandpass filter, phase comparator (ICD2, ICD5), 4Fsc VCO (X4) and counter (ICD10). It serves to generate the RCK (4Fsc) pulse which is synchronized with the burst signal in the REF VIDEO signal.
For operation, the connections between the sync generator and subcarrier generator are changed for each of the 5 modes listed below.

(a) PAL • EXT • COLOR mode
(b) PAL • EXT • B&W mode
(c) PAL • INT mode
(d) SECAM • EXT mode
(e) SECAM • INT mode

(a) PAL • EXT • COLOR mode

In this mode the sync generator and subcarrier generator operate independently.
In the sync generator loop, the 908FH frequency signal output from the VCO (X3) is divided down in ICG17 by 908 to form the FH pulse. The phase of this FH pulse is adjusted in the sync delay circuit by the SYNC CONT voltage, after which the signal is supplied to ICF12 and its phase is compared with that of the reference sync signal. The resulting phase difference is converted into a voltage which is supplied to VCO (X3), and a loop is configured. It is in this loop that the various sync signals and 908FH signal which is synchronized with the reference sync signal are generated.
The sync delay circuit is composed of a monostable multivibrator (ICG15) and integrator (ICG2D and ICE13). The FH pulse (pin 23/ICG17) is output to

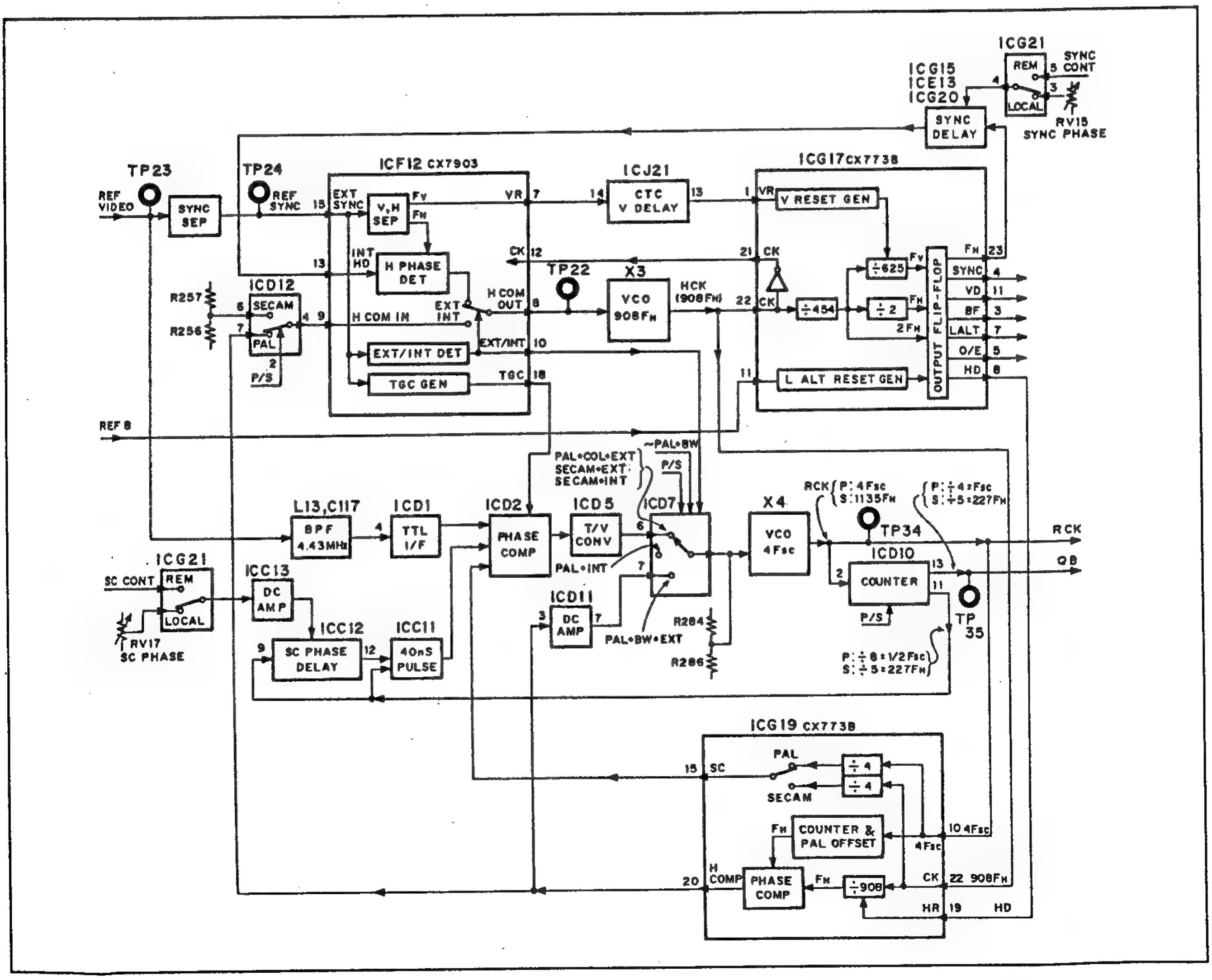


Fig. 4-4-37. Sync/Subcarrier Generators (RD-7)

a position which is ahead of the TBC SYNC signal (TP30 : A23C) by 174 clock pulses (equivalent to 12.3 μ sec). ICG15 is triggered by the FH pulse and the loop operates so that the fall edge of the ICG15 output signal is aligned with the leading edge phase of the reference sync signal. The ICG15 pulse width

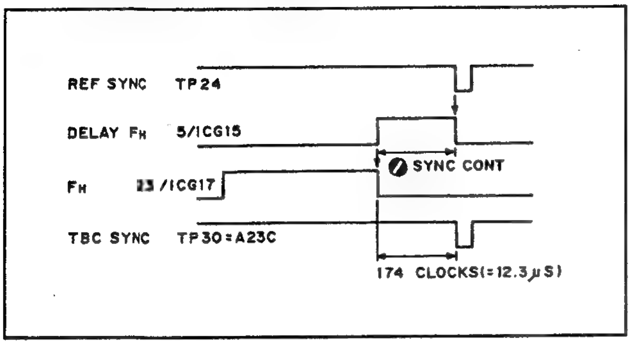


Fig. 4-4-38. Sync Delay Control Circuit (RD-7)

is controlled by the SYNC CONT voltage and, as a result, it is possible to yield an adjustment of the TBC SYNC signal phase across a -1 to $+3\,\mu$ sec range with respect to the reference sync signal.

In the subcarrier generator loop, the 4Fsc frequency signal which is output by the VCO (x4) is divided down by 8 in ICD10 to form the 1/2 Fsc signal which is then supplied to the ICC12 monostable multivibrator. The delay of this signal is first adjusted by the SC CONT voltage, after which a pulse with a width of 40 nsec is created by ICC11. While the burst gate pulse (TGC : pin 18/ICF12) is high, the phase of this 40 nsec pulse is compared by ICD2 with the phase of the burst signal in the reference signal, the resulting phase difference is converted into a voltage by ICD5 and supplied to VCO (X4), and a loop is configured. It is in this loop that the 4Fsc pulse synchronized to the burst signal in the reference signal is generated.

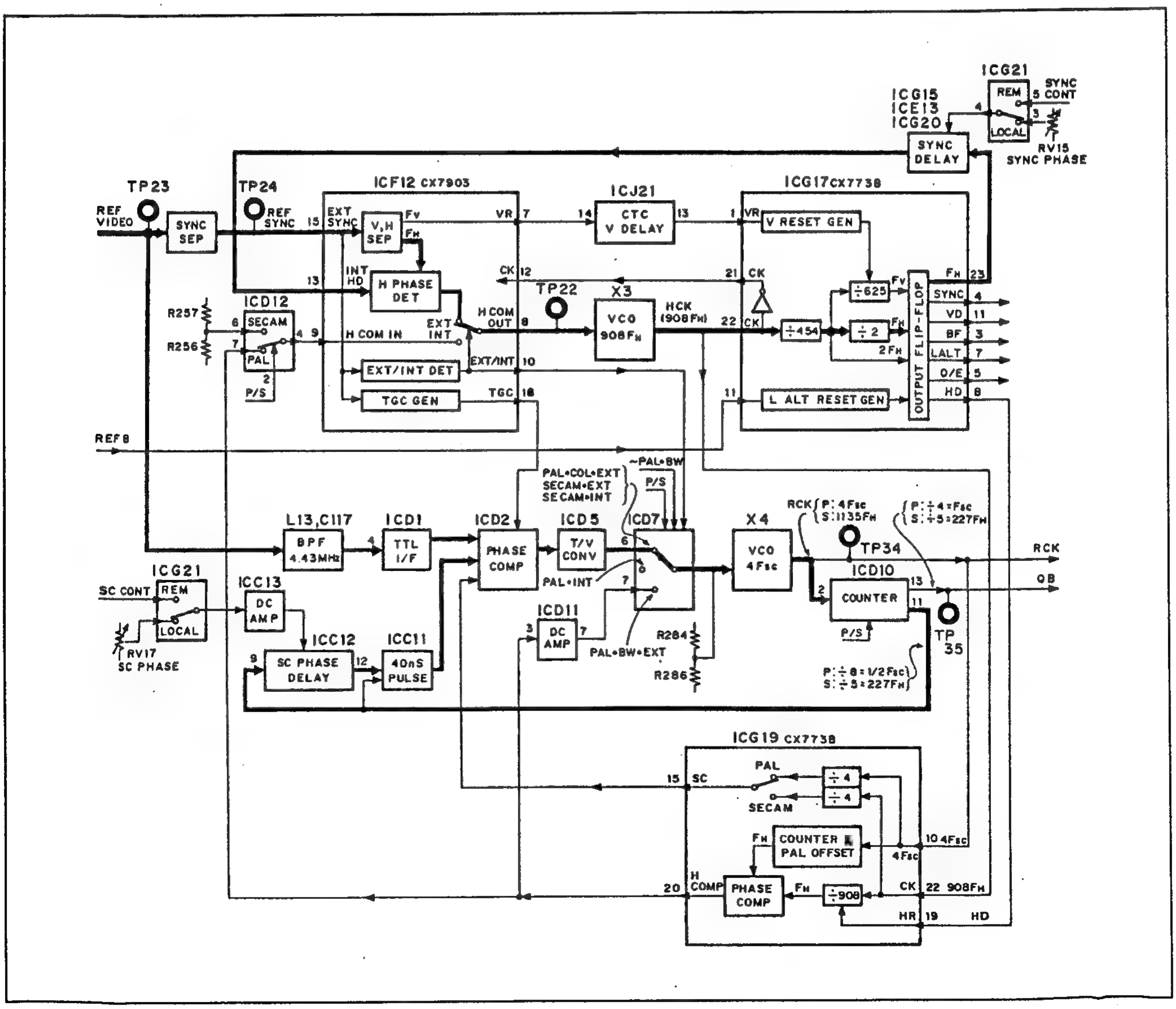


Fig. 4-4-39. Sync/Subcarrier Generators : PAL • EXT • COLOR Mode (RD-7)

(b) PAL・EXT・B&W mode

In this mode, the 908FH frequency signal which is synchronized to the REF SYNC signal is generated and the 4Fsc signal is created for synchronization with the 908FH signal.

As with the PAL・EXT・COLOR mode, the 908FH signal is similarly generated in the sync generator loop.

The 908FH signal synchronized with the REF SYNC signal and the 4Fsc VCO (X4) output are supplied to the phase comparator circuit (ICG19 : CX773B). ICG19 divides down the 908FH and 4Fsc signals to create two FH pulses. PAL offset is applied to the FH pulse created from the 4Fsc signal. The phases of these two FH pulses are compared, the voltage arising from the resulting phase difference is output from ICG19 pin 20 and supplied to the 4Fsc VCO, and a loop is configured. The Fsc and FH pulses stand in the following relationship :

$$4Fsc = \left(1135 + \frac{4}{625}\right) F_H$$

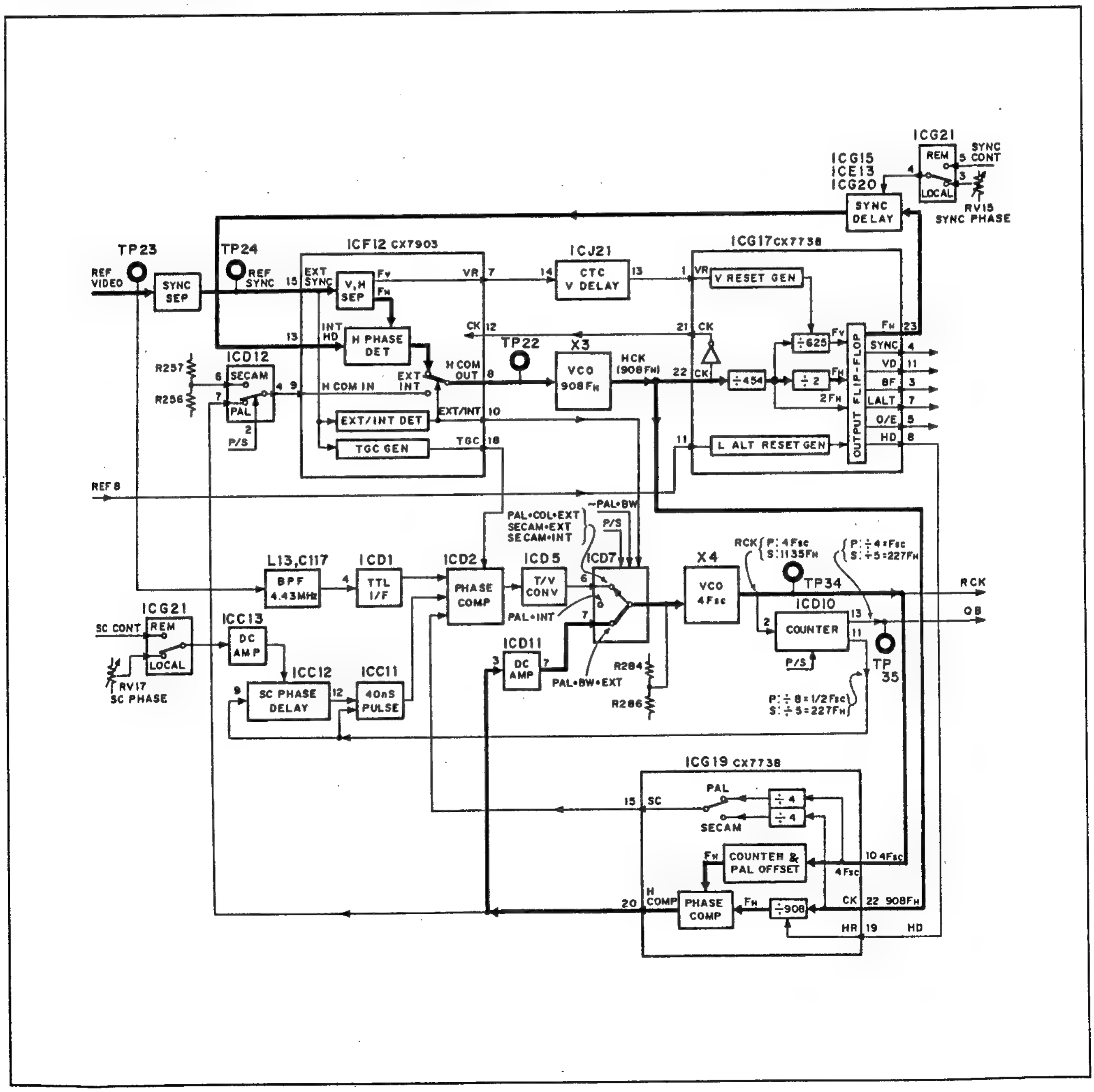


Fig. 4-4-40. Sync/Subcarrier Generators : PAL・EXT・B&W Mode (RD-7)

(c) PAL • INT mode

In this mode, fixed oscillation is provided by the 4Fsc VCO (X4) and the 908FH VCO is synchronized with it.

In the PAL • INT mode, the ICD7 selector selects a high impedance and the voltage produced by dividing +5V by R284 and R286 serves as the 4Fsc VCO control voltage.

As with the PAL • EXT • B&W mode, the phase of the 908FH VCO (X3) output signal is compared by ICG19 with the phase of the 4Fsc VCO output signal, the voltage arising from the phase difference is supplied to the 908FH VCO, and a loop is configured.

The Fsc and FH pulses stand in the following relationship :

$$4Fsc = (1135 + \frac{4}{625})\ F_H$$

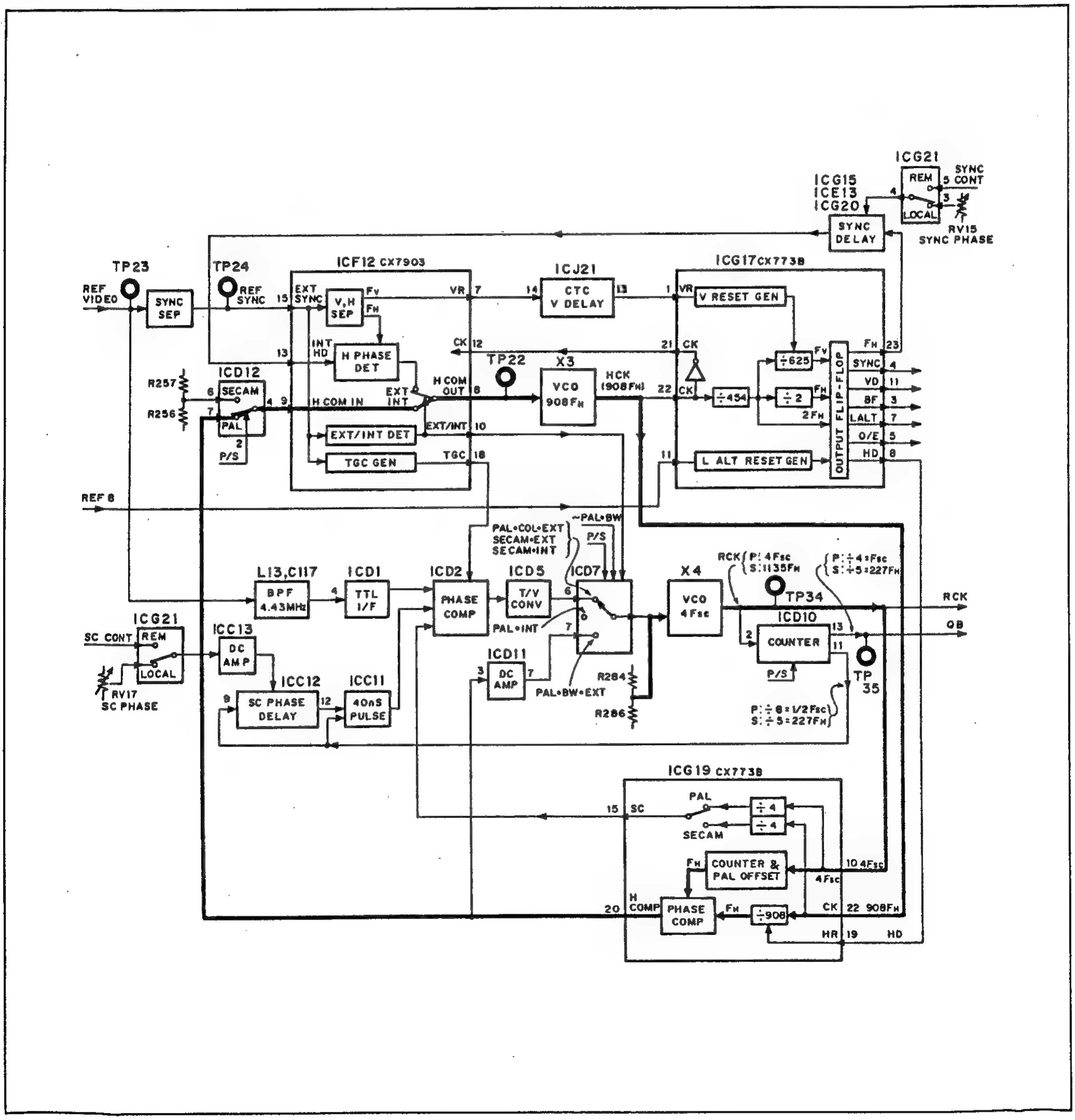


Fig. 4-4-41. Sync/Subcarrier Generators : PAL • INT Mode (RD-7)

(d) SECAM・EXT mode

In this mode, the 908F_H (HCK) signal synchronized with the REF SYNC signal is generated by VCO X3 and the RCK signal synchronized with this is generated by VCO X4.

The 908F_H signal is generated in the same way as in the PAL・EXT・COLOR mode.

The VCO X4 output signal is divided down by 5 in ICD10 and the phase of the resulting signal is compared in ICD2 with the phase of the VCO X3 (908F_H) output signal which has been divided by 4. The phase difference is converted into a voltage by ICD5 and supplied to VCO X4, and a loop is configured. The frequencies of the RCK and HCK signals applying in this case stand in the following relationship.

$$RCK = \frac{5}{4} HCK$$

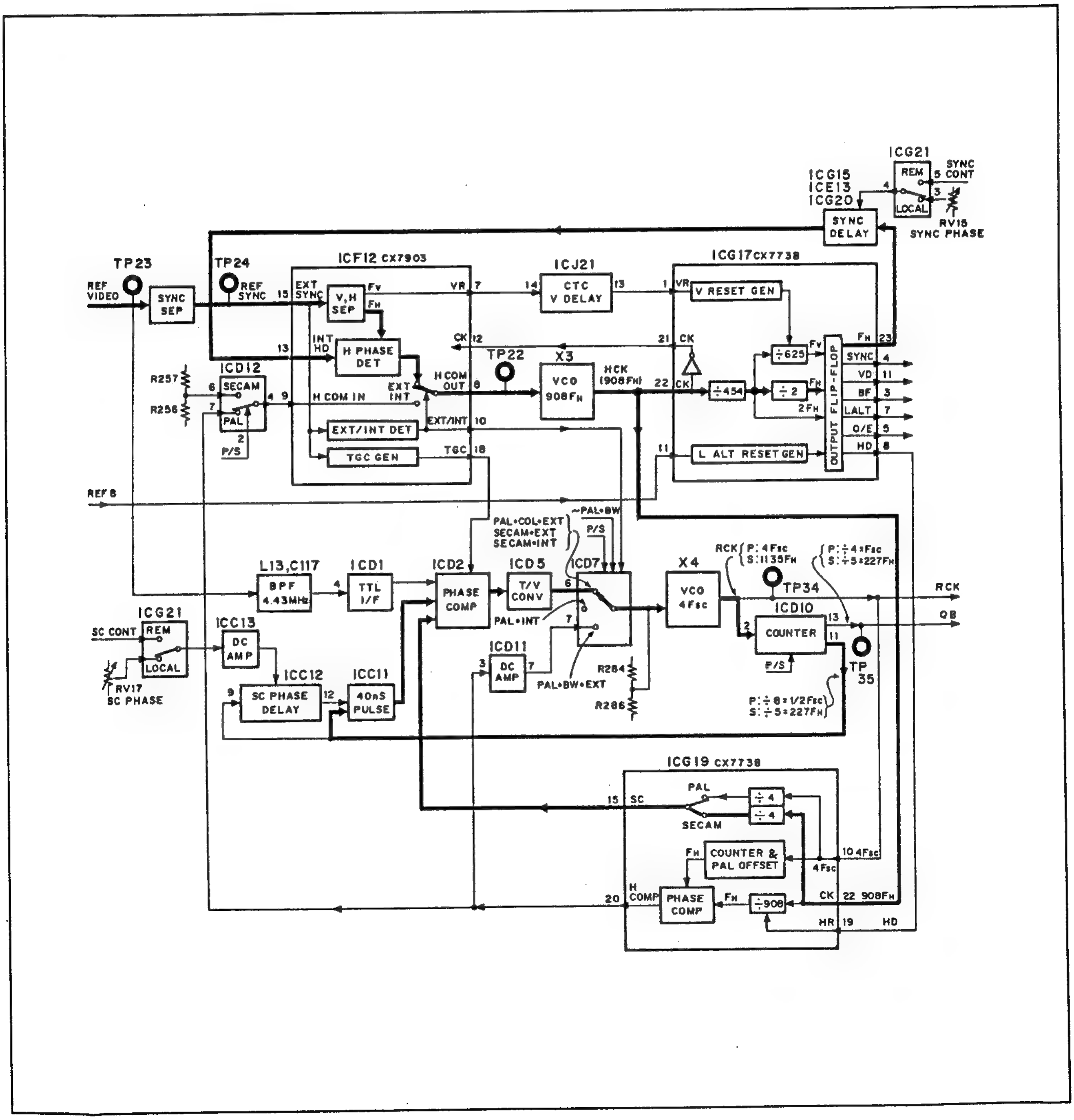


Fig. 4-4-42. Sync/Subcarrier Generators : SECAM・EXT Mode (RD-7)

(e) SECAM • INT mode

In this mode, the voltage produced by dividing +5V with R257 and R256 serves as the the 908FH VCO control voltage, and the 908FH VCO generates a fixed oscillation frequency. As with the SECAM•EXT mode, VCO X4 is synchronized with the 908FH signal.

$$RCK = \frac{5}{4} HCK$$

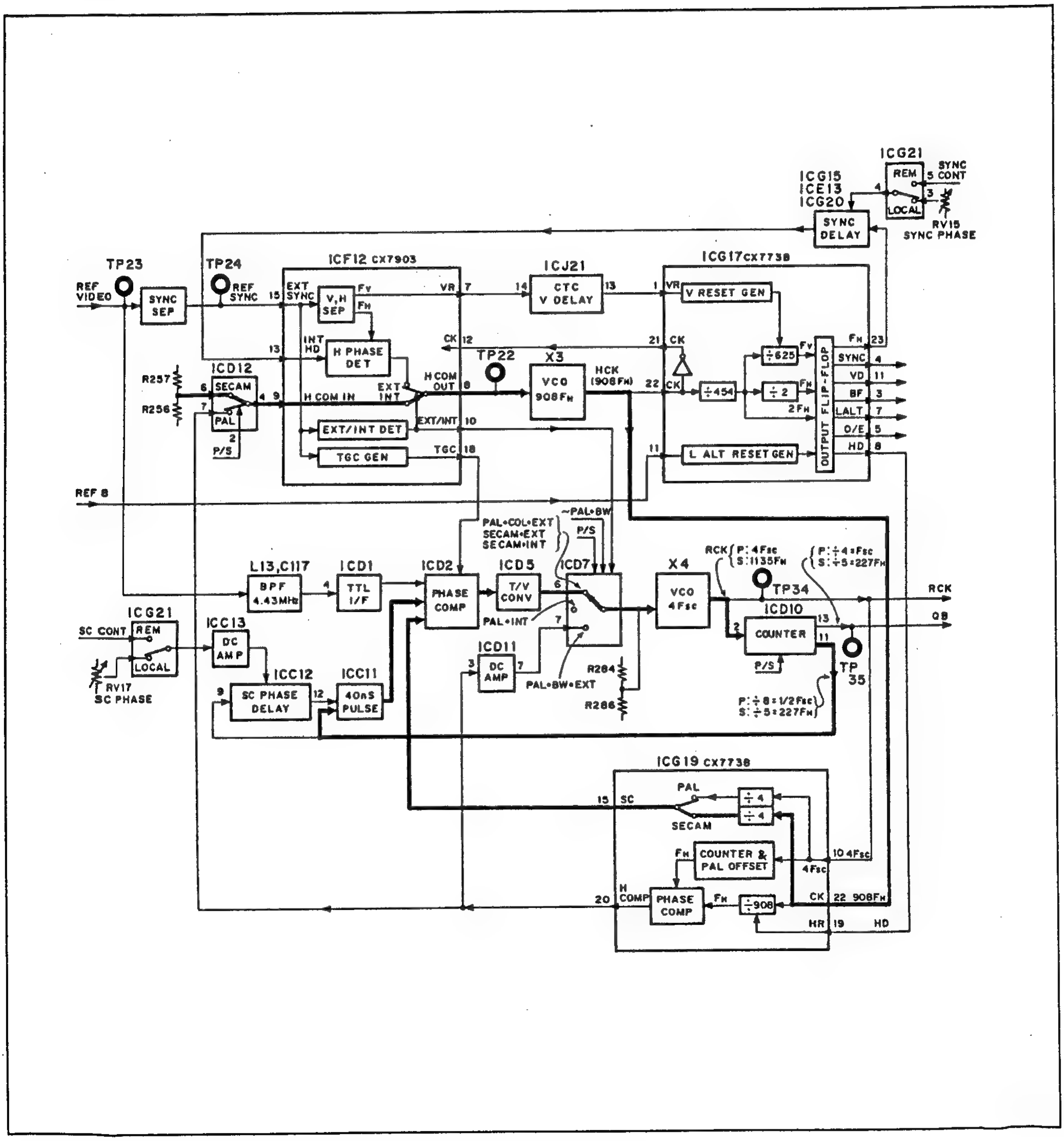


Fig. 4-4-43. Sync/Subcarrier Generators : SECAM • INT Mode (RD-7)

(4) V phase control (RD-7 board)

The TBC sync signal is synchronized to the reference sync signal by resetting the sync generator using the VR (V reset) signal generated from the reference sync signal by the ICF12 gen-lock driver. Depending on the mode, the VR signal is delayed by the CTC (ICJ21 : μ PD71054C) and, as a result, the vertical phase of the TBC sync signal is delayed. The 454FH pulse, which is produced by dividing down by 2 the 908FH VCO output is used for the CTC clock signal.

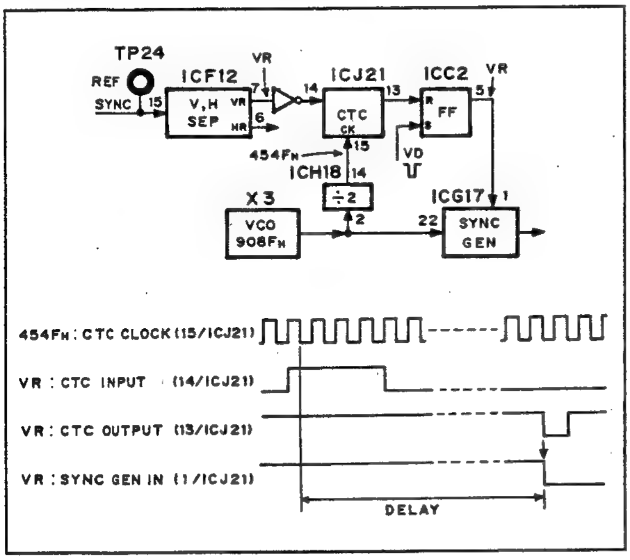


Fig. 4-4-44. V Reset Delay Circuit (RD-7)

The vertical phase of the video signal read from the main memory is determined by the REF VN signal. Depending on the mode, the VD pulse generated by the sync generator is delayed by the CTC (ICJ19 : μ PD71054C) to form the REF VN signal. The R ZERO signal is used as the H rate pulse with a timing delayed slightly from the VD pulse for the CTC clock signal.

The video signal which is read from the main memory is further delayed by the CK board and PR board. The following table lists the VR signal delays and video signal delays for each of the various modes.

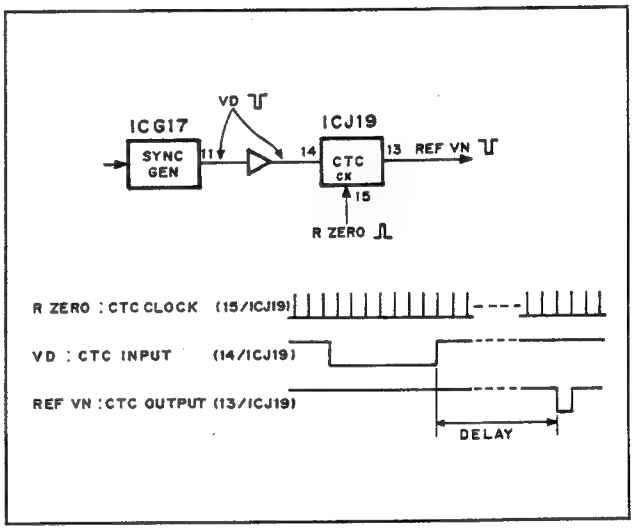


Fig. 4-4-45. REF VN Generator (RD-7)

VTR status			VR delay	Video signal delay		
Mode	PR board	PAL SECAM		REF VN	CK board	PR board
NORMAL	PR-92	×	0*5	0*5	0	0
	PR-98	×	0*5	0*5	0	2H
EE NON DELAY*1 or PREVIEW NON DELAY*2	PR-92	×	0	0	4H	0
	PR-98	PAL	0	2H	4H	2H
		SECAM	0	0	4H	2H
EE DELAY*3 or PREVIEW DELAY*4	PR-92	×	8H	8H	0	0
	PR-98	×	8H	6H	0	2H
CONFI DELAY	PR-92	×	1/3V+13H	1/3V+13H	0	0
	PR-98	×	1/3V+13H	1/3V+11H	0	2H

*1 : When [I10. EE SYNC DELAY] menu is set to [DISABLE]
*2 : When [I11. EDIT SYNC DELAY] menu is set to [DISABLE]
*3 : When [I10. EE SYNC DELAY] menu is set to [ENABLE]
*4 : When [I11. EDIT SYNC DELAY] menu is set to [ENABLE]
*5 : There is no need to delay the VR and REF VN signals since the drum servo is advanced by

(5) Y ADD GATE and UMSC signal (RD-7)

The Y ADD GATE signal is a pulse which prohibits Y signal line adding in the DT playback mode and it indicates the lines which do not have video components. Using the VD pulse provided by the sync generator as the input and the R ZERO signal as the clock pulse, the CTC (ICJ19 : μ PD71054C) generates the Y ADD GATE signal.
Normally, the Y ADD GATE signal is low for 25 lines of the vertical blanking period. In the case of zero advance (see note below), the video start point is delayed so that it comes after the sync signal in the output signal and so this delay is added and the Y ADD GATE signal is created. This means that this signal has an increased width equivalent to 8H with PAL • PR98 and equivalent to 4H for PAL • PR92.

Note : Zero advance
When the sync signal of the TBC output is not delayed in the EE mode or EDIT mode, the vertical sync signal of the TBC output will have the same phase as the reference video signal. This is known as zero advance.

In the case of SECAM signals, the video start point is delayed by 6H but the Y ADD GATE signal width is not increased because this signal acts as the reference pulse of the UMSC signal which is described below.
The SECAM signals are frequency-modulated signals and lines where the subcarrier is not superimposed are characterized by noise. For instance, in the EE • NON DELAY mode, the subcarrier is added to the 4 lines following the vertical blanking period and the lines are replaced with a black picture. The UMSC signal functions to indicate those lines which are to be replaced with the black picture.
The UMSC signals are produced from the Y ADD GATE signal, V ID signal and the signal generated by the two CTCs (ICJ18 : μ PD71054C) which use the VD pulse as the input and the R ZERO signal as the clock. The V ID signal serves to indicate the lines where the SECAM ID signal is to be superimposed.

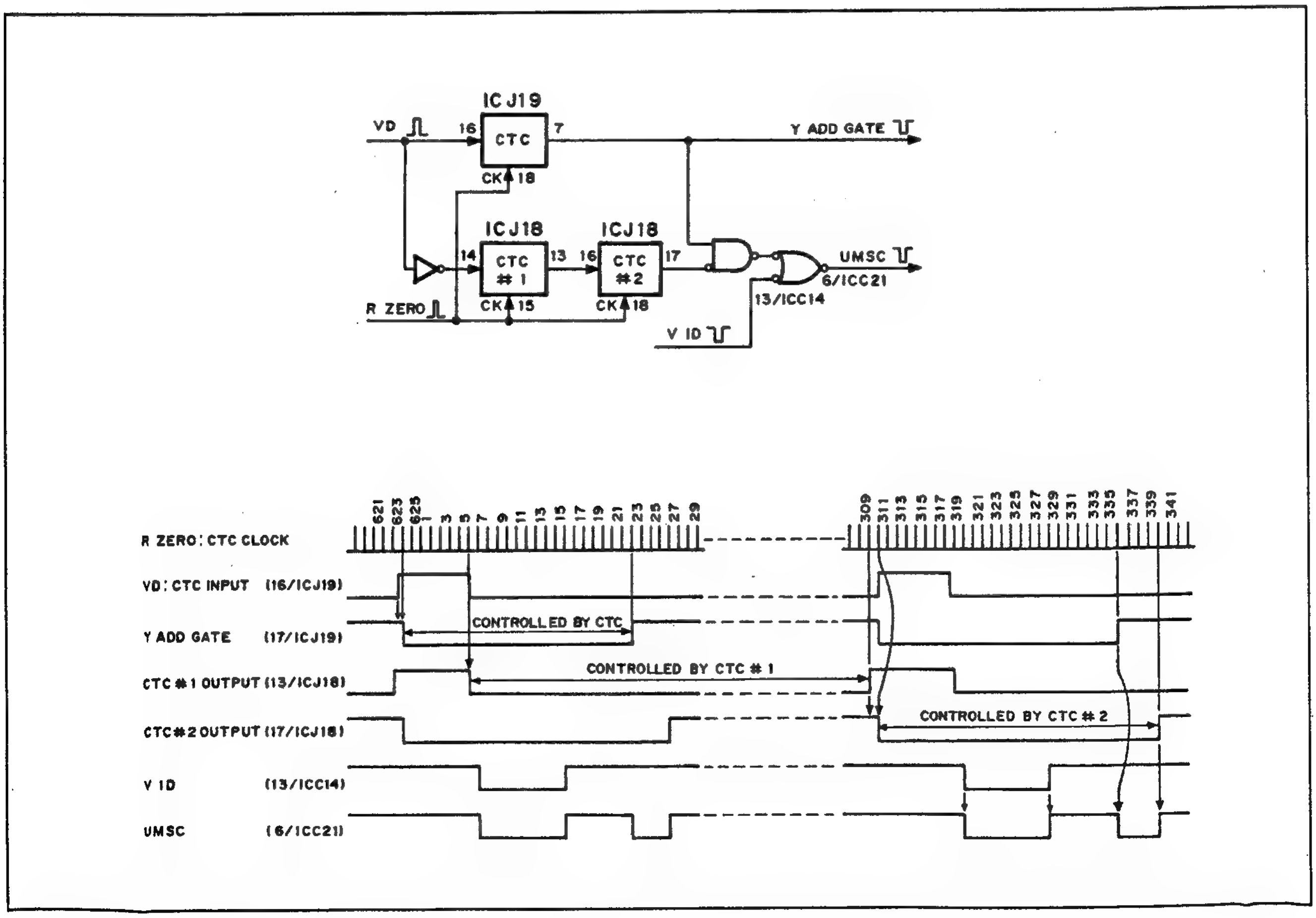


Fig. 4-4-46. Y ADD GATE/UMSC Generator (RD-7)

dcdsfe mdjsfWhen the SECAM • PB COLOR • $\overline{\text{F BID}}$ mode is established, the UMSC signals are generated as shown in the figure below.

A. EE • DELAY EN
B. EE • DELAY DISABLE
C. PLAY STATUS • EDIT • DELAY DISABLE
D. PLAY STATUS • $\overline{\text{EDIT • DELAY DISABLE}}$
E. BID • EDIT • DELAY DISABLE
F. BID • $\overline{\text{EDIT • DELAY DISABLE}}$
G. DT • Y ADD OFF
H. DT • Y ADD ON

Note: The "PLAY STATUS" signifies the NORMAL FWD mode or EE mode in which the capstan servo is locked.

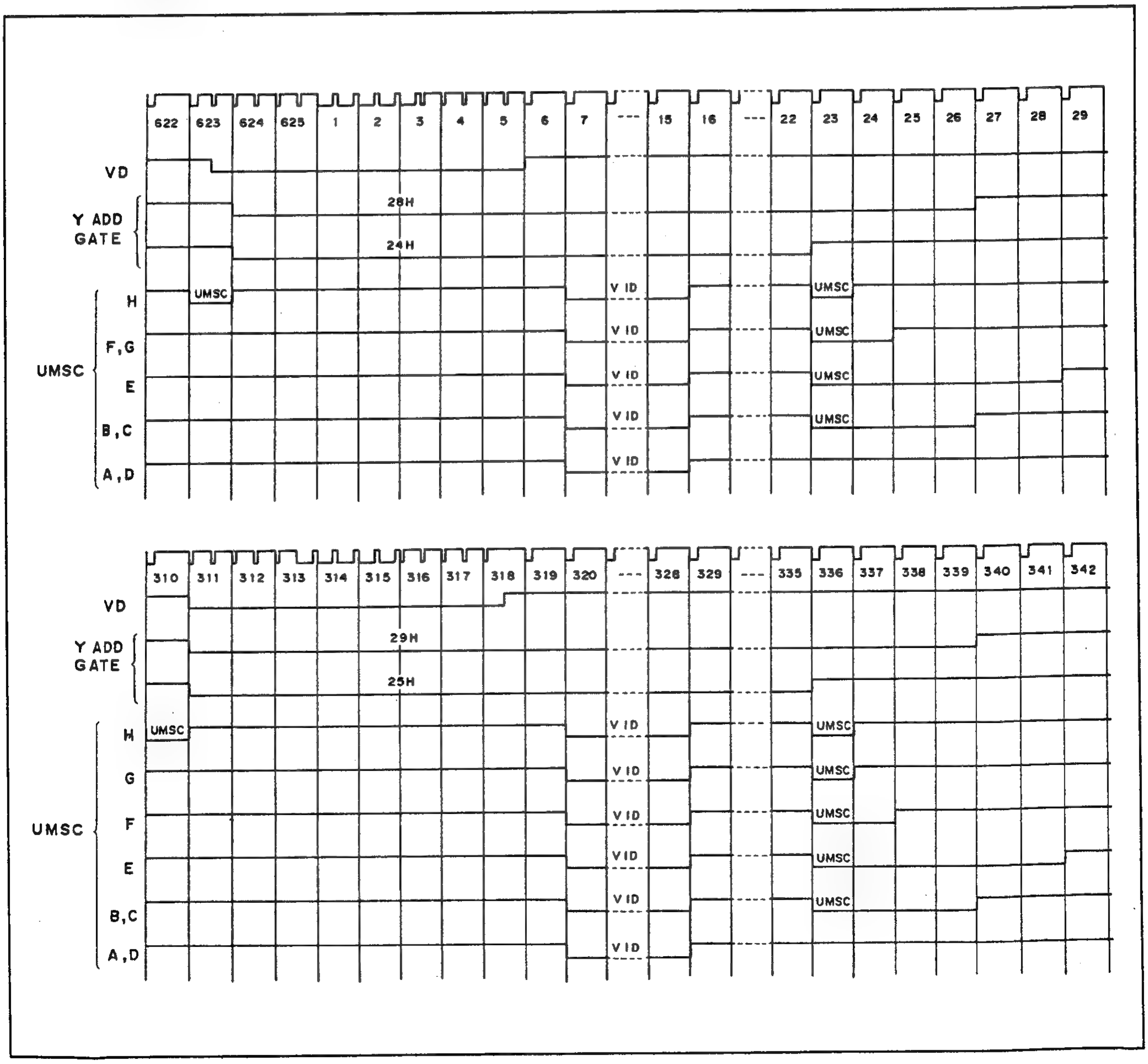


Fig. 4-4-47. UMSC Signals : SECAM • PB COLOR • $\overline{\text{F BID}}$ Mode

(6) SECAM B&W mode

In the PAL mode, the COL/B&W signal which is detected from the reference video signal determines whether the burst signal is to be added to the TBC output signal. The burst signal that is added is created from the reference video signal.
However, in the SECAM mode, the burst (line ID) signal read from the main memory is added to the TBC output signal without change or modification. If the burst signal is added again, discontinuity will result in the carrier and the color will be disturbed. Consequently, whether the picture is to be in color or B&W for the SECAM mode is determined not by the REF COL/B&W signal but by the PB COL/B &W signal. This PB COL/B&W signal also determines whether the SECAM ID (V ID) signal is to be added to the TBC output signal.
A description of each of the SECAM B&W modes is given below.

(a) BLACK BURST ENABLE (I88 menu)
The TBC output signal forms a black picture or black-and-white striped picture, depending on what has been selected in the [I88. BLACK BURST OUTPUT] menu. The PB COL/B&W signal is low (=B&W) at this time and so the TBC output signal does not have the V ID signal and line ID signal.

(b) PR TEST 1 ENABLE (T05 menu)
When the PB COL/B&W signal is high (=COL), the V ID signal is added to the TBC output signal; when it is low (=B&W), it is not added. Regardless of the status of the PB COL/B&W signal, the line ID signal is not added. If the monitor is the type which detects the V ID signal, noise will affect the whole screen in the PB COLOR mode, and a signal without the line ID and subcarrier will be output for use in the TEST mode.

(c) BVB ENABLE (S06 menu)
When the PB COL/B&W signal is high (=COL), the V ID signal is added to the TBC output signal; when it is low (=B&W), it is not added. The video lines of the TBC output have the line ID and subcarrier when the PB COL/B&W signal is high and a black picture is produced.

(7) Blanking pulse generator (RD-7 board)

The horizontal (H) blanking pulses are produced from the HD pulses by ICF20. Their width differs depending on whether the signals are SECAM or PAL (and SECAM B&W) and this means that the time constant of ICF20 is switched by ICH14. The pulses are supplied to ICJ13 and mixed with the vertical blanking pulses produced by ICJ13.

The vertical blanking pulses are created from the VD pulses by ICJ13 (CX20162). ICJ13 is provided with a pin which controls whether lines 7 through 22 (320 through 335) are to be blanked or not, and the control signal specified by the [I80. BLANKING LINE] menu is input to this pin. The blanking width of line 23 is based on the half H pulse provided by ICJ6.
ICJ13 also creates the SECAM V ID pulses.

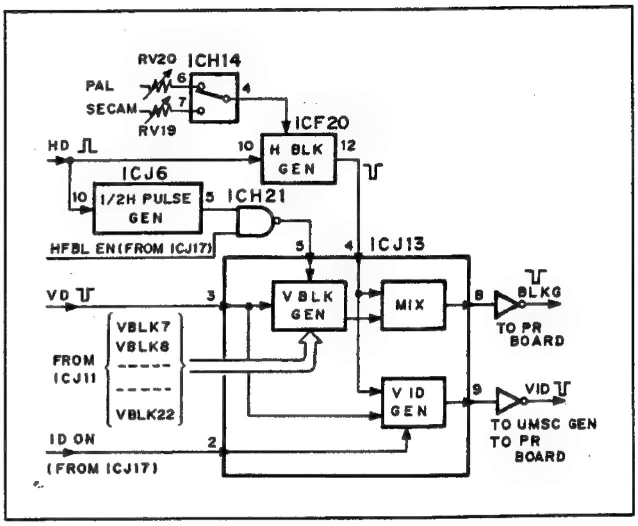


Fig. 4-4-48. Blanking Pulse Generator (RD-7)

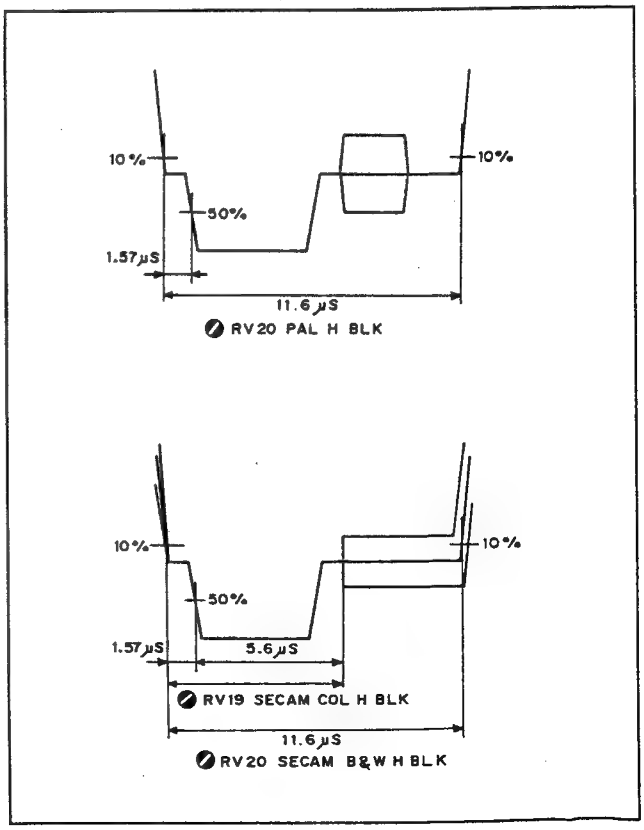


Fig. 4-4-49. H Blanking

4-4-7. Read Clock/Read Zero Generator (RD-7 Board)

(1) Burst-chroma phase controller (RD-7 board)

The Fsc pulse (QB) generated by the subcarrier generator is supplied to ICB10, and the RD Fsc signal whose phase is shifted 90° every other line is created. The RD Fsc signal is sent to the PR board to serve as the PAL burst signal.
Prior to its 90° shift, the Fsc pulse is supplied to pin 1 of the ICB1 monostable multivibrator, its phase is shifted by the BURST CHROMA control (RV23 or remote control), and the REF CK signal is produced. The phase of this REF CK signal is then shifted by ICB1/RV25 and modulated in the next stage by the velocity error voltage, after which the fourth-order harmonics are extracted to produce the read clock signal for the PAL mode.
The REF CK signal is also sent to the PR board where it is used to create the DECODE/ENCODE CARRIER.

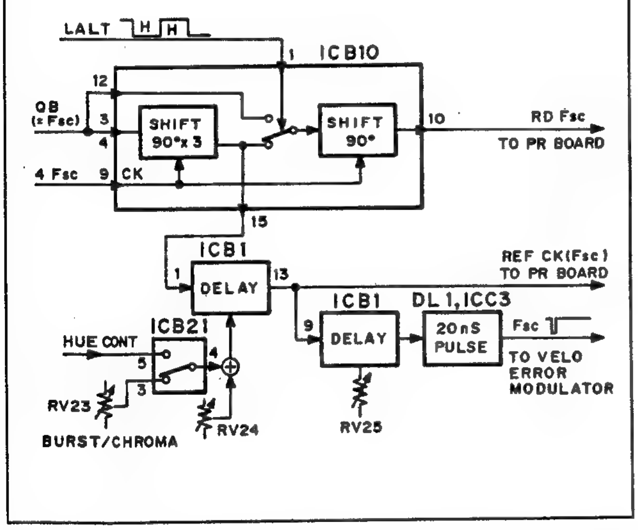


Fig. 4-4-50. Burst-Chroma Phase Controller (RD-7)

(2) Velocity error modulator and read clock generator (RD-7 board)

After the phase of the Fsc pulse has been adjusted by the burst-chroma phase controller, it is modulated by the velocity error voltage. The DP VIDEO signal (Y signal sent from the write side for differential phase compensation) is superimposed onto the velocity error voltage, and phase modulation conducted for differential phase compensation is carried out simultaneously. In the SECAM mode, the signals bypass this circuit.

The Fsc pulse is supplied to pin 13 of the RS flip-flop which is composed of the ICB9 NAND gate, ICB9 pin 3 is set low at the fall edge of the pulse, and the output voltage of the sawtooth wave generator composed of ICB7, Q10 and Q11 starts to rise. This ramp wave is supplied to pin 3 of the ICC10 voltage comparator and ICC10 pin 9 is set low when the velocity error voltage supplied to pin 4 is exceeded. The ICC10 pin 9 output enters pin 1 of the ICB9 flip-flop, the RS flip-flop output is reset high, and the ramp wave (TP25) is reset. When the next Fsc pulse is supplied to the RS flip-flop, the same operation is repeated. As a result, the phase of the pulse which is output from ICC10 pin 9 is shifted in accordance with the velocity error voltage.
The fourth-order harmonic components of the phase-modulated Fsc pulse are filtered out by the FL1 bandpass filter and the PAL read clock is created.
In the SECAM mode, both velocity error and differential phase compensation are not necessary and so the 1135FH pulse, which is created by the sync generator circuit, is used without change or modification as the read clock signal. ICC5 functions to select the PAL and SECAM read clock signals.

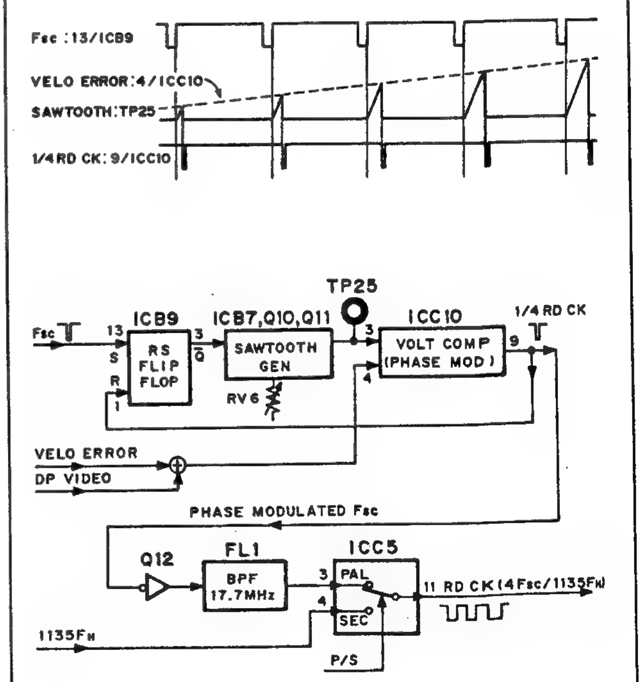


Fig. 4-4-51. Velocity Error Modulator and Read Clock Generator (RD-7)

(3) PAL H generator and REF SCH detector (RD-7 board)

The PAL H generator is composed of the V sawtooth wave generator, H sawtooth wave generator, voltage comparator and SC-H phase comparator. The PAL H pulse is the signal produced by removing the V/2 offset from the HD pulse created by the sync generator, and it serves as the reference signal for creating the PAL read zero signal.
The V sawtooth wave is produced from the VD pulse by the integrator (ICE19) and analog switch (ICF21). The H sawtooth wave is produced from the HD pulse by the switching transistor (Q13), constant-current source (ICE19, Q14) and capacitor (C153). By comparing the two voltages in ICD20, H pulse whose phase has been modulated by the V sawtooth wave is created. The ramp of the V sawtooth wave is adjusted so that the H pulse phase advances by an amount equivalent to half the subcarrier period per field. As a result, the PAL H pulses with phases of 0°, 270°, 180° and 90° with respect to the subcarrier are output in this sequence from ICD20.
The 4Fsc (RD CK), Fsc (1/4 RD CK), N/I (LALT/2) and RD FLD (O/E) signals are supplied to ICE15, 1/Fsc interval pulse whose phase with respect to the subcarrier commences at 0°, 270°, 180° and 90° is created, and the phase of the pulse is compared with that of the PAL H pulse in ICD19 and ICC19. The phase difference is converted by ICC17 into a voltage, and a loop is configured by adding this phase difference voltage (TP36) to the V sawtooth wave and it is controlled so that the PAL H pulse phase will be made constant.
When the phase difference voltage (TP36 : TBC REC SCH signal) exceeds ±3V, the CF RESET signal is created by DT CPU (ICM18) and gated by the VD pulse in ICC15, and the phase difference voltage is reset during the vertical blanking period.

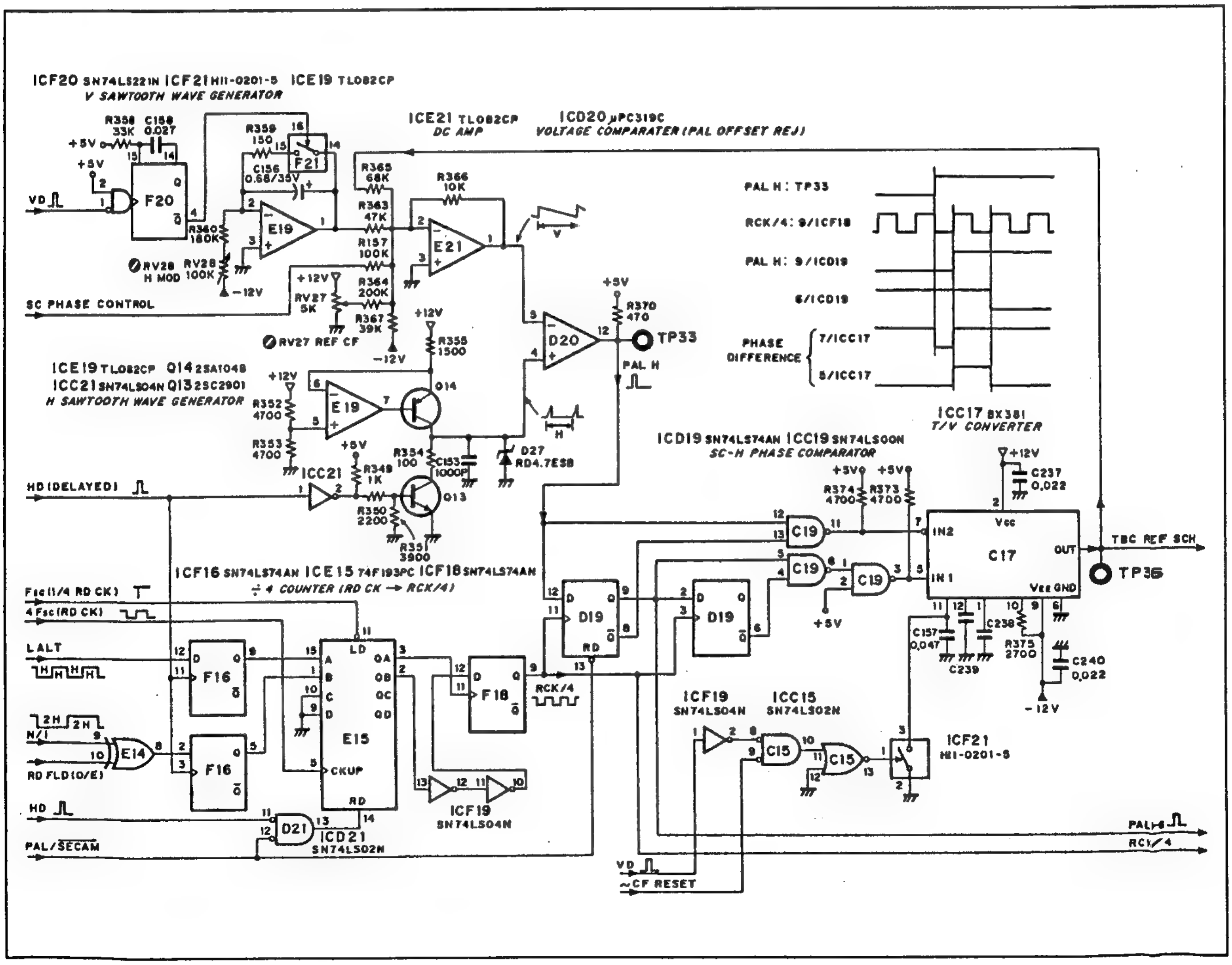


Fig. 4-4-52. PAL H Generator and REF SCH Detector (RD-7)

(4) **READ ZERO generator (RD-7)**

The READ ZERO generator is composed of the CTC (ICJ21 : μ PD71054C) and the counter (ICA12 and D14 : SN74LS163AN). In the PAL mode, the READ ZERO pulse is created based on the PAL H pulse; in the SECAM mode, it is created based on the HD pulse. ICD21 functions to select the PAL H and HD pulses.

The READ ZERO pulse is created at a position which allows for the system delay from the WRITE ZERO pulse. The PAL H pulse is positioned between the READ ZERO 2 and READ ZERO 3 pulses, as shown in Fig. 4-4-53, and the CTC uses this PAL H pulse as its input and, with the RCK/4 pulse serving as the clock pulse, the counter (ICA12) load pulse is output in each mode. The RCK/4 pulse is created when the RD CK pulse is divided by 4 in ICE15 (Fig. 4-4-52). The ICE15 load data are latched by the HD pulse and so the RCK/4 pulse is characterized by discontinuity in the vicinity of the leading edge of the HD pulse. The RD CK pulse is a signal which has undergone velocity error compensation, which means that the RCK/4 pulse is discontinuous at the timing (1 to 2 μ sec from the leading edge of the H sync pulse) when the velocity error is reset. In order to prevent ICA12 from counting at these timings, the READ ZERO JUMP signal is set low for the READ ZERO 1 and READ ZERO 3 pulses.

The VPF1 and VPF2 signals provide the fine adjustment in each mode. The READ ZERO SHIFT signal is set high when the N/I signals of the write and read sides do not match. The READ ZERO pulse is shifted by 2 clocks at this time to prevent color reversal.

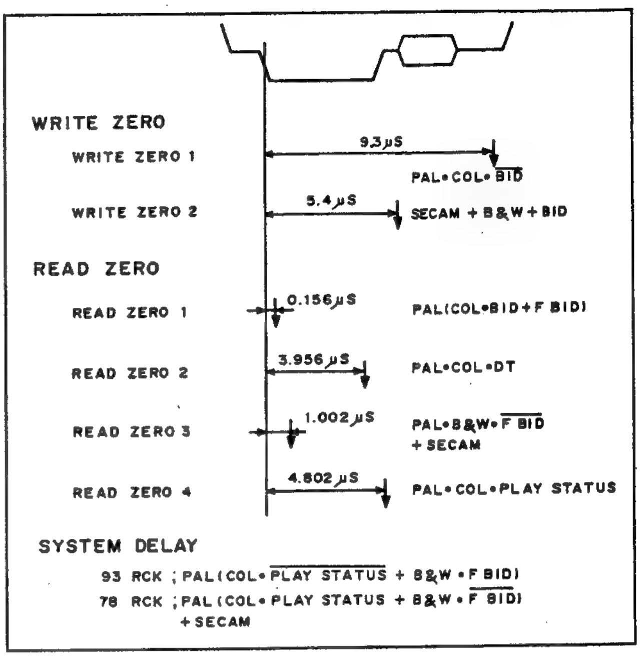


Fig. 4-4-53. READ ZERO Timing

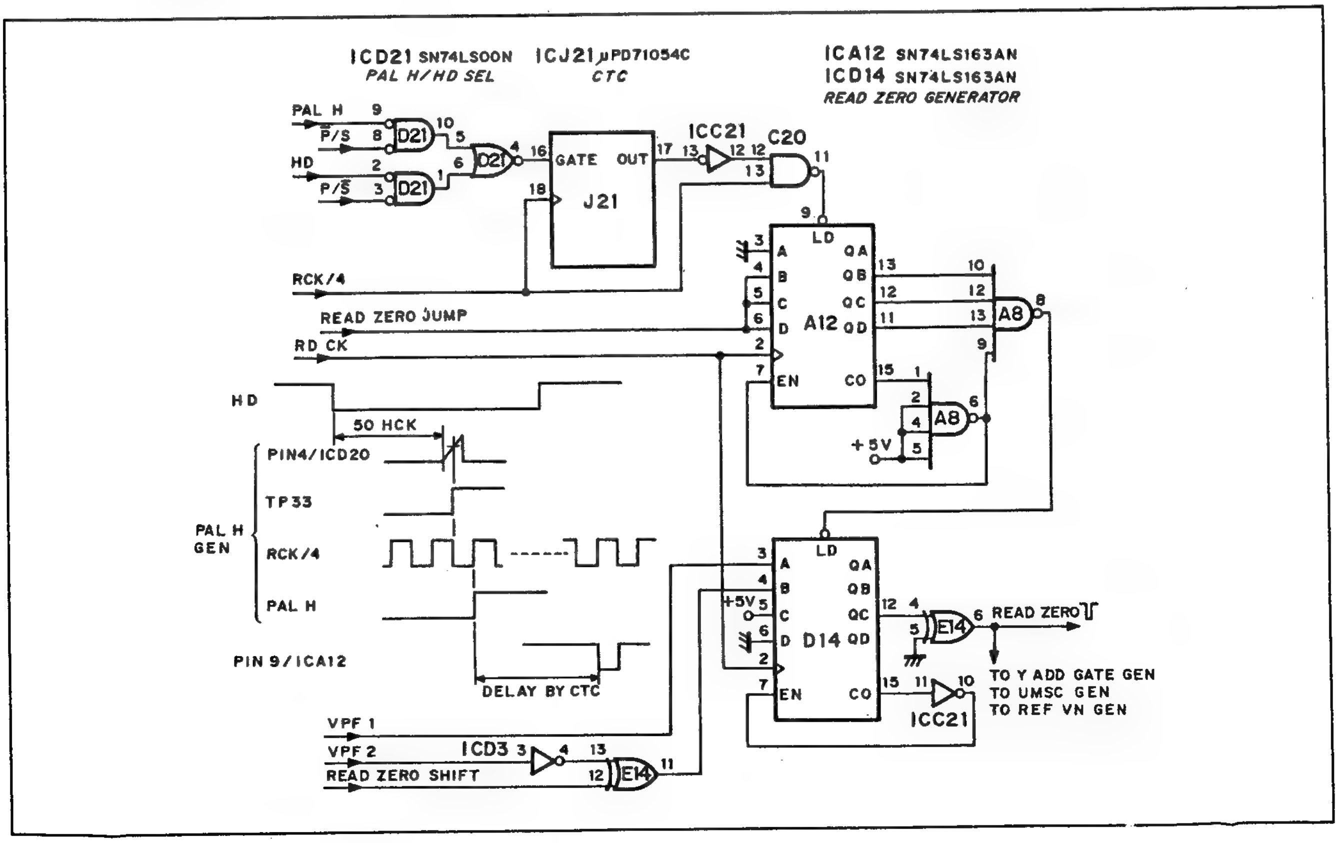


Fig. 4-4-54. READ ZERO Generator (RD-7)

4-4-8. Velocity Error Interpolator (RD-7 Board)

The velocity error voltage which has been decoded on the CK board is supplied to the velocity error interpolator on the RD-7 board. In the interpolator, it is interpolated by second order approximation so that it approaches a true velocity error.

The two-line adding of the velocity error voltage is conducted together with the line adding of the chroma signal.

The Y signal, which has been D/A converted, is first added to the interpolator output for DP compensation and it is then sent to the read clock generator so that the phase of the read clock will be modulated.

The principle of interpolation by the second order approximation is shown in Fig. 4-4-55. ϕ is the velocity error and t_H is the 64 μsec H period. $t=0$ is the timing at the W CK head (timing with APC applied to W CK). At this time, ϕ is equal to 0.

If it is assumed that the velocity error of a particular line Lo is ϕ_0 and the velocity error of the line before L_{-1} is ϕ_{-1} then the second order approximation of the change in the velocity error at Lo will be as follows :

$$\phi = \frac{1}{2t_H}\left\{\frac{1}{t_H}(\phi_0 - \phi_{-1})\,t^2 + (\phi_0 + \phi_{-1})\,t\right\} \cdots (1)$$

In the actual circuit, velocity errors ϕ_0 and ϕ_{-1} are ϕ-V converted and obtained as voltages V_0 and V_{-1}. The velocity error second order approximation interpolator is a circuit that generates the voltage below using V_0 and V_{-1} in correspondence with formula (1).

$$V = K\left\{\frac{1}{t_H}(V_0 - V_{-1})\,t^2 + (V_0 + V_{-1})\,t\right\} \cdots (2)$$

In Fig. 4-4-55, C144 holds V_{-1} and the voltage $C(V_0-V_{-1})\,t$ produced by integrating V_0-V_{-1} is output to pin 1 of ICB14. V_0 and V_{-1} are then added to this voltage and when this is supplied to next-stage integrator ICB12, the voltage in the following formula is obtained at pin 1/ICB12 and formula (2) is realized.

$$K\left\{\frac{1}{t_H}(V_0 - V_{-1})\,t^2 + (V_0 + V_{-1})\,t\right\}$$

The voltage produced here is supplied to the velocity error moudlator, V-ϕ converted and, as a result, formula (1) is realized.

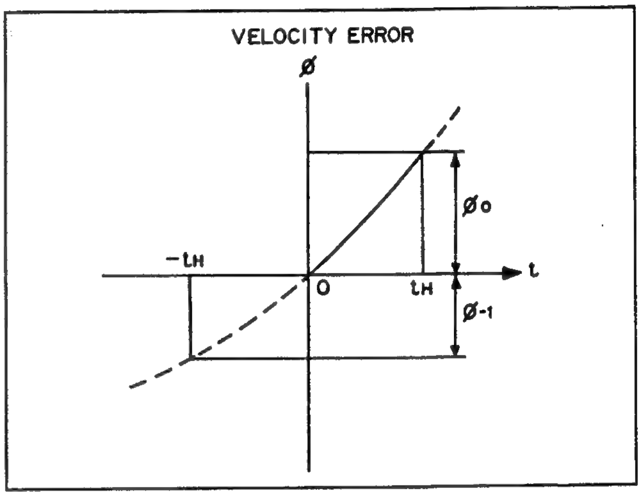


Fig. 4-4-55. Principle of Interpolation by 2nd-Order Approximation

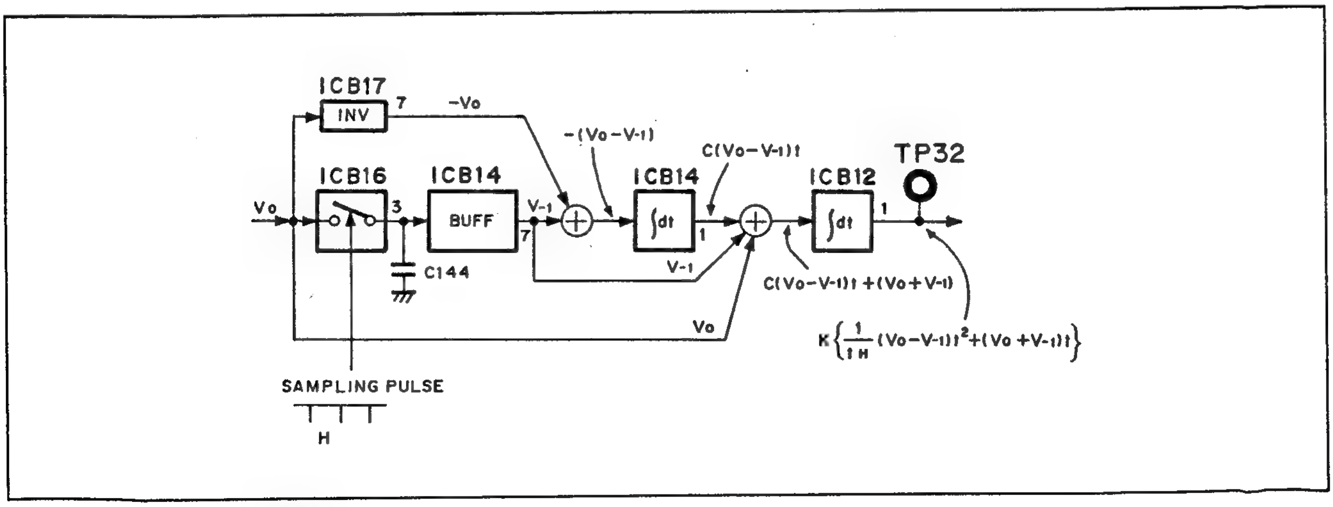


Fig. 4-4-56. 2-Line Adding and Interpolation by 2nd-Order Approximation (RD-7)

The integration capacitor in the interpolator is discharged by the HD pulse which is ahead of the read zero signal, and the velocity error voltage is reset. During the VD period, the resetting mode is established and the interpolator output is turned into a constant DC voltage.

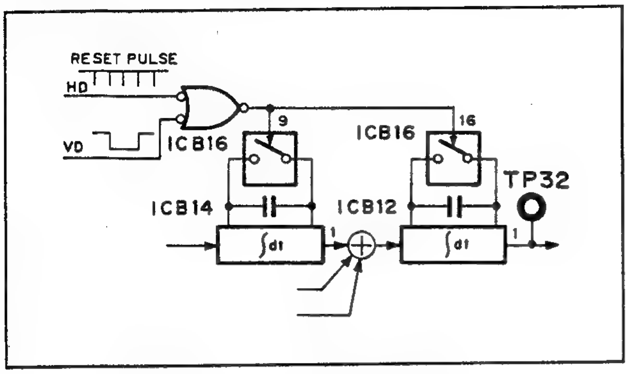


Fig. 4-4-57. Velocity Error Reset (RD-7)

4-4-9. DP Video Modulator (RD-7, PR-98/92 Boards)

DP (Differential Phase) is compensated, as outlined below, in the TBC block.
The 8-bit Y signal data supplied from the Y/C separator circuit is converted into an analog signal by ICJ9 (or by ICK5 on the PR-92 board). The offset and gain of this analog Y signal are then adjusted by RV1 and RV2, and the signal is further supplied to the RD-7 board for the purpose of DP compensation.
The DP VIDEO (analog Y) signal supplied to the RD-7 board is added to the velocity error and supplied to the phase modulator circuit of the read clock. DP is compensated by reading out the video data from the memory using the phase-modulated read clock signal.

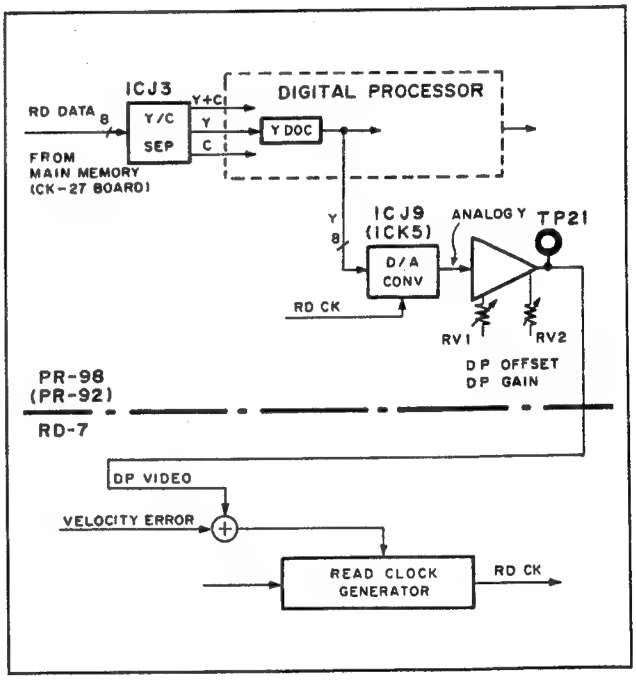


Fig. 4-4-58. DP Video Modulator (RD-7, PR-98/92)

(2) Y signal digital processor (PR-92 board)

(a) Y signal dropout compensator (PR-92 board)

Dropouts in the Y signal are compensated for by "partial replacement using the Y signal of 1H before." The Y signal data which have been output from the ICJ3 Y/C separator are applied to terminal "1" of DO switcher ICJ6 and ICK6. The DO switcher output is delayed 1H by line memory ICJ7 and returned to terminal "0" of the DO switcher. The DO switcher normally selects terminal "1" but it is switched to "0" during the dropout period and the data of 1H before the dropouts are supplied to the line memory again.
The μPD41102C used for the memory devices is a FIFO (first-in, first-out) memory and so the memory addresses are created from the clock input.

(b) DOC control circuit (PR-92 board)

The DOC control circuit expands and delays the pulse width of the DO signal (Y DO) which has passed through the main memory and it outputs the DOC switching control signals which accord with the various modes.
The DOC control circuit employs a special-purpose IC (ICM9 : CX20219). Its main functions are outlined below.

1. Input DO pulse delay (38 to 50 clocks)
2. Pulse width expansion (±32 clocks)
3. DO processing switching of the previous line or the lines before and after
4. Line adding peripheral circuitry
5. RZ (READ ZERO) signal differential circuit
6. Maximum operating frequency of 20 MHz
7. Compatible with NTSC, PAL and SECAM systems

Fig. 4-4-62 shows the configuration of the CX20219 circuit.

(c) Y-ADD circuit (PR-92 board)

With variable speed playback such as in the DT/BIDIREX mode, the phenomenon inevitably occurs in which the field sequence of the playback video signal matches or fails to match the reference video signal. The matching/non-matching repeat period is long when the tape speed approaches ±1 times normal speed, but its length is reduced when the speed deviates from ±1 times normal speed.
When the field sequence does not match the reference video signal, it is made to match as far as appearances are concerned either by 1H delaying the even fields of the main memory output or by 1H advancing the odd fields. As a result, the picture in the mismatched field will shift downward by 0.5H. This is known as vertical (V) shift. Depending on the tape speed, the V shift phenomenon is perceived as flicker.
The Y-ADD ON mode is provided in order to smooth out the V shift to all appearances by line addition to the Y signal, and also to remove the flicker. Y signal line addition accompanies the delay and so, in the Y-ADD ON mode, the odd fields of write side are advanced by 1H.
The Y-ADD ON mode is specified by set up menu S84 : Y-ADD.
ICJ8 and J9 provide line addition for the ICJ5 output (Y signal) and ICK8 output (1H delayed Y signal). When dropouts occur in the Y-ADD ON mode, Y signal line addition is not provided and DOC is conducted.
The picture processed in the Y-ADD ON mode is natural and without flicker but when the tape speed approaches ±1 times normal speed, the picture will become defocused by the Y signal line adding and, depending on the design, an out-of-focus picture and a clear picture may appear alternately for long periods.

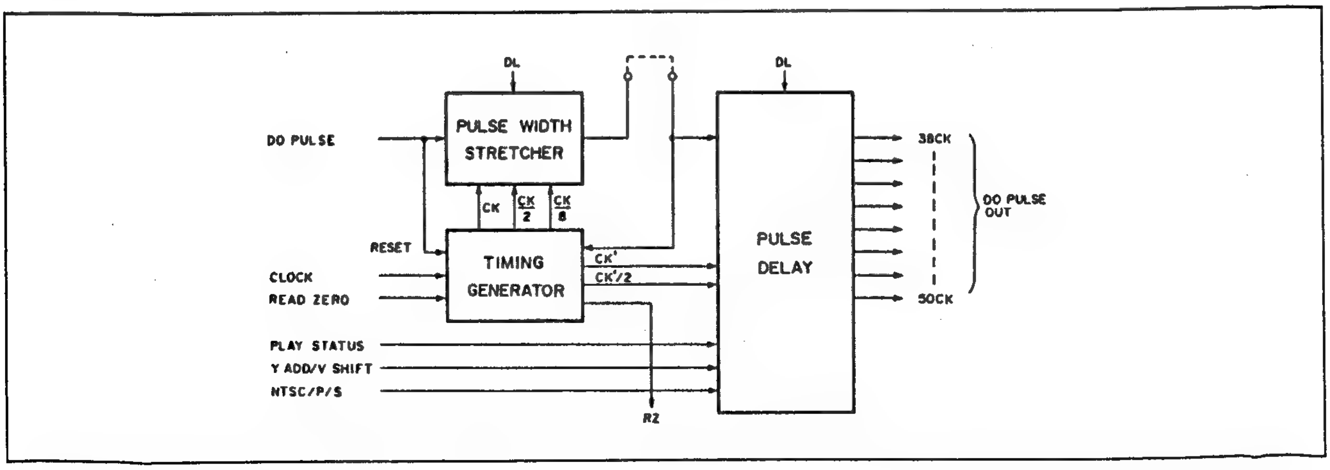


Fig. 4-4-62. Configuration of CX20219 (ICM9/PR-92)

(3) Chroma signal digital processor (PR-92 board)

(a) Chroma signal dropout compensator (PR-92 board)
Dropouts in the chroma signal are compensated for by the "partial replacement using the chroma signal of 2H before (line replacement when the dropouts occure in the burst signal)" in the PAL mode and by the "line replacement using the chroma signal of 2H before" in the SECAM mode.
Chroma signal DOC is performed by the 2H line memory (IC101 and ICG9). In other words, the data input into the 2H line memory are output immediately.
The data which are read out will be the data of 2H before and the dropout portion will be replaced by the chroma signal of 2H before.
The write line in the 2H line memory is determined by the W O/E (W D'R/D'B) signal.
The read line of the 2H line memory is the same line as the write line in the PAL mode.
In the SECAM mode, the 2H line read differs according to whether the playback mode is normal or BIDIREX. In the normal playback mode, it is the same line as the write line and in the BIDIREX mode, it is the same line as the write line or the line 1H after so as to provide line D'R/D'B alignment. When the W D'R/D'B and R D'R/D'B signals match, it is the same line as the write line and when they do not match, the line 1H after is the read line and the line D'R/D'B is aligned with the reference video signal.
In this way, the 2H line memory also functions to align the line D'R/D'B of the BIDIREX playback signal in the SECAM mode. This is in addition to its DOC function.

(b) Chroma off
When the S84 : CHROMA ON/OFF menu is set to OFF, the chroma signal is no longer output from the latch (ICK10) and the only the Y signal is output from the PR borad.
With CHROMA OFF, the chroma signal is not input to ICK10 from ICH9. In the SECAM mode, the unmodulated subcarrier provided by the SECAM ID generator (ICK9, K11, K12 and K13) is input to ICK10 and in the PAL mode, the chroma zero level data provided by the R4 and RB4 resistors are input to ICK10.

(4) Processing by individual mode (PR-92 board)

The operating modes of the TBC can be broadly classified into the NORMAL PLAY, DT, SLOW BIDIEX and FAST BIDIREX modes. The actual processing differs greatly depending on whether the playback video signal is a color signal or black-and-white signal and a PAL signal or SECAM signal.

- **NORMAL PLAY mode**
In this mode, the tape is played back at normal speed (+1×) and except when dropouts are present, the digital processor section is bypassed.
- **DT mode**
In this mode, the tape is played at any speed ranging between −1 and +3 times normal speed (except at the +1 times normal speed) using the PLAY head (DT head), and various processes are undertaken in order to yield playback which is free from guard band noise.
- **SLOW BIDIREX mode**
In this mode, the tape is played back at speeds up to ±8 times normal speed except in the NORMAL PLAY and variable play modes. The color is locked but guard band noise is produced.
- **FAST BIDIREX mode**
In this mode, the tape is played back at speeds exceeding ±8 times normal speed and the picture appears in black and white.

The signals are processed as follows in the NORMAL PLAY mode and DT/BIDIREX mode. Fig. 4-4-63 through 4-4-68 show the signal processing route in the various modes.

PAL or SECAM	NORMAL or BIDIREX	S83 CHROMA ON or OFF	S84 Y-ADD ON or OFF	Fig.
P/S	NORMAL	ON	×	4-4-63
P/S	NORMAL	OFF	×	4-4-64
PAL	BIDIREX	ON	ON	4-4-65
PAL	BIDIREX	ON	OFF	4-4-66
SECAM	BIDIREX	ON	ON	4-4-67
SECAM	BIDIREX	ON	OFF	4-4-68

(2) Y signal digital processor (PR-98 board)

(a) Y signal dropout compensator (PR-98 board)

This circuit compensates for the dropouts in the Y signal. When a dropout or dropouts have been detected, the separated Y signal is processed as follows. Dropouts are detected on the CK board and supplied to the PR board as the Y DO and C DO signals.

When dropouts occur, the Y signal which has been 1H delayed by ICJ6 is returned to selector ICJ7 and J8 so that it is further 1H delayed by ICJ6. The resulting 2H delayed Y signal is added by line adder ICK7 and K8 to the Y signal whose delay has been adjusted by ICJ5 and J6. As a result, the dropouts are compensated for.

The Y DO detection signal is applied to the select pin of selector ICJ7 and J8, while it is inverted by ICK4 and OR-ed with the signal which has been 1H delayed by ICM16. The OR-ed signal is supplied to the select pin of the line adder. When dropouts have occurred over a multiple number of lines, the interim lines and final line are respectively processed as follows in accordance with the processing of this detection signal. The interim dropout lines are replaced by the Y signal of the line before that in which the dropout has occurred. The final dropout line is replaced by the signal which is produced by adding the Y signal of the line before that in which the dropout has occurred to the normally returned line Y signal.

When no dropouts are detected, the Y signal is delayed by 1H+5 clocks and it is then output.

(b) Y field interpolator (PR-98 board)

Using the reference signal and playback signal field coincident/non-coincident information, this circuit conducts field interpolation from the Y signals equivalent to 4 lines and it improves the picture quality in the DT playback and STILL modes.

The Y signal is delayed 1H each by ICK9, L10 and L11. The factors corresponding to the amounts of the delay are applied by ROMs ICK10, J11, K11, L14, L13 and L12 to the delayed Y signal and, in accordance with the combinations shown in the figure, they are added by line adders ICJ12/K12, J13/K13 and J14/K14. As a result, field interpolation is conducted using the data of 4 lines each in all.

The Y ROM A9 and Y ROM A8 signals which switch the factors of the ROMs represent information relating to whether the reference signal and playback signal fields coincide or not and whether the fields should be interpolated.

[Y ROM A8] 0: Field coincident 1: Field non-coincident
[Y ROM A9] 0: No interpolation 1: Interpolation

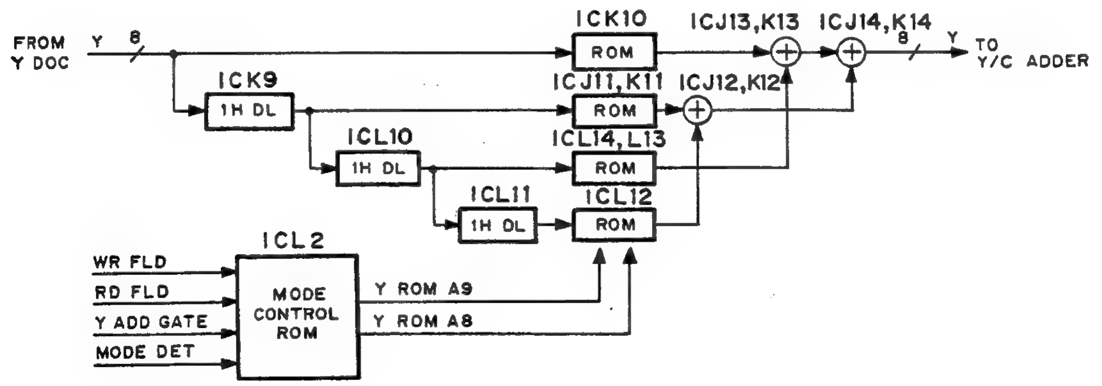


Fig. 4-4-72. Y Field Interpolator (PR-98)

4-4-12. Analog Processor (PR-98/92 Board)

The anfalog processor block contains a processor circuit, which controls the video level, chroma level and black level (PAL signals only) with the Y D/A converter and also which adds both the reference sync signal and the reference burst signal (PAL signal only) to these video signals.
In the FAST BIDIREX mode over ±8 times normal tape speed, the video signals in both the PAL and SECAM mode are restricted to a 2.5MHz band, the chroma signal is cut out and a monochrome signal is output.
The C phase corrector is a circuit which processes the chroma signals in the PAL BIDIREX mode.

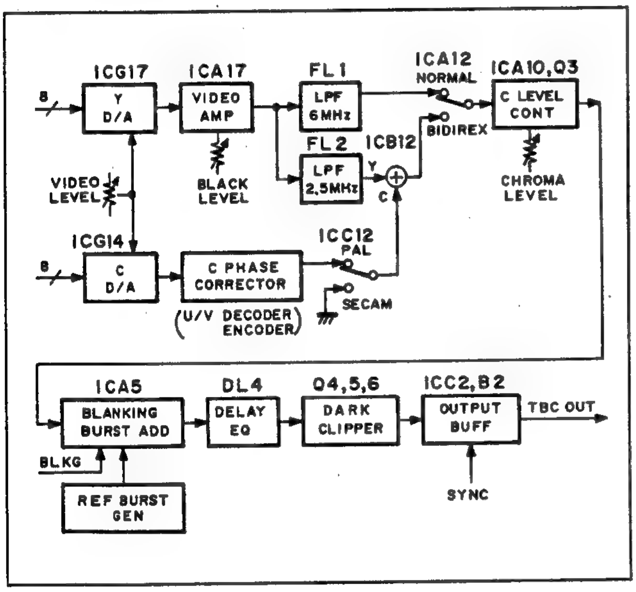


Fig. 4-4-73. Outline of Analog Processor (PR-98/92)

(1) D/A converter (PR-98/92 board)

The Y D/A converter converts the digital output of the digital processor circuit into an analog signal. The input of this converter is delayed by ICJ18 and J19 (or ICJ16 on the PR-92 board) in clock pulse units equivalent to the time required for chroma signal processing. The Y D/A output signal is a composite signal in both the PAL and SECAM modes.
The C D/A converter provides D/A conversion for only the Y/C separated chroma signal. The input of this converter is delayed in clock pulse units by ICK16 and J17 (ICG11 and H12) in order to align the Y/C delay of the PAL BIDIREX playback signal. The phase of the C D/A output signal is compensated in the PAL DT/BIDIREX playback mode.
Both output levels of the Y D/A and C D/A converters are adjusted by the VIDEO LEVEL control. The adjustment is made in order to adjust the video levels of TBC OUT and TBC NON COMP.

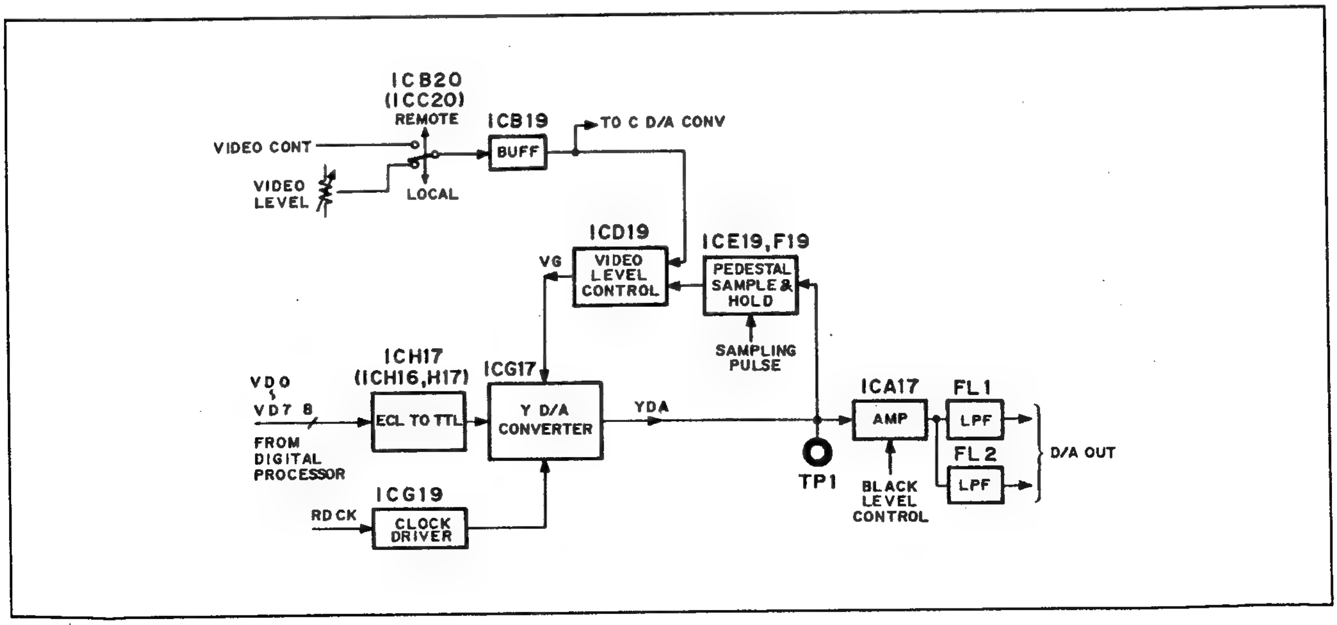


Fig. 4-4-74. Y D/A Converter (PR-98/92 board)

(2) LPF and mode switching circuit (PR-98/92 board)

In the normal playback mode, the frequency response of the Y D/A output signal is first compensated by ICA17, the signal is then interpolated by FL1 (6 MHz low-passfilter) and sent to the ICA12 switcher. Mode switching circuit ICA12 is set to NORMAL in the following modes; in all other modes, it is set to BIDIREX.

PAL • COLOR • PLAY STATUS
+ (SECAM+B&W) • $\overline{\text{FAST BIDIREX}}$

In the PAL BIDIREX playback mode, the band of only the Y signal of the video signal output from ICA17 is restricted by FL2 (2.5 MHz low-pass filter), the chroma signal whose color field sequence has been corrected at the input side of ICB12 is then added to the resulting signal, and the signal is then sent to the ICA12 switcher.
In the FAST BIDIREX mode, the Y signal whose bandwidth is restricted by FL2 is sent to ICA12 without chroma signal adding, because the chroma signal is prohibited in the C phase corrector circuit.

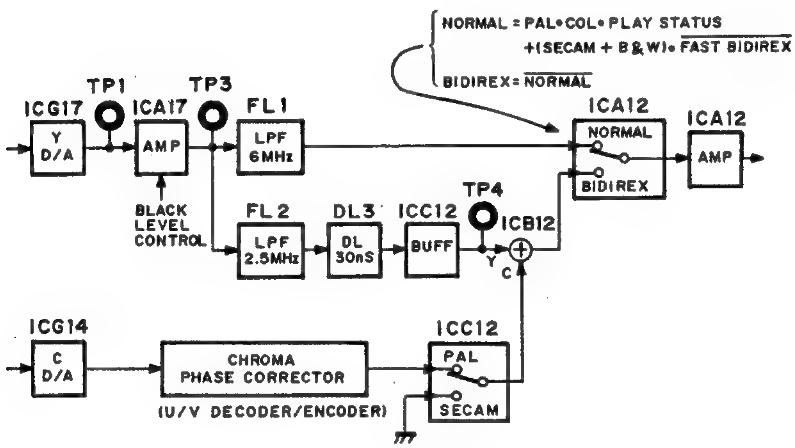


Fig. 4-4-75. LPF and Mode Switching Circuit (PR-98/92)

(3) Chroma level and black level control circuit (PR-98/92 board)

The chroma level control circuit is composed of delay line DL2, linear multiplier ICA10 and chroma component adder Q3. The amount of delay in the delay line is 1/2 fsc sec. This means that when the video signal which passes through the delay line is subtracted from the video signal containing the reflection component of the delay line, only the chroma components will be output from ICA10. The level of these chroma components depends on the voltage applied to pin 8/YIN (−) of ICA10. Consequently, when the ICA10 output is added to the video signal (FL3 output), the result will be a video signal whose chroma level has been adjusted by the CHROMA CONT voltage. Low-pass filter FL3 functions as a delay line for aligning the timing.
When changing the shorting plug position from JP10 to JP9, the chroma level control can be possible in the SECAM mode.
Fig. 4-4-77 shows the frequency response of the chroma level control circuit.
The black level control circuit comprises a feedback loop stretching from Q3 to ICA17. ICB18 controls the offset of ICA17 so that the pedestal level of the Q3 output will follow the SET UP CONT voltage applied to ICB18.

The respective remote/local control modes are selected using the "I83. CHROMA LEVEL" and "I82. BLACK LEVEL" initial set-up menus.
In the SECAM mode, the black level control voltage is switched off by ICD18 and black level control does not function.

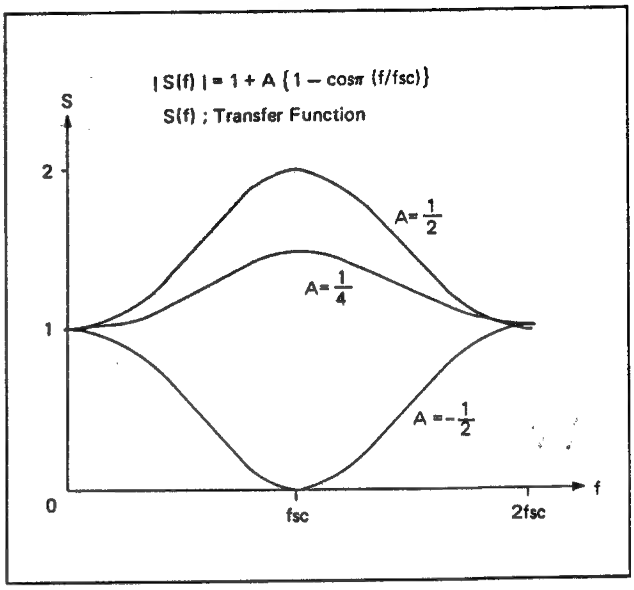


Fig. 4-4-77. Frequency Response of Chroma Level Control Circuit

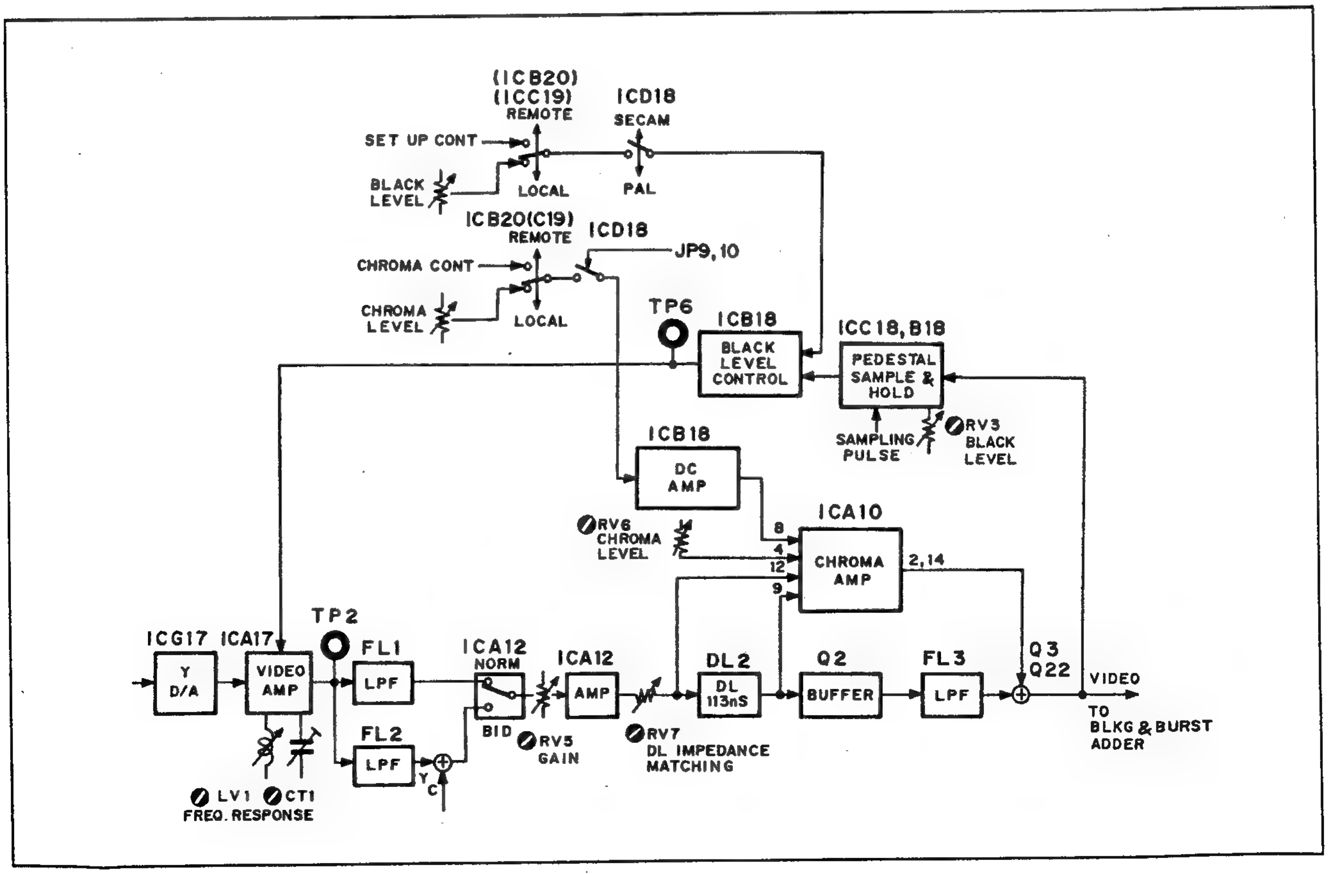


Fig. 4-4-76. Chroma Level and Black Level Control Circuit (PR-98/92)

(4) Blanking/burst adder, Y/C delay adjustment and dark clipper (PR-98/92 board)

The video signal, whose chroma level and set-up level have been controlled, is now supplied to switcher ICA5. The reference burst signal is supplied to the other input pin of the switchers. The reference burst signal is added at the same time as blanking is applied by selecting these switchers using the blanking signal.
The output of the blanking/burst adder circuit is fed to the Y/C delay adjusting circuit consisting of S1, S2 and DL4. The Y/C delay is adjusted by using group delay of the delay equalizer (DL4) so that the adjustment of 7 nsec per one step accuracy can be carried out by the selection of S1 and S2.
However, when Y/C adjustment will be performed using this circuit, the burst phase also varies, consequently, it is necessary to perform the SC/H phase adjustment again.
The dark clipper is a circuit consisting of Q4, 5 and 6 as well as bandpass filter BPF1. The video signal, to which the reference burst signal has been added, is applied to one base of Q4 and to the other base is applied only the chroma components which have passed through the bandpass filter. This means that the signal clipped below the pedestal level and excluding the chroma components is output to the emitter of Q4. Q5 and 6 function to stabilize the operating point of Q4, enabling the Q4 gain to be compensated during the clipping operation.
An example of how this circuit operates is shown in Fig. 4-4-79.

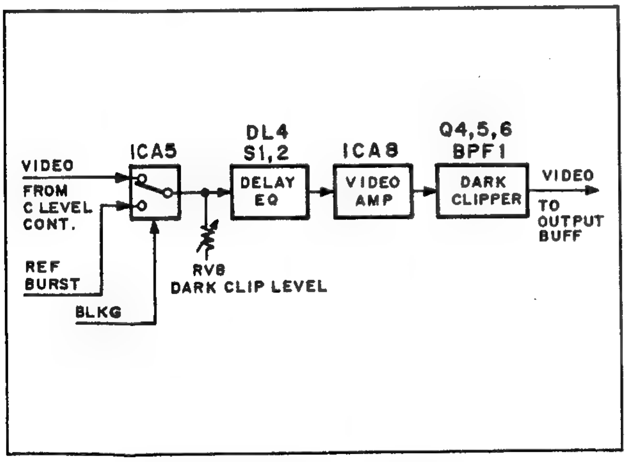


Fig. 4-4-78. Blanking/Burst Adder, Y/C Delay Adj. and Dark Clipper (PR-98/92)

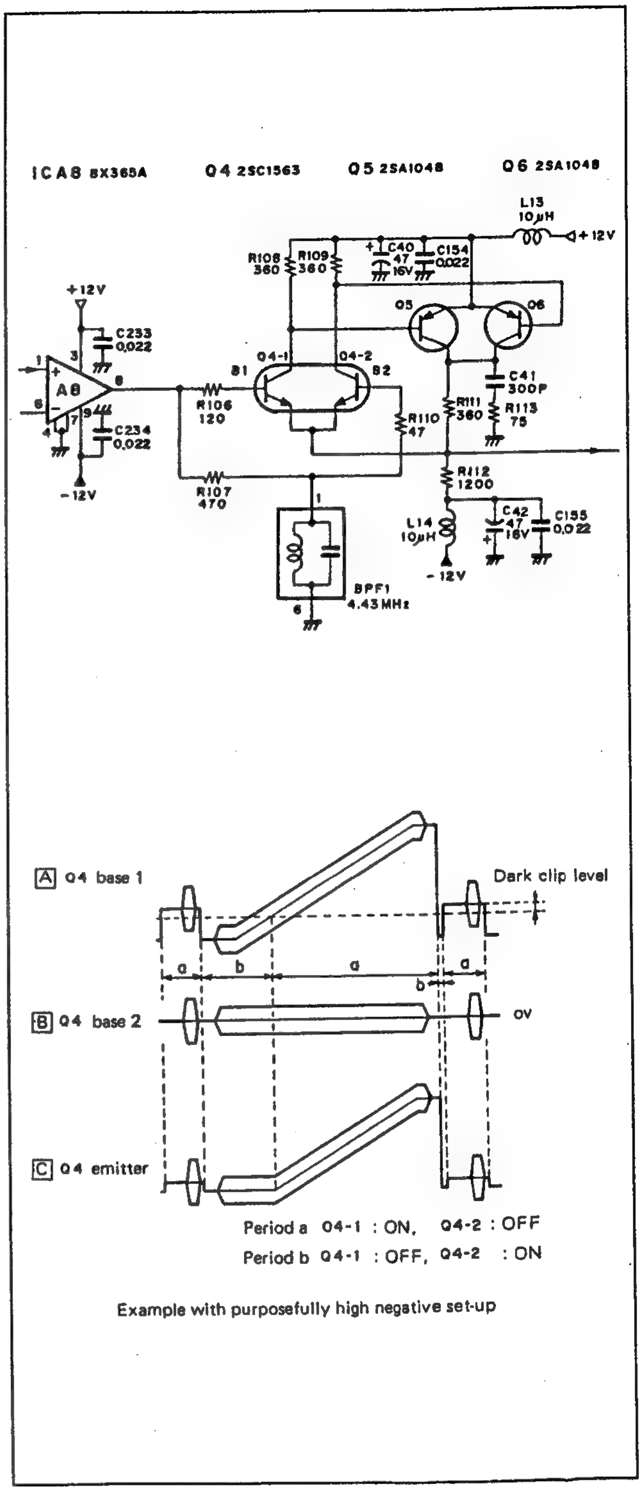


Fig. 4-4-79. Dark Clipper Operation (PR-98/92)

(5) Reference burst generator (PR-98/92 board)

The reference burst signal is generated from the RD Fsc signal which is gated by the burst gate signal created from the BURST FLAG signal. After its band has been limited by the bandpass filter, it becomes the reference burst signal.
Whether or not the burst signal is to be added to the VTR output depends on the setting of the "I89. BURST" initial set-up menu.
In the SECAM mode, the BF signal input is prohibited and the reference burst signal is not output.

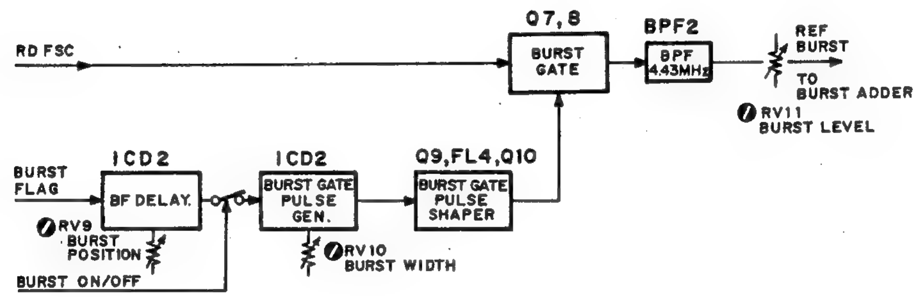


Fig. 4-4-80. Reference Burst Generator (PR-98/92)

(6) Output video buffer and sync adder (PR-98/92 board)

IC C2 and B2 are output buffers. At the output side of each buffer is added the sync signal which is generated from the TBC SYNC signal. The amplitude of the TBC SYNC signal which is applied to Q11 is adjusted by RV12, the waveform of the signal is then shaped by low-pass filter FL5, and then the signal is added to the respective buffer outputs by Q12, 13 and 14. The switching operation of Q13 and Q14 is turned on or off by the "S81. COMP/NON COMP" select menu, which enables the COMP or NON COMP mode for VIDEO OUT 3 to be selected.

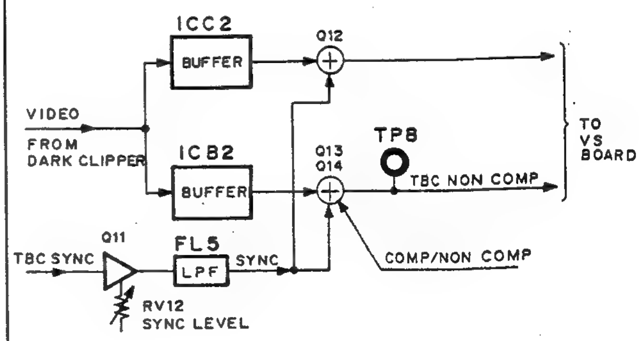


Fig. 4-4-81. Output Video Buffer and Sync Adder (PR-98/92)

(7) Chroma signal phase corrector (PR-98/92 board) (PAL U/V decoder/encoder)

The chroma signal phase corrector circuit is a circuit which processes the chroma signals in the PAL signal BIDIREX mode. Among other circuits, it consists of the PAL U/V separator circuit, decoder, encoder, and decode/encode carrier generator.
In the PAL BIDIREX mode, the phase of the chroma signal sent from the CK-27 board dose not match that of the reference signal.
In order to bring the chroma signal into alignment with the reference signal, the chroma signal phase corrector circuit generates a decode carrier synchronized to the C D/A output signal, and that decode carrier is used to decode the C D/A output signal. Next, the decoded signal is encoded using a carrier synchronized to the reference signal.
In the FAST BIDIREX mode, the encode carrier is not generated and the chroma signal is set off.

(8) U/V separator (PR-98/92 board)

BPF3 serves to filter out only the chroma components from the C D/A output signal. The level of the BPF3 output is adjusted by RV13 so that the level of the signal input into the decoder circuit is made uniform, and then its phase is adjusted by RV14 so that it coincides with the decode carrier in the DT mode.
The U components are obtained by adding the 1H delay signal delayed by DL1 and the signal which is not 1H delayed (ICD13 output) in the U/V separator circuit, and the V components are obtained by subtracting these two signals in the same circuit.
The phase inverter circuit composed of Q17 and ICD13 is designed to invert the chroma phase so that the U/V separation can be conducted properly even when the main memory output has jumped by 2H due to an excessive WINDOW in the main memory.

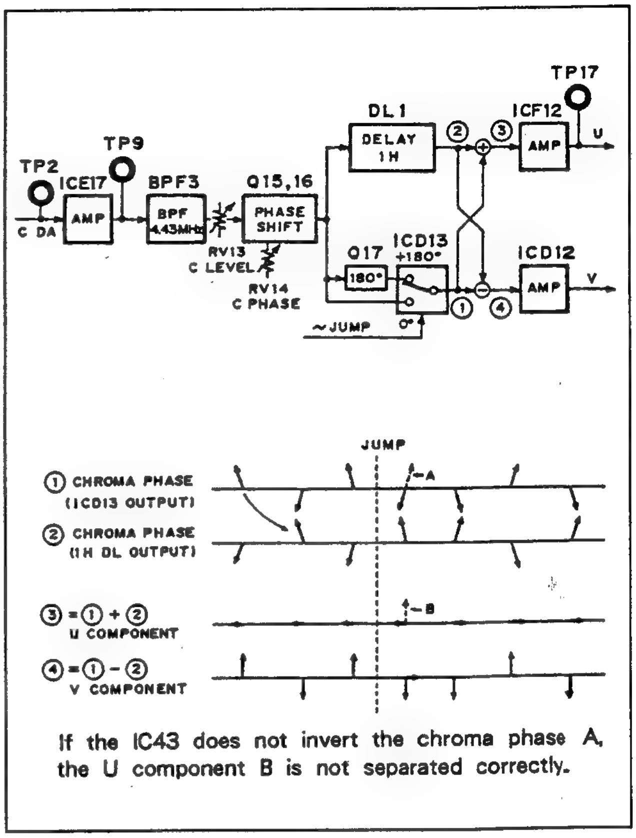


Fig. 4-4-83. U/V Separator (PR-98/92)

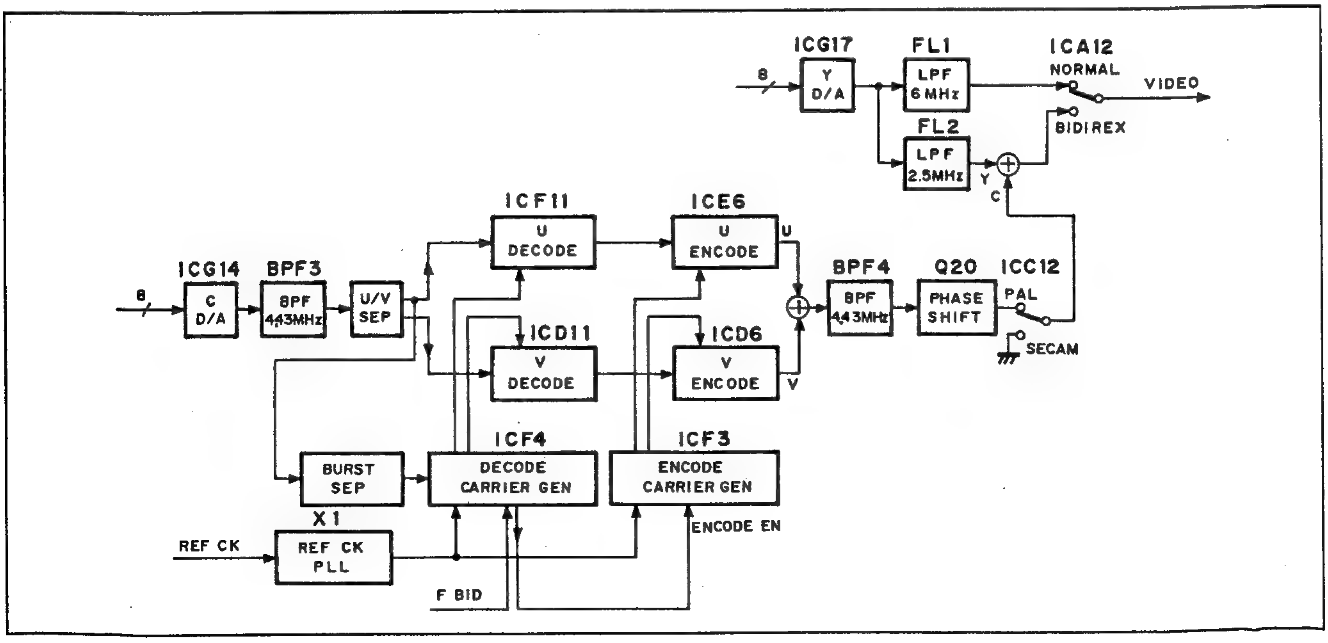


Fig. 4-4-82. Chroma Phase Corrector (PR-98/92) (PAL U/V Decoder/Encoder)

(9) U/V decoder (PR-98/92 board)

The U/V separated signals are decoded by the decode carriers in ICF11 and ICD11 respectively, the signals pass through the FL7 and FL6 low-pass filters, and base band chroma signals are obtained.
The decoded chroma signal is clamped to 0V, with the digital blanking section serving as the reference. ICE7 and ICE9 make up the clamp circuit for the V components while ICF7 and ICE9 make up the clamp circuit for the U components.

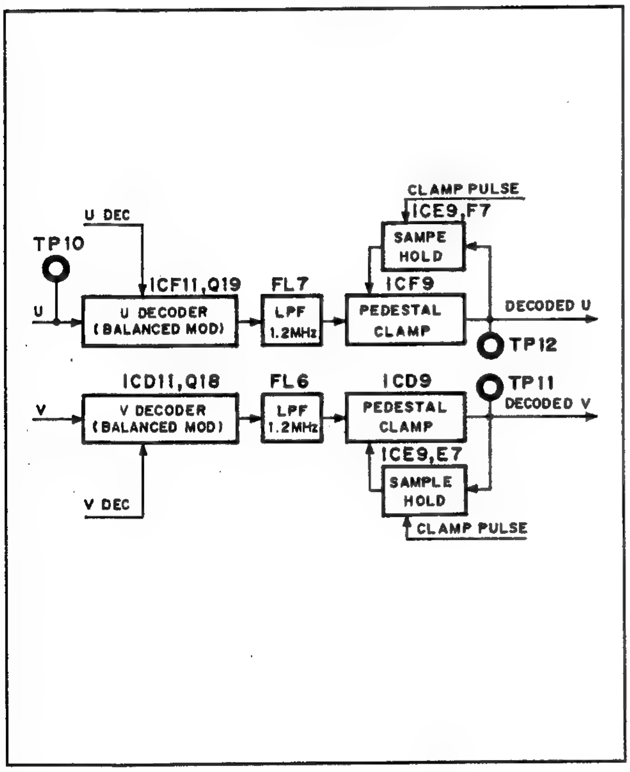


Fig. 4-4-84. U/V Decoder (PR-98/92)

(10) REF CK PLL (PR-98/92 board)

With the REF CK signal sent from RD-7 board serving as the reference, the REF CK PLL circuit provides an Fsc clock or 4Fsc clock signal which serves as the reference for the encode or decode carrier.
REF CK is the Fsc clock signal which is not subject to velocity error phase modulation but which is subjected to SC phase and Burst-Chroma phase control. The Y/C delay in the BIDIREX mode is adjusted by varying the amount of delay in the chroma signal system in single 4Fsc clock units by means of JP1 and JP2. This adjustment has the effect of varying the CDA signal phase in 90° steps, and ICH2 is a circuit for varying the phase reference of the decode carrier in accordance with these phase fluctuations.

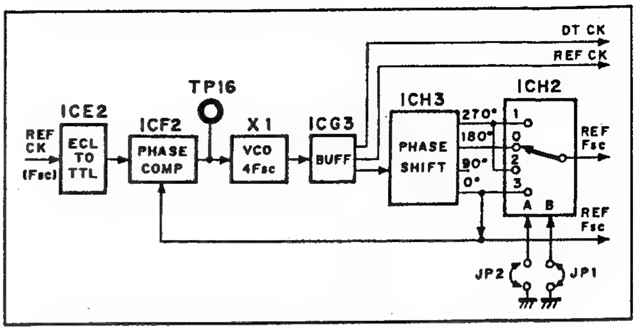


Fig. 4-4-85. REF CK PLL (PR-98/92)

(11) Decode carrier generator (PR-98/92 board)

The decode carrier is provided by ICF4 but the way in which it is provided differs depending on whether the mode is SLOW BIDIREX or DT.

SLOW BIDIREX mode

In the SLOW BIDIREX mode, the playback burst signal is written into the main memory. The decode carrier is provided using this burst signal.
The U/V separated U component signal passes through Q21, it is turned into a binary value by ICF5 and then input into ICF4 as the WSC signal. Using the WSC signal and clamp pulse (H SYNC), one cycle of the U component in the burst signal is taken out by ICF4.
This is called the RESET signal. The shuttle decode clock generator composed of ICE3 employs this RESET signal as the voltage-controlled oscillator (VCO) reset pulse, and the output phase of this VCO is locked to the phase of the U component in the burst signal. The frequency of the VCO output (4Fsc) is divided down by 4 in ICF4 and the U-axis decode carrier UDEC is created as a result.
ICG4 functions to control the phase in 90° steps when the frequency is divided down by 4, and the V-axis decode carrier is also produced by this control. The phase of the V-axis decode carrier is advanced by 90° over the phase of the U-axis decode carrier.
The frequency of the VCO in the shuttle decode clock generator is stabilized by first comparing the phases of the UDEC and REF FSC signals during the VD period by ICF4, passing the resulting error voltage through ICD5 to the D10 varicap diode and then locking the oscillation frequency of the VCO to a value equivalent to four times the REF FSC frequency.

DT mode

As with the normal playback signal, the DT playback signal is subject to the time base correction processing. Consequently, the video signal of the D/A output is time-base-corrected at a high degree of

precision even in the DT mode.
However, since any field is played back with DT playback, the color field sequence of the playback signal becomes discontinuous, the phase of the D/A output chroma signal is shifted by 90° with respect to the phase of the reference signal, and the V-axis swing sequence is reversed.
As a result, the decode carrier in the DT mode is produced not by a method that uses the playback burst signal as in the SLOW BIDIREX mode but by a method that modulates the phase of the REF FSC signal, which is the REFERENCE SC signal, in 90° steps in accordance with the state of the D/A output chroma phase.
The state of this phase is identified by comparing the W O/E and W N/I signals which indicate O/E and N/I of the playback signals with the R O/E and R N/I signals which indicate O/E and N/I of the reference signal. This comparison and the results are sent to the PR board as the OEDC and NIDC signals.
Based on these OEDC and NIDC signals, the phase control signals UOE, UNI, VOE and VNI for producing the U-axis and V-axis decode carriers are produced themselves by the O/E and N/I decoders composed of ICL4 and K5 (or ICL15 and M11 on the PR-92 board). These signals are sent to ICF4 for phase modulation with the REF Fsc signal produced by the REF CK PLL circuit. The REF Fsc signal whose phase is modulated by the UOE and UNI signals becomes the U-axis decode carrier while the REF FSC signal whose phase is modulated by the VOE and VNI signals becomes the V-axis decode carrier.

(12) Encoder (PR-98/92 board)

The decoded U and V components are first encoded by ICE6 and ICD6 and then added together to form the chroma signal whose color sequence is made to coincide with that of the reference video signal. The bandwidth of the added chroma signal is restricted by the BPF4 bandpass filter and it then enters the chroma phase shifter. The chroma phase shifter is a circuit for adjusting the chroma phase of the Burst-Chroma phase, and RV19 is used for the actual phase adjustment.
The chroma phase shifter output is added to the Y signal via ICC12. O/E detector ICD7 is a voltage comparator for detecting the direction (O/E) of the V axis in the shuttle mode.

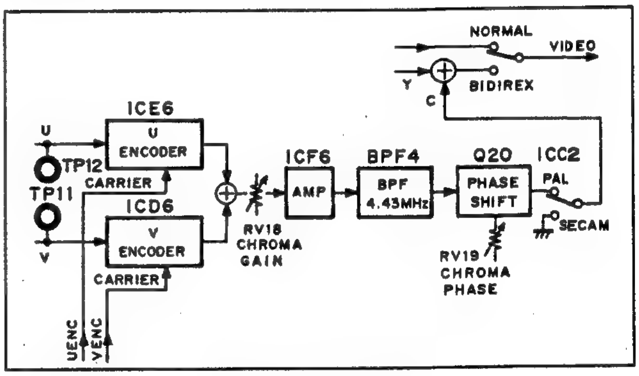


Fig. 4-4-87. Encoder (PR-98/92)

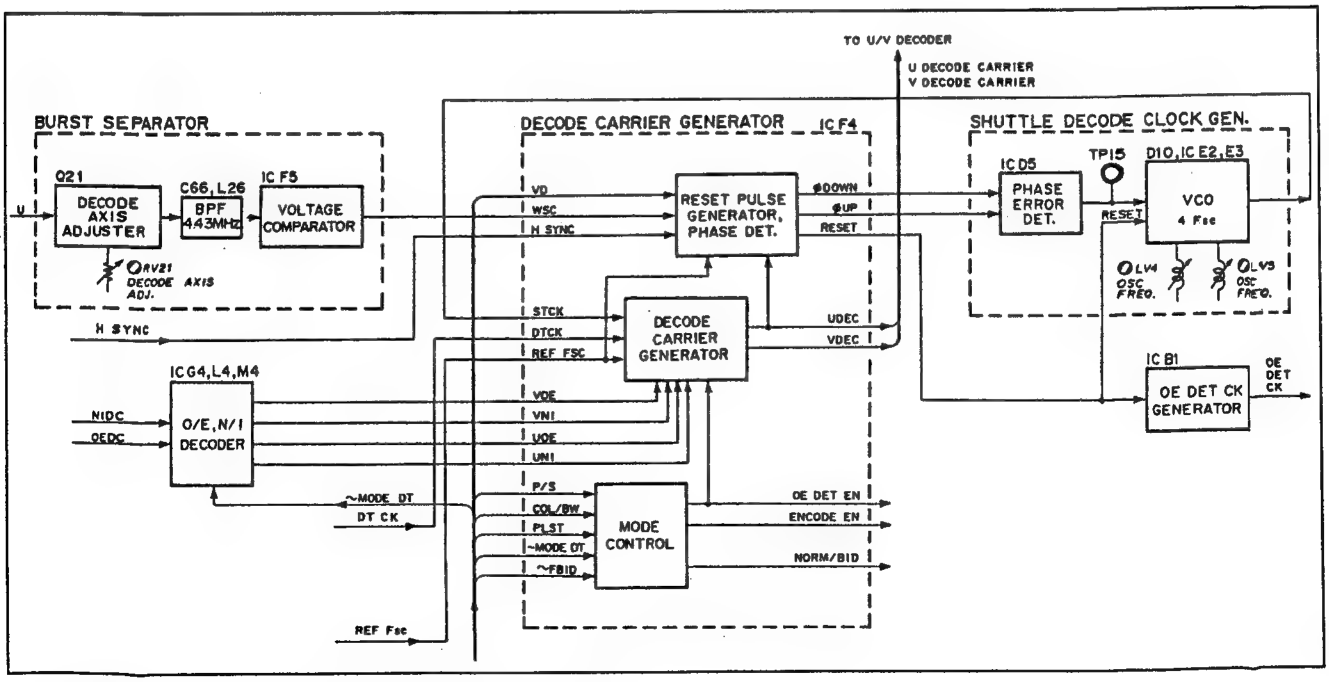


Fig. 4-4-86. Decode Carrier Generator (PR-98/92)

(13) Encode carrier generator (PR-98/92 board)

The encode carrier is produced by ICF3 using the REF Fsc signal as the reference, but the way in which it is produced differs depending on whether the mode is SLOW BIDIREX or DT.
The I/O3 and I/O4 signals of ICF3 are the mode switching signals of the encode carrier. The I/O3 signal is for switching between the DT and SLOW BIDIREX modes.
In the PAL•COLOR•SLOW BIDIREX mode, the SLOW BIDIREX encode carrier is produced ; in the other modes the DT encode carrier is produced.
The I/O4 signal is for stopping the encode carrier output. In the PAL•COLOR•(SLOW BIDIREX+DT) mode, the encode carrier is output; in any other mode, it is not output.

DT mode
In the DT mode, U-axis encode carrier UENC is produced by delaying the REF Fsc signal phase by 90° . V-axis encode carrier VENC is produced in-phase with the REF Fsc signal.
O/E conversion of the chroma phase in the DT mode is performed by inverting the phase of the V-axis decode carrier at the decode side. Consequently, the V-axis encode carrier phase is constant at all times.

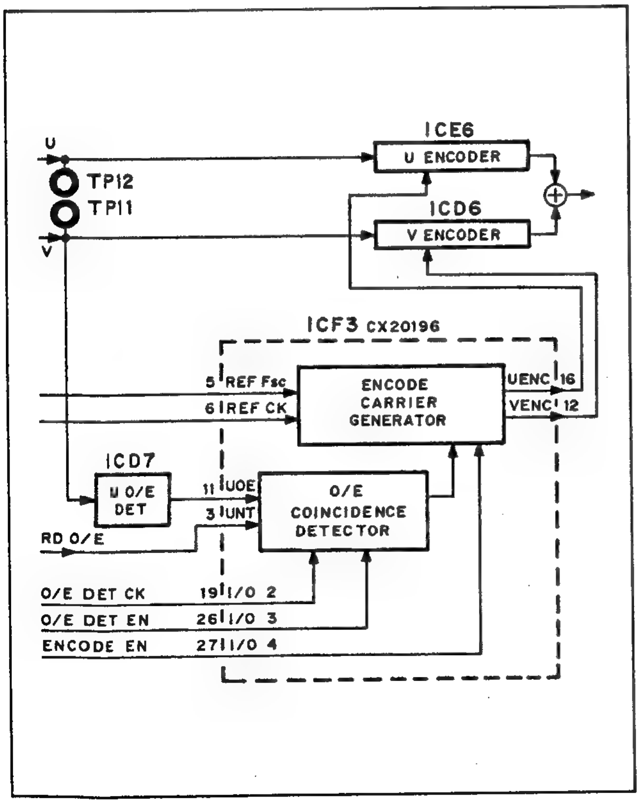


Fig. 4-4-88. Encode Carrier Generator (PR-98/92)

SLOW BIDIREX mode
In the SLOW BIDIREX mode, U-axis encode carrier UENC is produced in the same way as in the DT mode.
V-axis encode carrier VENC is produced in-phase with the REF Fsc signal when the UOE signal detected by the ICD7 voltage comparator coincides with the UNI signal which is the O/E information of the reference signal. If the signal does not coincide, it is produced by inverting the REF Fsc signal phase. By inverting the phase, the color field sequence of the playback signal is made to coincide with that of the reference video signal.
Fig. 4-4-89 gives an example of O/E conversion in the SLOW BIDIREX mode.

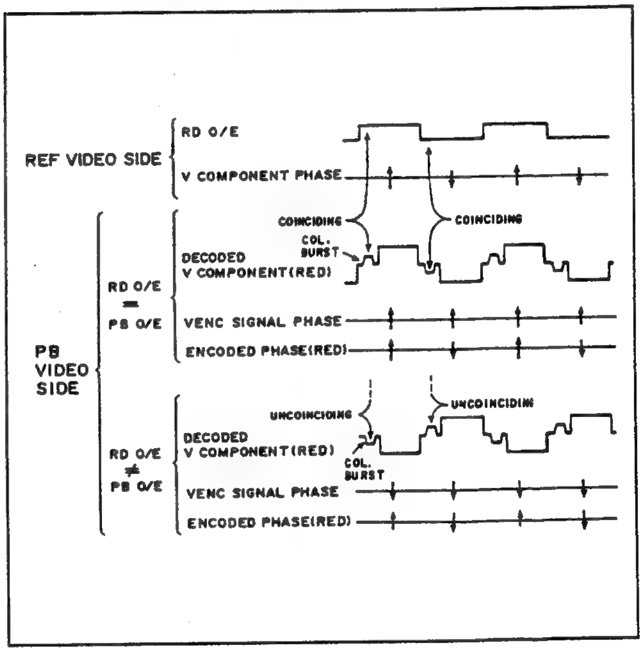


Fig 4-4-89. O/E Conversion : SLOW BIDIREX Mode

4-5. DT SYSTEM

4-5-1. Outline of DT System (RD-6/RD-7 Board)

Note 1 :
The DT system of BVH-3000/3100 employs the RD-6 board for NTSC model and the RD-7 board for PS model. The reference numbers that are given to respective parts and components are different in the RD-6 board and in the RD-7 board. Therefore, the reference numbers for the RD-6 board/NTSC model are shown first and those for the RD-7 board/PS model are shown in parentheses.

Note 2 :
RD-6 board and RD-7 board have currently three types respectively, having the part numbers' last two digits of "-11", "-12" and "-13". The same circuit components sometimes have the different reference numbers in the "-11/-12" and "-13". In order to avoid confusion, the reference numbers for the RD-6 board and the RD-7 board ending by "-13", are omitted in the subsequent description.

Note 3 :
The circuit compositions of the "-11" version and the "-12" version of the RD-6 board and the RD-7 board, are mostly same. The "-13" version has the following additional functions that are not found in the "-11, -12" versions.
- Ringing amount detector
- Wobbling phase shifter
- Filter during DT OFF period
- Feedback gain suppressor during INTEG OFF period

The DT system of BVH-3000/3100 has the most distinguished point in its microprocessor system where most of DT system controls are performed by the microprocessor. The changes in the DT head characteristics and the changes in tape properties are automatically compensated by the microprocessor. Amount of jump that has been frequently adjusted in the conventional type, becomes automatic control and the optimum control for the DT head transient response becomes possible.
The signals that are supplied from other circuit boards for DT head control, are listed as follows.

From VO board
- PB V : PB V signal
- PB H : PB H signal
- RF ENV : PB RF envelope signal

From CK board
- FHX : PB H signal (AFC output)

From DD board
- ST GAUGE : DT head operation information

From SV board
- ~RD INT 2 : 32×V signal
- ~RESET : Reset signal for CPU
- PB WINDOW : Window of the PB V signal
- REF ADV V : Phase information of the REF V signal
- SV A0-SV A5 :
- SV D0-SV D7 :
- ~RD CS :
- ~SV RD :
- ~SV WR :

(SV A0-SV A5 through ~SV WR: CPU control information)

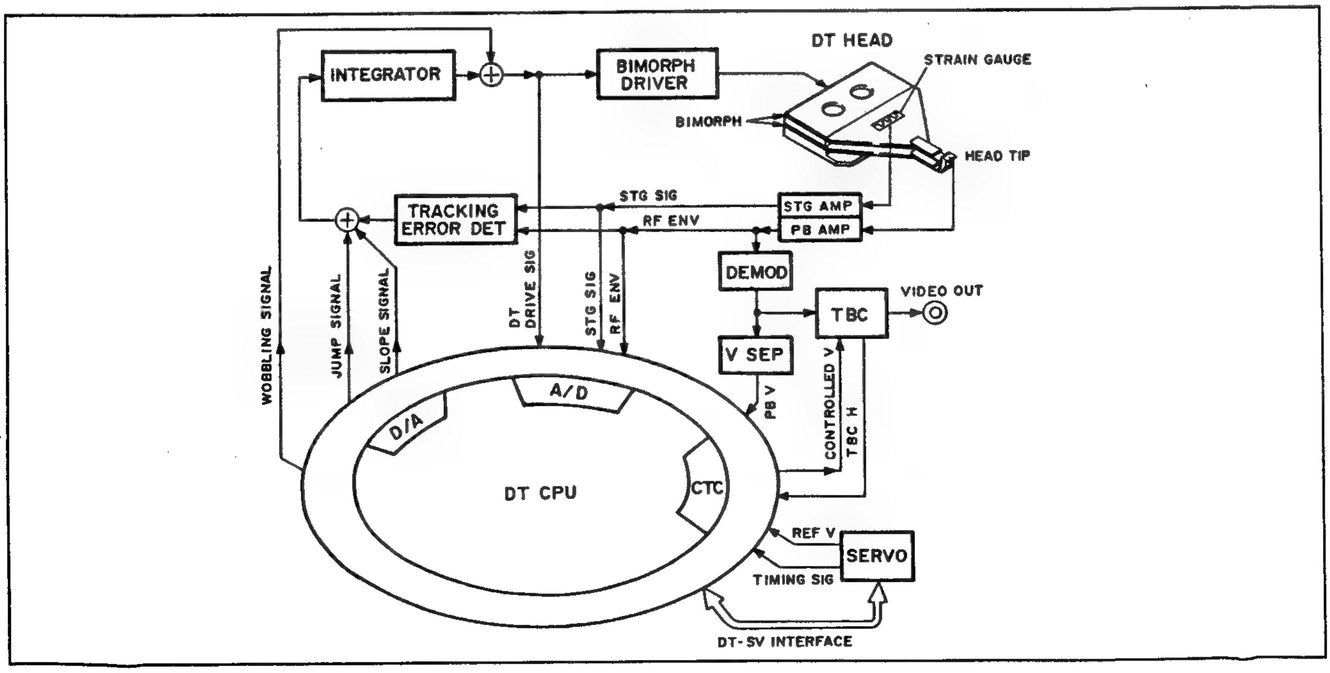


Fig. 4-5-1. BVH-3000/3100 DT System

4-5-2. DT CPU (RD-6/RD-7 Board)

(1) Outline of CPU (RD-6/RD-7 board)

ICL20 (ICM18) μPD78C10G is the CMOS 8-bit CPU that has built-in 16-bit ALU, 256 bytes RAM, 8-bit A/D converter, multi-function 16-bit timer/event counter, two 8-bit timers and general purpose serial interface. This CPU is also capable to make direct addressing to external memories of maximum 64k bytes.

The clock signal is the 12 MHz that is generated by the ceramic resonator (X1), realizing the minimum command execution time of 1 μsec. As its external memories, the ICL15 (ICM14) 8k bytes EPROM and ICM16 (ICN15) 2k bytes SRAM are employed. The power voltage of SRAM is backed up by ICN22 (ICM21) and battery so that the data can be kept memorized even while the power is turned off.

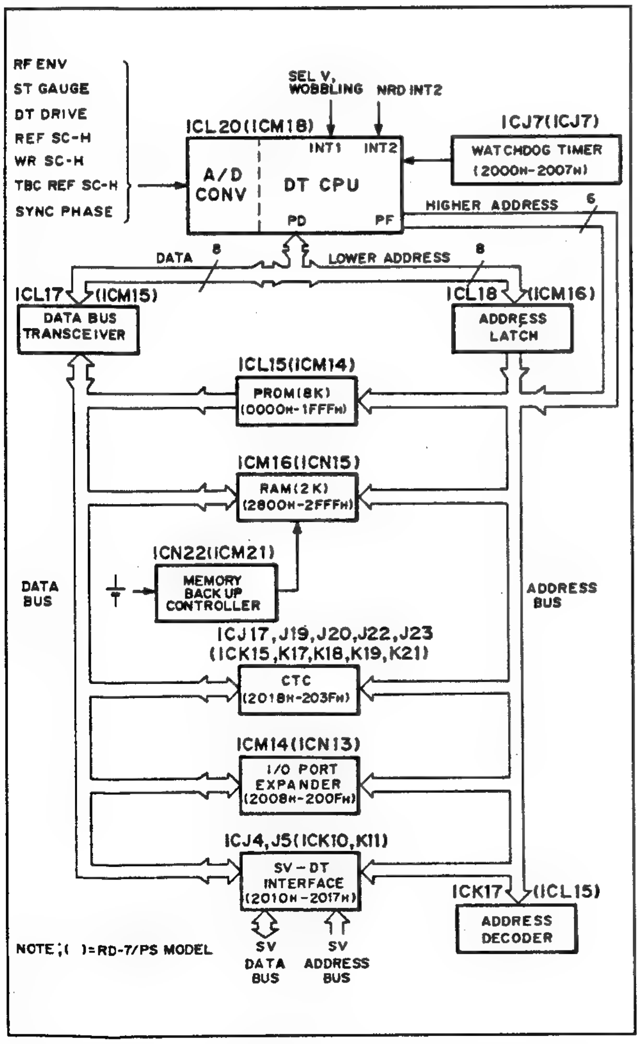


Fig. 4-5-2. CPU Peripheral Circuit (RD-6/RD-7)

The ICM14 (ICN13) I/O port expander is securing the ports equivalent to 4.5 bytes. Various measurements are performed by five CTC (programmable timer counter) ICJ17, J19, J20, J22, J23 (ICK15, K17, K18, K19, K21). These programmable timer counters are those of 3×16 bits, capable to measure in six modes of operation that are controlled by CPU. Clock frequency of up to 8 MHz can be used. The vertical information and wobbling information are input to pin 26 (INT1 terminal) of CPU while the "~RD INT2" signal is sent from the SV board to its pin 20 (INT2 terminal), as the external interrupt signal to the CPU. The "~RESET" signal that is supplied from SV board, is passing through ICL14 (ICL12), and is input to its pin 28 (RESET terminal) as CPU reset signal. By this reset signal, if the power supply voltage becomes lower than approximately 4.5V or when the power is turned on/off, the CPU is automatically reset. The DT CPU is interfaced to the SV CPU on the SV-90 board through ICJ4 and J5 (ICK10 and K11) 4×4-bit memories.

The DT CPU is functioning not only as the DT head controller but also controlling the detection of the servo reference SC-H phase, tape SC-H phase, SV CF detection.

(2) Address/data separator (RD-6/RD-7 board)

Because the transmission and reception of data D0 through D7 and the output of lower addresses A0 through A7 are commonly sharing the port D (PD0 through PD7) in the ICL20 (ICM18) CPU, data and address are separated by the ICL18 (ICM16) address latch and the ICL17 (ICM15) bus transceiver. The lower addresses that are output from the address latch, are added to the upper addresses (A8 through A13) that are output from port F (PF0 through PF7), becoming the 14-bit address bus. At the same time, the signal that has passed through bus transceiver, becomes the 8-bit data bus. The ICK17 (ICL15) is the address decoder that is generating the write address.

(3) Watch dog timer (RD-6/RD-7 board)

The ICJ7 (ICJ7) monostable multivibrator is functioning as a watch dog timer that generates approximately 2 msec pulse by the write pulse. The write pulse is input to the watch dog timer in every 1/32 field (approximately 520 μsec in NTSC model, and 625 μsec for the PAL/SECAM model). The Q output of ICJ7 is kept to "H" level normally, but it will go into "L" level if the CPU should run-away, so that the CPU should be reset.

(4) Memory back-up circuit (RD-6/RD-7 board)

The ICN22 (ICM21) is the back-up controller for the ICM16 (ICN15) SRAM, that is monitoring the +5V power supply voltage at all times. If the power supply voltage becomes approximately 4.5V or less, the chip enable terminal of ICM16 (ICN15) is set to "H" level so that write operation is inhibited, and at the same time the power supply to the SRAM is switched to the battery. The ICN22 (ICM21) detects the battery output voltage when the power is turned on. When the battery output voltage is lower than 2.0V, the second memory cycle is prohibited so that check becomes possible.
The lithium battery of 180 mAH is employed. When the TC5517AFL SRAM consumes the maximum consumption current of 1 μ A in standby mode, and the DS1210 back-up controller consumes 1 μ A, the battery life is calculated as approximately 10 years. If two times tolerance is considered, it becomes approximately 5 years.

(5) I/O port expander (RD-6/RD-7 board)

The ICM14 (ICN13) I/O port expander is equipped with the four sets of 8-bit I/O port where input and output can be assigned in 4-bit unit, and one set of 4-bit I/O port where input and output can be assigned in 1-bit unit. The following signals are assigned to the CPU and I/O port expander.

CPU port assignment : ICL20 (ICM18)

PIN	I/O	SIGNAL
1 : PA0	I	REF FRAME
2 : PA1	O	Δf GATE
3 : PA2	I	IN-PHASE DETECTOR (H : IN-PHASE)
4 : PA3	O	PB V SELECTOR (H : PB V)
5 : PA4	O	SG OFF (H : ON)
6 : PA5	O	INTEG OFF (H : OFF)
7 : PA6	O	DT DRIVE SELECTOR (H : ON)
8 : PA7	I	PB V
9 : PBO	I	BURST DETECTOR············RD-7/PS
10 : PB1	O	RINGING OFF (H : OFF) ····13 board
11 : PB2	O	SC-H/RING (H : SC-H) ·······13 board
12 : PB3	O	INT1 SG SELECT (H : ON) ····13 board
13 : PB4	O	DT FILTER (H : OFF)········13 board
17 : PCO	O	GREEN LED : DARK (H : ON)
18 : PC1	O	GREEN LED (H : ON)
19 : PC2	O	RED LED (H : ON)
20 : PC3	I	INT2 INTERRUPT
21 : PC4	O	CPU MONITOR
22 : PC5	O	INTERRUPT MONITOR
23 : PC6	I	WOBBLING TIMING (H : OFF)
24 : PC7	O	DT RESET (L : RESET)

I/O port expander port assignment : ICM14 (ICN13)

PIN	I/O	SIGNAL
54 : PA0	O	12-BIT D/A CONVERTER
55 : PA1	O	
56 : PA2	O	
59 : PA3	O	
60 : PA4	O	
61 : PA5	O	
62 : PA6	O	
63 : PA7	O	
64 : PB0	O	
3 : PB1	O	
4 : PB2	O	
5 : PB3	O	
11 : PC0	O	8-BIT D/A CONVERTER
| |	O	
18 : PC7	O	
20 : PD0	O	JUMP STATUS 1
21 : PD1	O	JUMP STATUS 2
22 : PD2	O	JUMP STATUS 3
49 : PX0	O	SV CF
50 : PX1	O	CF RESET
52 : PX2	I	TEST SWITCH
53 : PX3	O	OUT SC-H (L : ON)·······RD-6/NTSC 3-FIELD RESET (H : EVEN)RD-7/PS

(6) Interrupt process (RD-6/RD-7 board)

Most of the data processing by the CPU, is carried out by interrupt using the "~RD INT2" signal that is supplied from the SV-90 board. The "~RD INT2" signal is the signal that is obtained by dividing one field into 32. It means that interrupt takes place every approximately 520 μ sec for the NTSC model and every approximately 625 μ sec for the PAL/SECAM model. The CPU performs the Δ f detection and outputting of the signal to the ICL12 (ICL11) 8-bit D/A converter at every interrupt, and performs other processing during the rest of time.
The V interrupt signal and wobbling interrupt signal are input to the INT1 terminal of the CPU. The CPU determines the amount of DT head jump by detecting the amount of Δ f and $\Delta\phi$, at the timing of V interrupt. The calculated amount of DT head jump is converted into analog signal by the ICM12 (ICM11) 12-bit D/A converter, and is sent to the DT head driver. The interrupt by wobbling can provide the detection whether DT head is displacing normally or not, from the strain gauge output, and makes judgment to turn on or off the integrator of the DT head driver. Interface between SV board and RD board, is carried out by the ICJ4/ICJ5 (ICK10/ICK11) 4×4-bit register file. Data transmission/reception that are periodically done, are shown as follows. Now, in the EPROM with version 1, write and read are done once in every vertical timing. In the EPROM with version 2, they are done twice in

every vertical timing, and not only the periodic data transmission / reception but also arbitrary data transmission/reception in accordance with requesting address from the CPU, is possible.

SV board→RD board

DSRO bit5 : STILL (version 2 and later)
bit4 : PHASE LOCK (version 2 and later)
bit3 : CONFI
bit2 : FIELD/FRAME
bit1 : CAPSTAN LOCK
bit0 : DT ENABLE

DSR1 bit3 : OUTPUT SC-H (1 : EVEN)
bit2 : PINCH OFF
bit1, bit0 :
SC-H SHIFT
00 : SC-H 0
01 : SC-H +
10 : SC-H −

DSR2 bit3 : VIDEO LACK
bit2, bit1 :
TV SIG
00 : NTSC
01 : PAL-M
10 : PAL
11 : SECAM
bit0 : AUTO JUMP

RD board→SV board

DSW0 bit3 : INTEG ON
bit2 : CF DETECT
bit1 : BAT ERROR
bit0 : DT CPU ERROR

DSW1 bit3 : TAPE/REF SC-H SEL
bit2, bit1, bit0 :
REF SC-H DATA
000 : BLANK
001 : SC-H<−70°
010 : −70° <SC-H<−40°
011 : −40° <SC-H<−20°
100 : −20° <SC-H<+20°
101 : +20° <SC-H<+40°
110 : +40° <SC-H<+70°
111 : +70° <SC-H

DSW2 bit3 : TAPE/REF SC-H SEL
bit2, bit1, bit0 :
TAPE SC-H DATA
000 : BLANK
001 : SC-H<−70°
010 : −70° <SC-H<−40°
011 : −40° <SC-H<−20°
100 : −20° <SC-H<+20°
101 : +20° <SC-H<+40°
110 : +40° <SC-H<+70°
111 : +70° <SC-H

4-5-3. ADV PB V Generator (RD-6/RD-7 Board)

The PB V signal is input to the RD board from the VO board as a jump timing signal. The PB V signal has the timing of negative going of the second equalizing pulse of the playback video signal. In order to prevent from the effect of dropout, etc., an AFC loop using PB signal, is formed in RD board that generates ADV PB V signal. The ADV PB V signal is used as the jump timing signal. The ADV PB V signal is the signal that is advancing to the PB V signal phase by 2H (3H for EPROM with version 2). This phase difference is provided considering the operation time of the CPU required to calculate the jump amount after detection of V signal. Jump timing is normally using the ADV PB V signal, but when the relation between ADV PB V signal phase and PB V signal phase is changed, it is reset immediately by PB V signal timing. Also the 16th line of playback signal is detected at the same time, and is sent to the TBC system (CK board) as the DT V signal.
The PB V signal that is input to "A20b" terminal of the RD board, is gated by the PB WINDOW signal that is input to "B4c" terminal, and is input to the ICK12 (ICK12) V selector. The PB WINDOW signal generated by the SV board is the window pulse of −6H/+4H width against the PB V signal. Because the PB WINDOW signal is generated from the PG pulse, when drum is not rotating, it may be input to the RD board with erroneous timing. To prevent this, the PB WINDOW gate is inhibited during DT OFF period in such mode as EE mode, by the PA6 (pin 7) output of the CPU.
The FHX signal that is input to B11c terminal of the RD board, is the playback H signal which is stabilized by AFC, and is supplied from the TBC (CK board). The FHX signal is frequency-doubled by ICH15 (ICJ7, J8) and becomes 2FHX signal. The CTC counts the 2FHX signal and generates the ADV PB V signal.
The ADV PB V signal is generated by the three counters (CTC32, CTC31, CTC30) that are built-in CTC ICJ20 (ICK17). The clock signal for each counters is the 2FHX signal. The GATE terminal (pin 16) of CTC32 receives the SEL V signal from the V selector. The GATE terminal (pin 14) of CTC31 receives the jump status signal from the output terminal (pin 17) of CTC32. The CTC30 GATE terminal (pin 11) of CTC30 receives the DT V signal from the output terminal (pin 13) of CTC31. The V selector (ICK12) selects first the PB V signal as the SEL V signal. After the ADV PB V signal and the PB V signal establish the specified phase relationship, it selects the ADV PB V signal as the SEL V signal. CTC32 performs three counts of 2FHX signal during when the SEL V signal remains "LOW" level, and produces its output. The CPU performs calculation to determine the jump amount during this period. The counted

data according as the jump amount, are written into CTC31. Thus, the output of CTC31 becomes always at the timing of 16th line of playback signal. Since the playback video signal length is made longer or shorter at every one track pitch jump for the amount of 2.5H (3.5H in the PAL/SECAM model), the counted data must be changed in accordance with the amount of jump. The CTC31 output is the DT V signal that is sent to TBC (CK board). CTC30 performs counting of fixed value after the DT V signal, and produces ADV PB V signal at the timing of 2H (3H for EPROM with version 2) before the PB V signal phase.

Counter 0 (CTC40) of CTC ICJ22 (ICK18) generates the one clock (1/2H) width pulse at the timing of 2H (3H for EPROM with version 2) after the ADV PB V signal. This pulse is input to ICK13 (ICK14) as the window of the PB V signal. ICK13 (ICK14) detects whether leading edge of PB V signal is located within the window pulse or not. The detected phase information is input to the PA2 terminal (pin 3) of the CPU. The CPU controls the V selector based on this phase information. The PB V signal is also input to the AN4 terminal (pin 38) of the CPU, so that the information from ICK13 (ICK14) is neglected if the PB V signal is not detected.

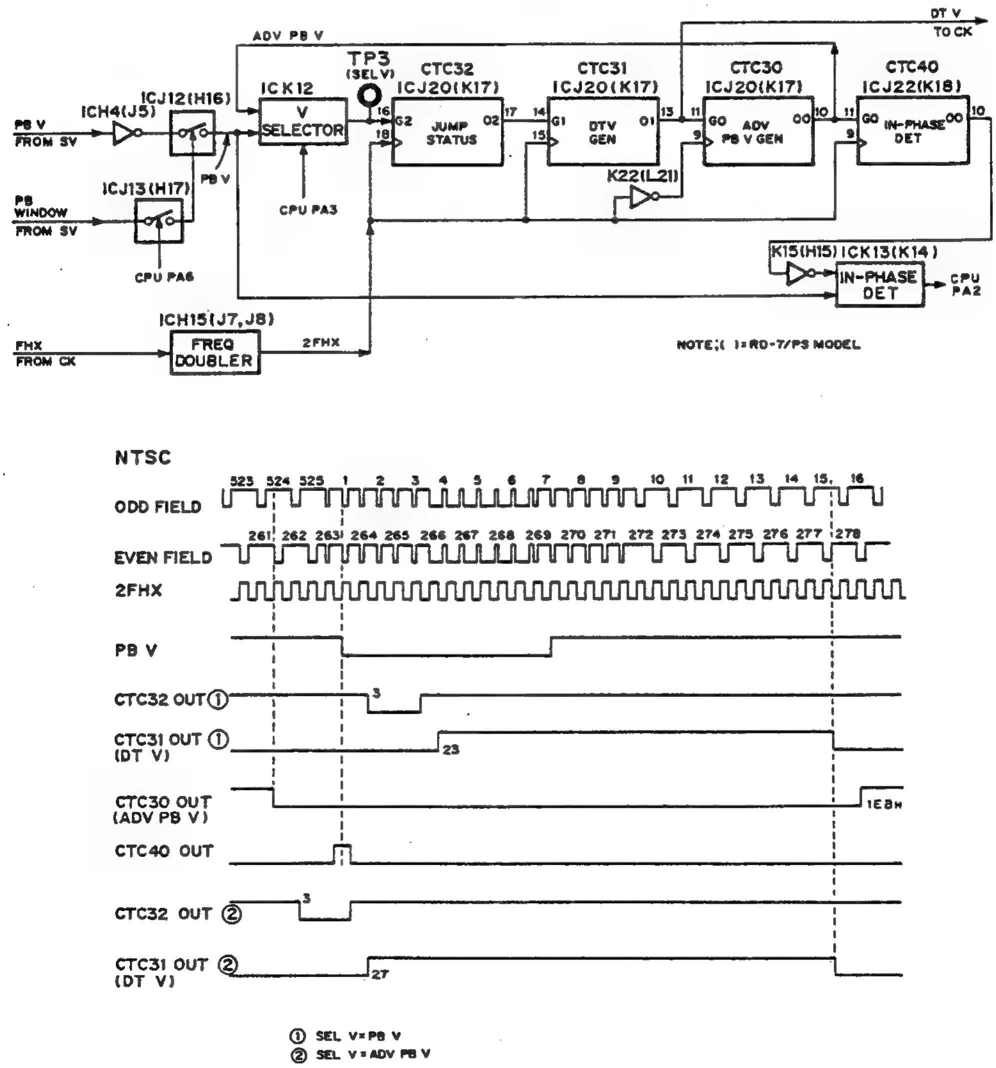


Fig. 4-5-3. ADV PB V Generator (RD-6/RD-7)

4-5-4. Δf Detector, $\Delta \phi$ Detector and Wobbling Signal Generator (RD-6/RD-7 Board)

When a recorded tape is played back in the different tape speed other than that used in the recording mode, the playback head will have different head angle other than that of recorded track. The Δf correction is to control the the DT head displacement until the trace angle of DT head becomes equal to the recorded track angle. When tape speed is changed, the trace angle of the DT head is also changed so that the length of playback video signal in a unit time period is also changed. By measuring the H sync pulse period of the playback signal, the Δf can be detected. In the other words, the Δf is the relative speed information of head against tape.

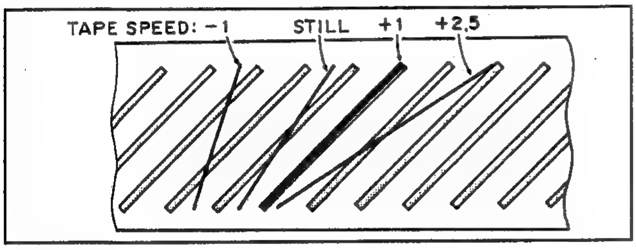


Fig. 4-5-4. Δf Correction

Because of difference in the track linearity between the recorded track and DT head, etc., the Δf alone cannot correct all the the tracking error so that some tracking error still remains. In order to remove the tracking error, the DT head is wobbled at a certain frequency (720Hz for the NTSC model, 700Hz for the PAL/SECAM model) in the direction parallel to the head gap. The playback RF signal is amplitude modulated by this wobbling where the amplitude modulation component is extracted from the playback RF signal, in order to detect tracking error component. Feedback is applied to the DT head controller until the tracking error is kept to constant value. Thus the DT head displacement is controlled.

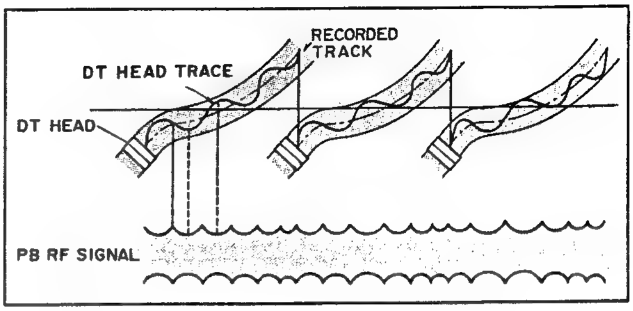


Fig. 4-5-5. Wobbling

When playback head reaches the end of a recorded track by tracing, it must determine which track should be traced next. When slow playback is carried out, the same video track must be repeatedly traced. When playback of faster than ×1 speed is carried out, skip tracing must be performed.
For an example, the case when DT playback at 1.2 times normal speed, is explained as follows.
The recorded track is shown in solid line and tracing of fixed playback head against the recorded track is shown in dotted line. In order for tracking to be conducted correctly, the DT head must be displaced from the dotted line to solid line. In this example, the 4th and 10th tracks are skipped. When the DT head is jumped, the jump position and jump amount are determined and controlled by the $\Delta \phi$ and aforementioned Δf. The $\Delta \phi$ is the phase information of the playback signal against the reference signal, that is detected by measuring the phase difference between the REF V signal and PB V signal.

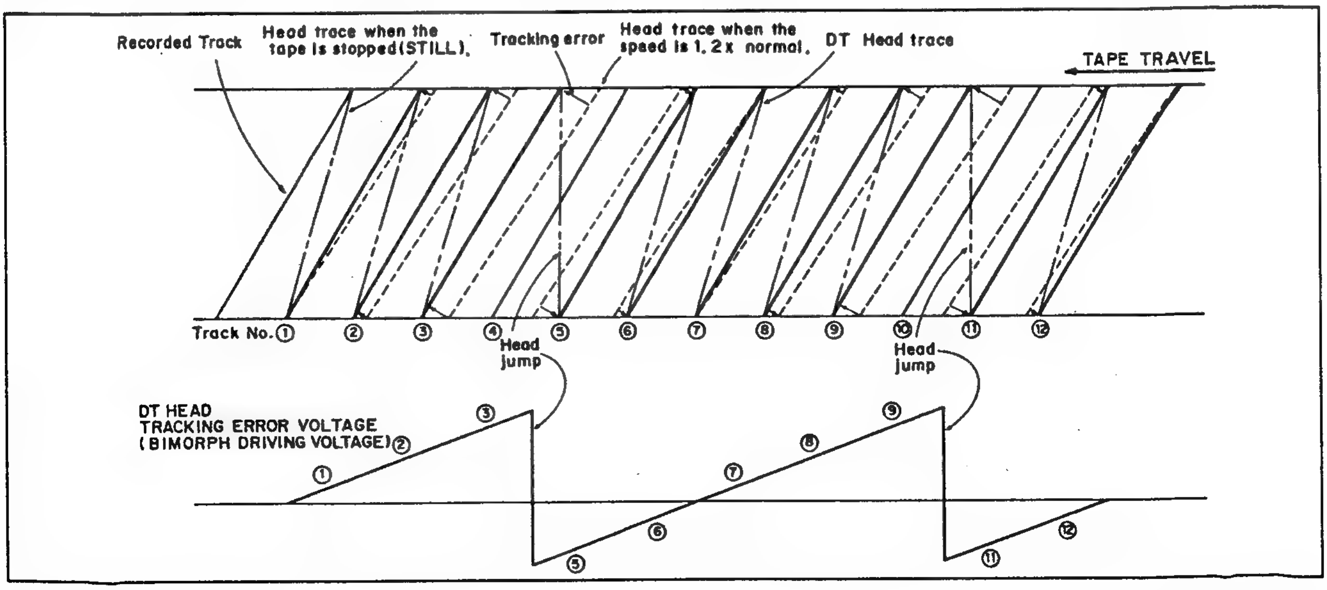


Fig. 4-5-6. Head Jump

(1) Δf detector (RD-6/RD-7 board)

The GATE terminal of CTC12 (pins 16, 17, 18 of ICJ17/K19) receives pulse from the PA1 terminal of the CPU at every interrupt event of "~RD INT2". CTC12 performs three counting of FHX that is the playback H signal, as triggered by the aforementioned pulse, so that the pulse that is equivalent to 3H width of playback signal, is output. CTC22 (pins 16, 17, 18 of ICJ19/K21) is a down counter that works only when its GATE terminal is "H" level, and is preset to "1417" in the NTSC model and "2374" in the PAL/SECAM model. When 3H width pulse is input to CTC22 from CTC12, CTC22 starts counting and the counted data are held after input pulse is ended. The clock pulse for CTC22 is 2fsc in the NTSC model and is $908f_H/2$ in the PAL/SECAM model. The memorized data in CTC22, is written by the CPU at the timing of next "~RD INT2" interrupt, so that the counter is preset again, and the PA1 terminal of the CPU output the pulse. This operation is repeated. The data that is written by the CPU is output from 8-bit D/A converter as the slope information of the head.

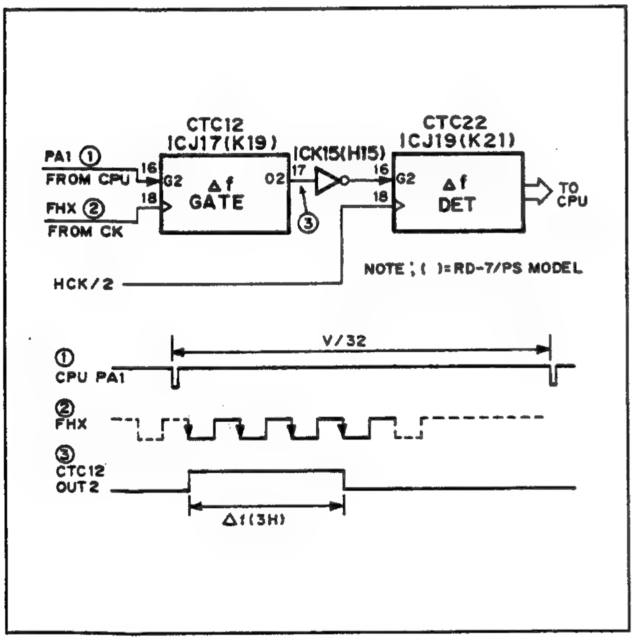


Fig. 4-5-7. Δf Detector (RD-6/RD-7)

(2) Δφ detector (RD-6/RD-7 board)

The REF ADV V signal is the signal of ±6H width centering around the PB V signal timing. This timing does not change due to tape speed nor phase. So, phase difference between the reference signal and playback signal can be known by measuring the SEL V signal phase against the REF ADV V signal phase. Because BVH-3000/3100 is using the ADV PB V signal as the V signal where the ADV PB V signal advances by 2H (after version 2, it is 3H) to PB V signal, the PRE REF ADV V signal whose phase is advancing 2H (or 3H) to REF ADV V signal, is generated by CTC41 (pins 13, 14, 15 of ICJ22/K18). The phase difference between the PRE REF ADV V signal and SEL V signal is compared by ICK13 (K14) and the phase difference is converted to a pulse width. CTC10 measures the pulse width of ICK13 (K14), that is in other words, Δφ. The measured Δφ data are read by the CPU at the SEL V signal timing, and are used for jump judgment. The 2fsc clock is divided by 25 with CTC11, and it is used as the clock pulse for CTC10 in the NTSC model. The $908f_H/2$ clock is divided by 34 with CTC11, and it is used as clock pulse for CTC10 in the PAL/SECAM model.

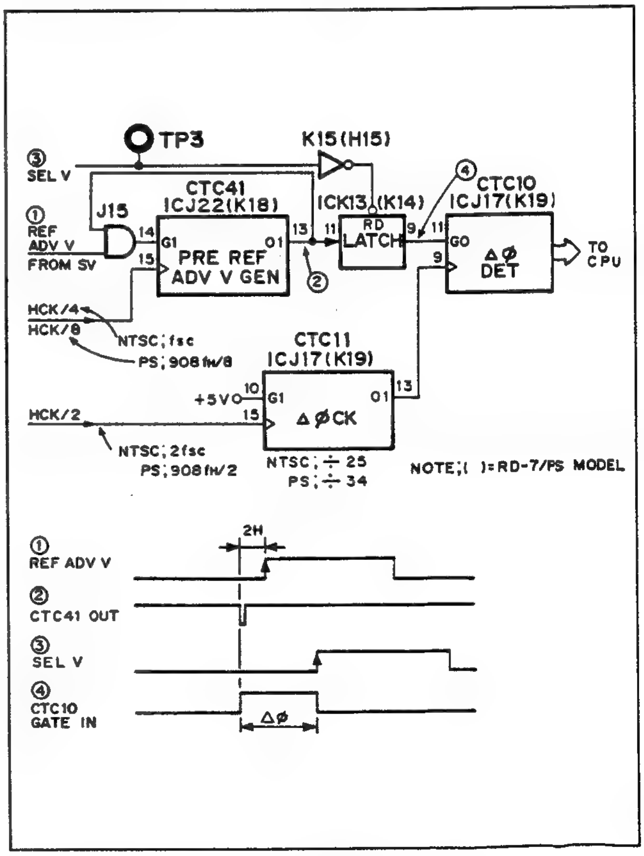


Fig. 4-5-8. Δφ Detector (RD-6/RD-7)

(3) Wobbling signal generator (RD-6/RD-7 board)

[When the suffix No. of the RD board is -11 or -12] CTC20 (pins 9, 10, 11 of ICJ19/K21) divides the clock signal to 720Hz (700Hz in the PAL/SECAM model) during when the GATE terminal is "H" level. PA6 is the signal that goes to "H" level when DT is ON. So, the GATE terminal of CTC20 receives the REF ADV V signal only when DT is ON so that the signal that has wobbling repetition cycle is output from pin 10 (OUT0). CTC21 (pins 13, 14, 15 of ICJ19/K21) outputs the pulse of approximately 1100 μsec width from the SEL V signal, and during this period, the wobbling is stopped to OFF. The output signal thus obtained, is passed through the ICL9 low-pass filter to be shaped to sine wave, and becomes the wobbling signal.

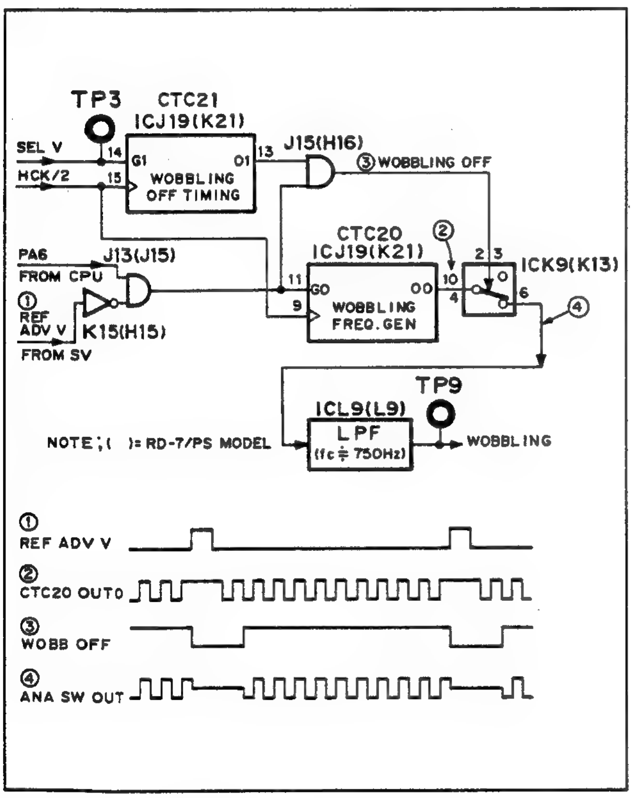


Fig. 4-5-9. Wobbling Signal Generator (RD-6/-7 : -11, -12)

[When the suffix No. of the RD board is -13] CTC21 (pin 13, 14, 15 of ICJ19/K21) counts the clock constantly from the REF ADV V signal only during DT ON, and outputs "L" level at the last clock timing. CTC20 (pins 9, 10, 11 of ICJ19/K21) divides the clock into 720Hz in the NTSC model (700Hz in the PAL/SECAM model). CTC20 starts counting at the rising edge of the GATE input pulse so that the wobbling phase can be changed by the counting numbers of CTC21. In the circuit on the RD board with "suffix-13", the wobbling off period is not set. The output pulse thus obtained, is shaped into sine wave by a low-pass filter, and becomes the wobbling signal.
Because the negative going of CTC20 output signal corresponds to the peak of wobbling signal, this signal is input to INT1 terminal of CPU so that the level of strain gauge signal is measured at the moment of interrupt, in order to detect the wobbling of DT head and is used to judge the generation of INTEG OFF (integrator stop to off) signal. The wobbling timing signal is input to PC6 terminal of CPU so that the SEL V signal and wobbling are discriminated when INT1 terminal is interrupted.

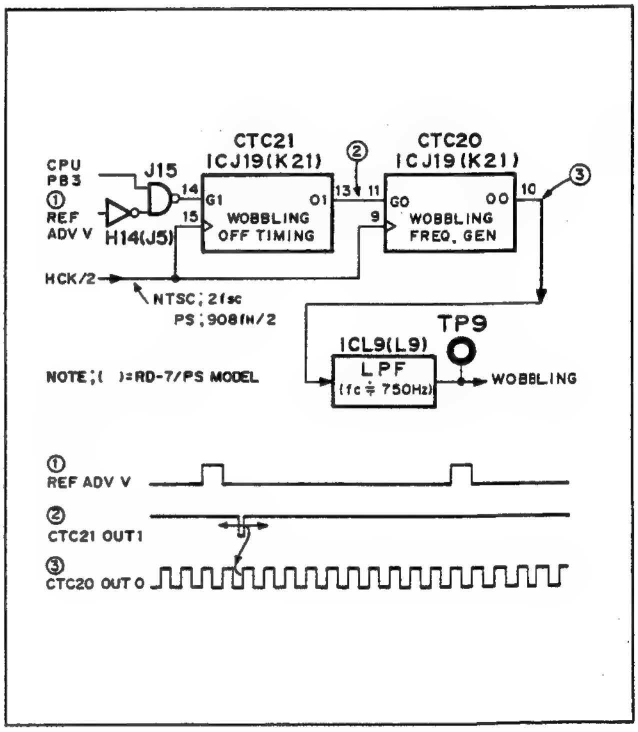


Fig. 4-5-10. Wobbling Signal Generator (RD-6/-7 : -13)

4-5-5. Tracking Error Detector (RD-6/RD-7 Board)

Displacement condition of the DT head can be detected from the ST GAUGE (strain gauge) signal. The strain gauge is a resistive material (approximately 120 Ω) that is attached on top of the bimorph plate of the DT head, whose resistance value changes depending upon physical stretch and shrinkage of the bimorph plate. Motion of DT head can be detected from the change of resistance value of the strain gauge.
Trace condition of the DT head with reference to the recorded track can be detected from the RF envelope signal. Since the DT head is tracing the recorded track while it is wobbling, the RF envelope of upper portion and lower portion will become symmetrical when the recorded track is straight. If the recorded track is curved, it will lose symmetry.

Only the AC component that is included in the RF envelope and strain gauge signals are amplified, and passed through approximately 500 Hz low-pass filter and are input to the ICM3 (ICN3) multiplier. The wobbling frequency component and its doubled frequency component that are included in the multiplier output signal, are removed by the notch filter (band eliminating filter) at the next stage so that only the tracking error information is extracted. The extracted tracking error information is input to the integrator (DT drive signal generator) at the next stage. The integrator output signal is fed back to the input of the strain gauge amplifier so that the slope signal component included in the strain gauge information can be removed.

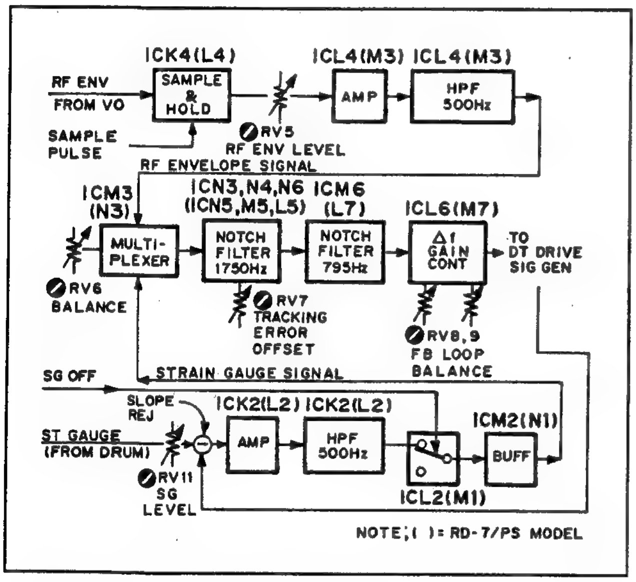


Fig. 4-5-11. Tracking Error Detector (RD-6/RD-7)

4-5-6. DT Drive Signal Generator (RD-6/RD-7 Board)

When a recorded tape whose track is outside the type-C format, is played back, or when sensitivity of the DT head is changed after long period of use, the jumped position (contact starting position) of a track can be off-track of the recorded tape. In this case, the playback RF signal level remains low until the DT head follows the recorded track by wobbling, so that streakings on the top of monitor screen can appear.

In the BVH-3000/3100, the RF envelope level at the beginning of playing back of a track, is detected and the jump amount is always changed for the maximum RF envelope level. This control is called as "AUTO JUMP". This jump amount data are memorized in each modes of every jump pitch (in field mode, −3, −2, −1, 0, +1, +2, +3 pitches, and in frame mode, −2, 0, +2 pitches respectively). This memorized data are backed up even during power is turned off.

The signal such as the jump signal from the ICM12 (ICM11) 12-bit D/A converter, Δf signal from the ICL12 (ICL11) 8-bit D/A converter and the tracking error information are added and are input to the ICL6 (ICM7) integrator. The integrator generates the slope wave from the Δf and tracking error information in proportional to the bending of recorded track, and converts the jump signal into the jump wave. The jump wave and the wobbling signal are superimposed and the the DT drive signal is generated. DT ON/OFF is controlled by PA6 (pin 7 of CPU). The RV10 is used when the DT head motion is visually checked and becomes active as the jumper plug is changed from JP3 to JP4.

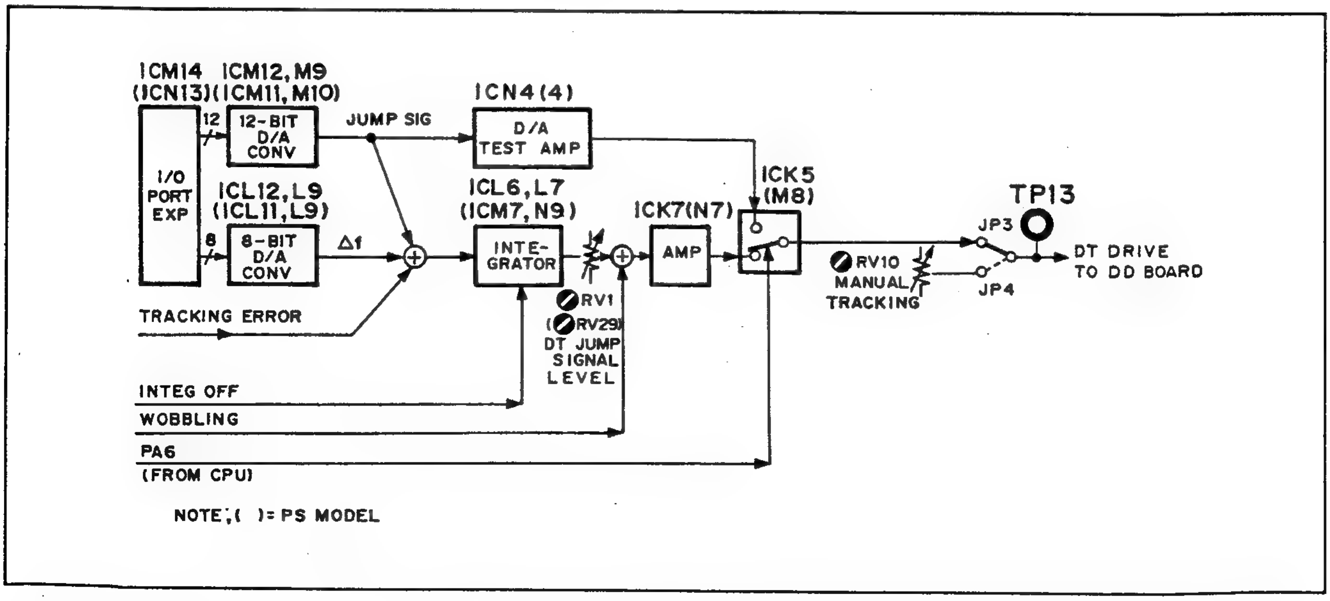


Fig. 4-5-12. DT Drive Signal Generator (RD-6/RD-7)

4-5-7. Additional Function for Board No."-13" (RD-6/RD-7 Board)

(1) Ringing level detector (RD-6/RD-7 board)

Ringing is the unwanted vibration that is generated when the DT head is moved quickly. The ringing is generated immediately after head jump, resulting in the poor RF waveform during playback at the beginning portion of track by the DT head.
BVH-3000/3100 employs the two-step jump system in order to decrease the ringing. In this system, steep slope is used first to drive the DT head and this slope is made slow in its middle in order to suppress ringing so that the DT head is driven.

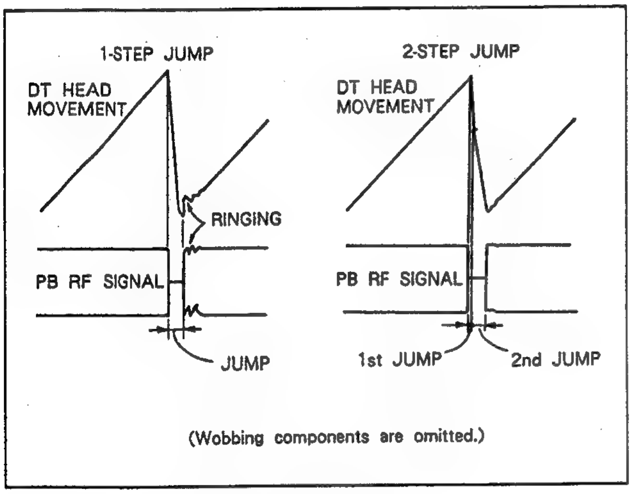


Fig. 4-5-13. Two-Step Jump System

But, the time that can be used for jump is fixed, the adverse effect from non-uniform performance of DT heads cannot be completely removed. Then, in the RD board having suffix-13 and later, the function that can control the jump time so that the ringing detection level becomes minimum, is added. The primary resonant frequency of bimorph that is the major component of the ringing, is extracted from the strain gauge signal, and input to the CPU. The CPU adjusts the ratio of jump at the first period and second period so that the ringing is minimized. This adjustment is started by pressing the TEST switch (S1) on the RD board for approximately two seconds during VAR −1 speed mode (CTL lock mode). During this adjustment, the "READY" LED blinks and when it is adjusted for optimum value, the LED is turned off and the adjustment is automatically finished. This adjustment should be done when upper drum is replaced so that the DT head can be jumped optimum track.
The strain gauge signal is passed through ICK2 (IC5) high-pass filter of 500 Hz center frequency so that the slope component is removed. It is input to the ICM1 and ICM2 ringing level detector. Out of this input signal, the notch filter having center frequency of 720 Hz is used to remove the wobbling component, and then the bandpass filter having center frequency of 1350 Hz is used to separate the ringing component. The separated the ringing component is input to the ICN1 analog switcher where the beginning portion alone is extracted to be peak-held by ICM1 and ICM2. The ringing signal is mixed with the REF SC-H signal by the ICN2 analog switcher and is input to the analog port of the CPU.

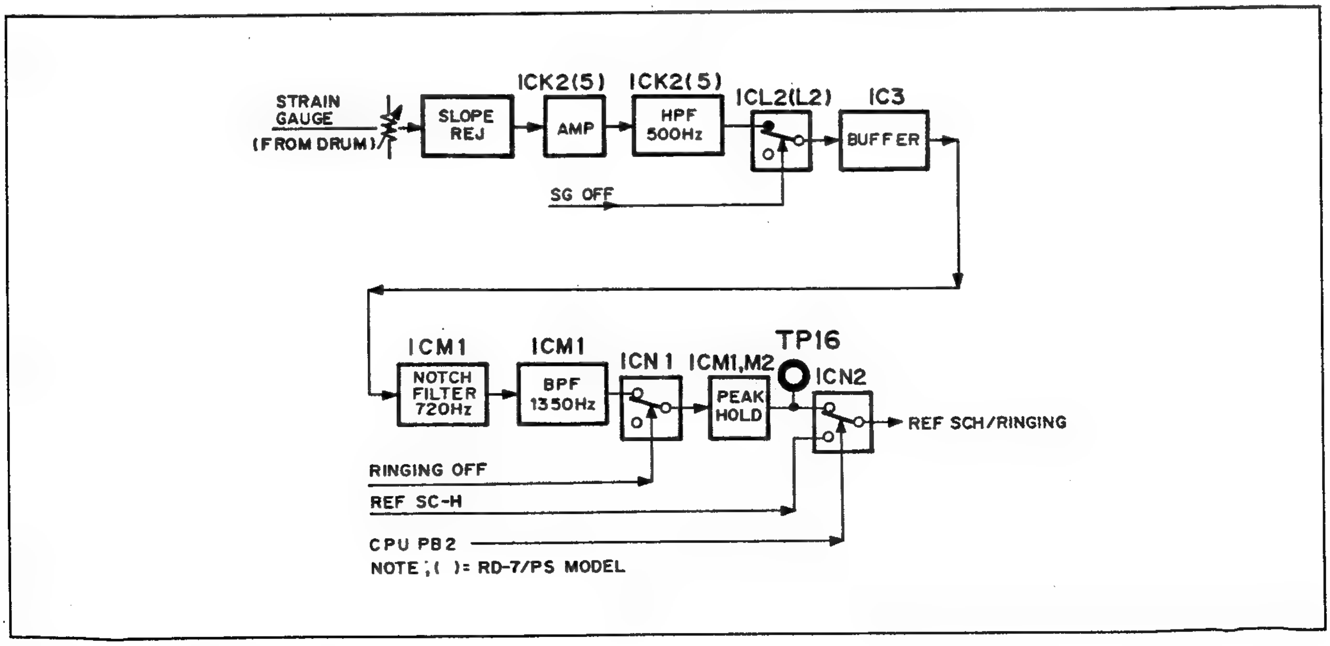


Fig. 4-5-14. Ringing Level Detector (RD-6/RD-7)

(2) Filter during DT OFF (RD-6/RD-7 board)

DT ON/OFF is controlled by the ICL5 analog switcher. When DT is OFF, output is set to 0V. But, depending upon the positions of the DT head, click noise can occur due to quick displacement. In the RD board having suffix-13 and later, the output is passed through a low-pass filter having center frequency of 500 Hz when the DT is turned OFF and then main line is released. Then the signal is smoothly set to 0V when DT is turned off and click noise is prevented.

(3) Feedback gain suppressor during INTEG OFF (RD-6/RD-7 board)

INTEG OFF is to stop the integrator that is generating slope signal, when the DT head happens to stop wobbling, or the DT head is not tracing the recorded track correctly. In this case, DT DRIVE signal is reset to the value near the center value and waits until the the DT head starts to follow the recorded track again. But, because tracking error detection gain is high, DT DRIVE signal comprises DC offset so that it takes time until the DT head starts following the recorded track again. Then in the RD board having suffix-13 and later, the tracking error detection gain is decreased during INTEG OFF period so that the time required to start following again, is shortened.

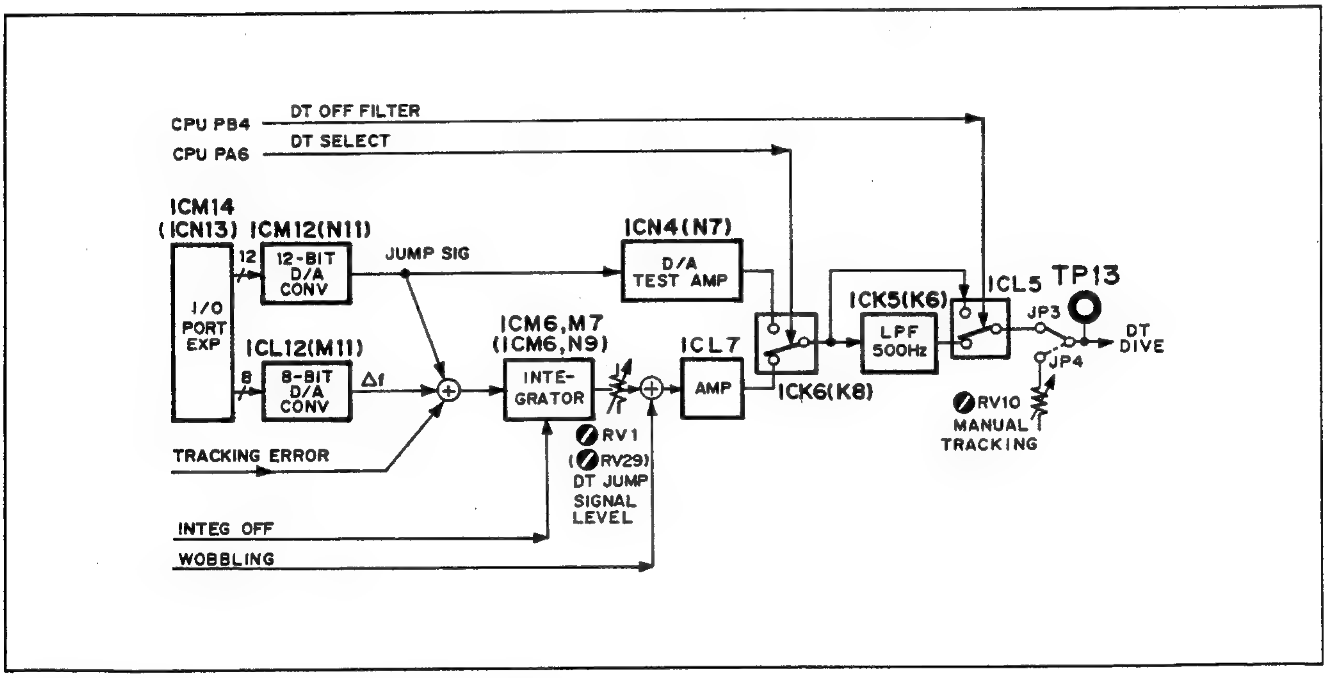


Fig. 4-5-15. Filter during DT OFF (RD-6/RD-7)

4-6. SERVO SYSTEM

4-6-1. Outline of Servo System

The servo system of the BVH-3000/3100 consists of the following boards.

SV-90 board : Main CPU
Address decoder
Video logic controller
Reference pulse generator
Sub CPU, motor servo
Tape transport interface
RD-6 (NTSC) /RD-7 (PS model) board :
Servo reference signal generator
CD-36 board : Capstan motor driver
Drum motor driver
RM-43 board : S reel motor driver
T reel motor driver
DS-19 board : Solenoid driver
Moving guide motor driver
IP roller motor driver
Sensor output level converter

(1) SV-90 board

The SV-90 board controls all operations after the mode controller, communication with the parallel remote (REMOTE 3), and logic processing of the video system, audio system, and TBC system.
Control signals for the tape transport system and video logic signals generated in this board are supplied directly as parallel data, and other control signals are supplied via a common bus, to the AU, VO, PR, CK, RD, SY and PA boards.
The SV-90 board has a main CPU (ICK19, V20 : μPD70108D) and a sub CPU (ICB15, μPD78C10G) which contains an A/D converter. The main CPU performs motor servo processing, CTL processing and timer processing. The RAM (ICE16) connected to the sub CPU is used for communication with the main CPU. Most of the data in the servo system are processed by software. The processed data are latched in the respective boards, and used as control signals.
Each motor used in the BVH-3000/3100 is controlled by the CPU servo. An analog damping loop operates for transient responses which the arithmetic section of the CPU cannot follow, and the analog control voltage obtained is superimposed on the CPU servo control voltage.

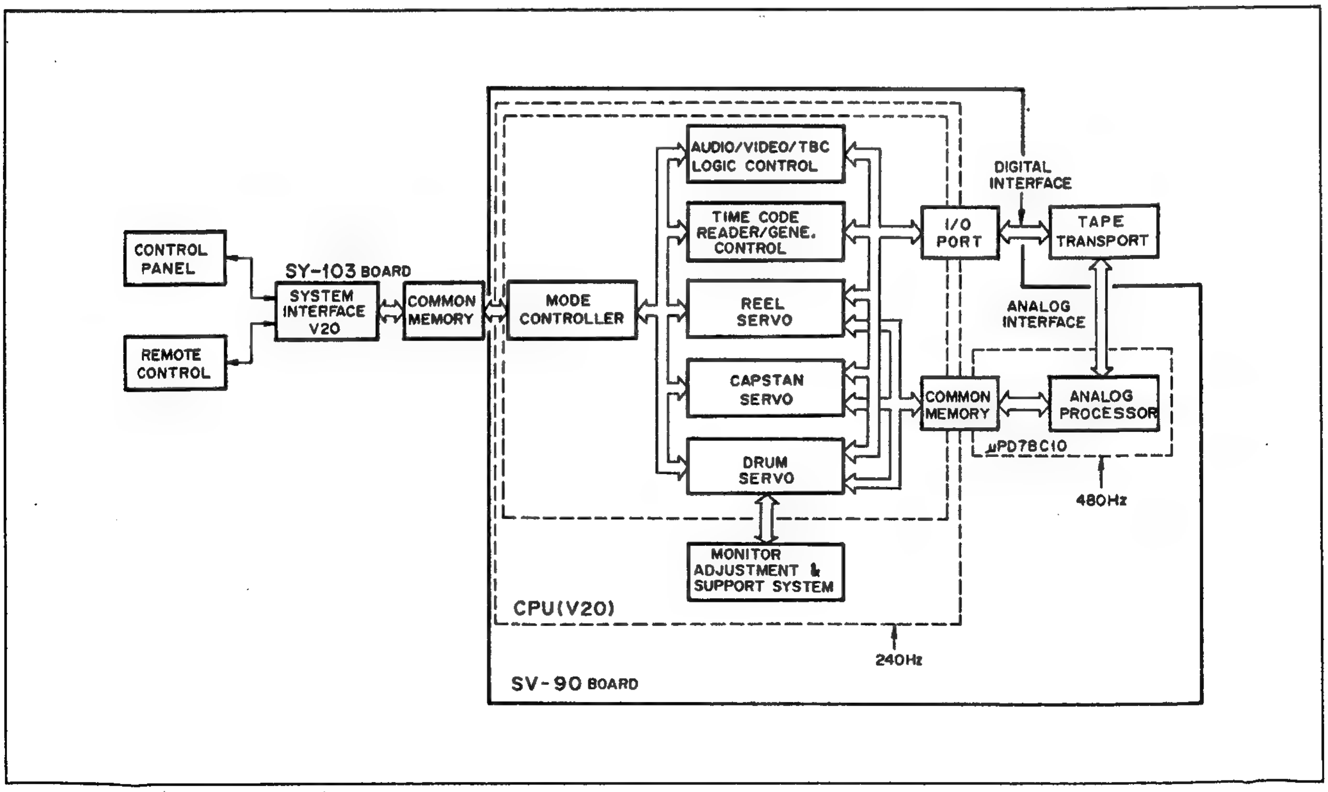


Fig. 4-6-1. SV-90 Board

In the CPU servo, the FG pulses and PG pulses generated according to the rotation of each motor are wave-shaped, and the outputs are input to the PTC (Programmable Timer Counter) and the PFC (Phase and Frequency Counter) where the phase and speed are measured.

The main and sub CPUs on the SV-90 board calculate the optimum control voltage for each motor based on the input data, and supply these voltages to D/A converter ICA16. The output of the D/A converter is time-sharing processed in an analog switcher, then passes through a sample hold circuit to be supplied to each motor as a motor control voltage for a digital servo.

The value of the potentiometer installed on the supply side (S) tension arm shaft (S-REEL TEN), capstan FG (CPADT, CPBDT, CPADD, CPBDD), T reel FG (T-REEL FG A, T-REEL F G B), S reel FG (S-REEL FG A, S-REEL FG B), the drum motor control voltage (DMVLD), and the capstan motor control voltage (CPVLD) are multiplexed by ICF9, ICF10 and ICF11, and supplied to the sub CPU ICB15 analog input (A-SIG0 to A-SIG3) terminals.

In the analog velocity loops of the drum system and capstan system, the time difference between the FG A pulse and the FG B pulse is measured for each pulse and converted into a voltage. The analog velocity loop is effective for the drum motor within ±6% of the regular speed, and for the capstan motor within ±6% of the velocity deviation in the normal PLAY mode. Consequently, in the variable mode, the capstan motor is controlled only by a digital servo which is controlled by the CPU.

Torque adjustment of each motor and drum PG adjustment, etc., can be performed from the control panel by using the setup menu. The adjustment values are stored in a non-volatile memory IC1 on the MB-140 board (mother board). Consequently, there is no need to adjust the servo system even if the SV-90 board is replaced.

(2) RD-6/RD-7 board

The RD-6 board (or RD-7 board for PAL/SECAM) consists of a servo reference signal generator circuit, TBC reference signal generator circuit, and DT control circuit.

The main functions of the servo reference signal generator circuit are as follows.

- REF SYNC generation
- REF V and REF H detection
- REF SC-H phase detection
- SEL FRAME and SEL CF generation

For details of the TBC reference signal generator circuit, refer to section 4-4 ; for details of the DT control circuit, see section 4-5.

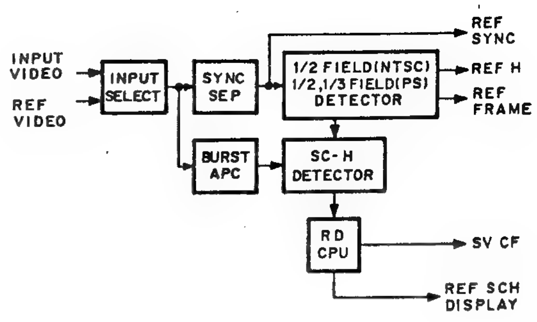


Fig. 4-6-2. Servo Reference Signal Generator (RD-6/RD-7)

(3) CD-36 board

The CD-36 board consists of the capstan motor and drum motor drive amplifiers. Each motor is driven by current control and voltage control by the MDA signal (analog signal) from the SV-90 board. The voltage is controlled by the MDA signal which varies the power supply voltage of the motor drive circuit up to a maximum of 40V. The variable voltage power supply is on the SP-02 board in the UR-20 power supply unit.

Three-phase DC motors are used for the capstan motor and the drum motor, hence it is necessary to switch the polarity on the drive circuit side. The signal which performs this polarity switching is generated inside each motor. The CD-36 board also detects the drum FG and capstan FG output and the drum PG.

(4) RM-43 board

In the RM-43 board, the analog control voltages (T REEL, MDA, S REEL MDA) and also the TRTCW signal and SRTCW signal which indicate the direction of torque generation are supplied from the SV-90 board in order to control the S reel motor and T reel motor drive voltage and current. Like the drum motor, the drive voltage controls the variable power supply voltage of the power supply unit. This voltage is set to a maximum of 80V.

The reel motor is a 3-phase DC motor, hence it is necessary to switch the polarity at the drive circuit side. The polarity switching signal is generated inside the motor. The RM-43 board also detects the reel motor FG output and the direction of rotation.

4-6-2. Servo Control System (SV-90 and MB-140 Boards)

(1) Clock pulse generator (SV-90 board)

This circuit consists of ICM19 and crystal X2. 14.7456 MHz clock pulses are output from pin 12 (OSC terminal) of ICM19. This frequency is divided into the specified frequencies by a circuit at a later stage, then used to measure the speed and phase of the motor servo system. Also, 50% duty 7.3728 MHz clock pulses are output from pin 8 (CLK terminal) of ICM19, and used in the main CPU and reference pulse generator circuit.

(2) Main CPU (SV-90 board)

The main CPU ICK19 (V20 : μPD70108D) is operated by 7.3728 MHz clock pulses from the clock pulse generator ICM19.
The main CPU uses interrupt control unit (hereafter called ICU) ICL16 as an external device. This device assigns a priority sequence to interrupts and then processes them. The following signals are input to the ICU.

- Pin 25 INTR7 : $\overline{\text{NVWR}}$ (When S2=ON)
- Pin 24 INTR6 : CPU INT (V／4 interval signal)
- Pin 23 INTR5 : TC INT (TC read timing signal)

EPROMs ICN5 and ICN3, each of which has a capacity of 256k bits, are used as external ROMs for the main CPU ICK19, providing a total memory capacity of 64k bytes. In addition, a 64k bit (8k byte) SRAM ICN7 is used as an external RAM.
In the main CPU ICK19, the lower 8 bits of the address bus are used both for addresses A7 to A0 and data D7 to D0. Consequently, it is necessary to separate data from addresses according to the respective timing. Addresses and data are separated by the ASTB (Address Strobe) signal output from pin 25 of the ICK19 main CPU. ICL2 and ICL1 are used as latches to extract only the lower 8 bits of the address. ICL2 operates as a latch for the internal bus, and ICL1 as a latch for the external main bus. Both of these ICs latch the lower 8 bits of the address at the rise timing of the ASTB signal. Data D7 to D0 which is separated from the address bus is interfaced to the data bus by bi-directional buffers ICM2 and ICM1.

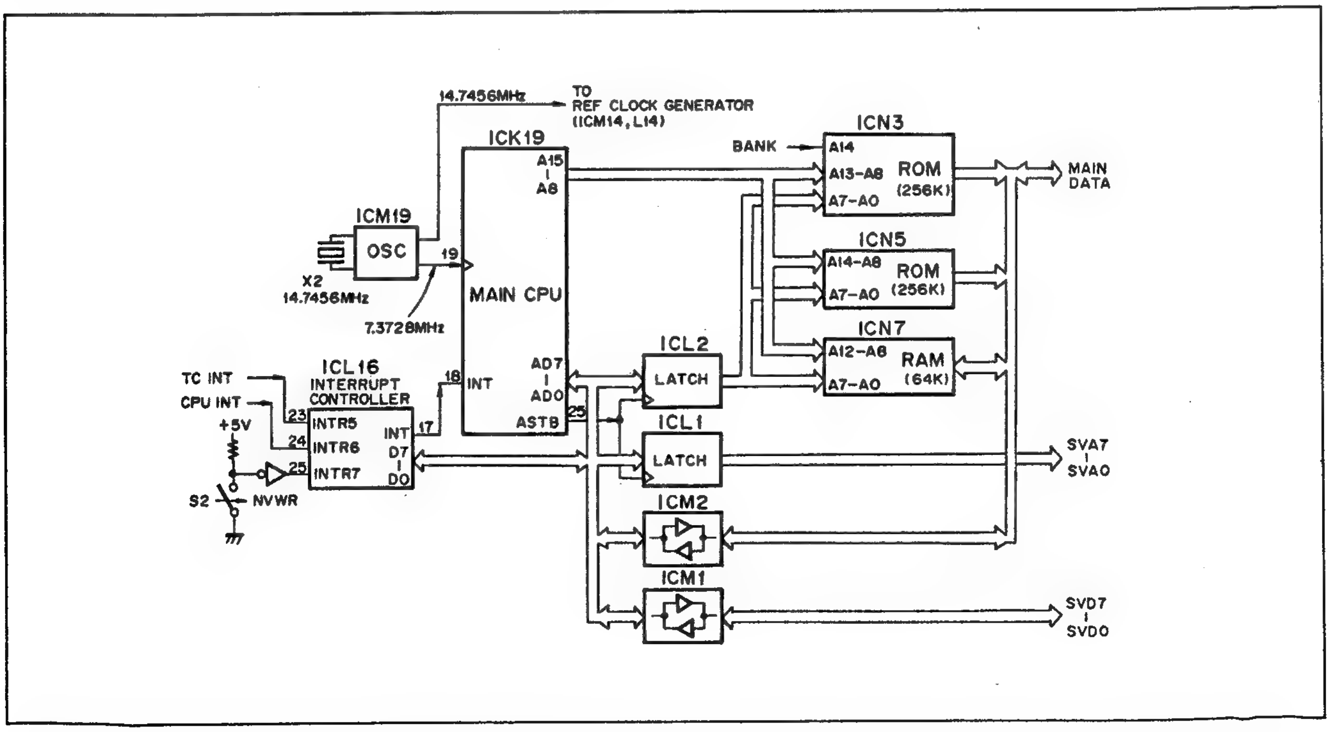


Fig. 4-6-3. Main CPU (SV-90)

(3) Main CPU memory (SV-90 board)

A 64k byte ROM (ICN5/ICN3) and an 8k byte RAM (ICN7) are used as the memory of the main CPU (ICK19). ROM ICN3 uses a bank select method in order to create a blank space in the address area. ROM ICN5 is assigned to addresses "0000H" to "3FFFH" and "C000H to "FFFFH". Also, ROM ICN3 is used as a bank method in which two kinds of data exist in addresses "4000H" to "7FFFH". Of these two kinds, the data to be output is selected by the BANK signal which is output from pin 20 of I/O expander ICG15. SRAM ICN7 is assigned to addresses "8000H" to "9FFFH".

(4) Address decoder (SV-90 board)

The main buses "SVA7 to SVA0" and "SVD7 to SVD0" are connected to each board in the amplifier chassis. They are also connected to various devices including PFC (Phase and Frequency Counter) and PTC (Programmable Timer Counter) as internal buses, and communicate with the main CPU (ICK19).
The chip select signal which specifies the opposite party for communication is generated by decoding the addresses output from the main CPU.
Chip selection of ROMs ICN5 and ICN3, and RAM ICN7 is performed by ICM4 and ICM5. The selection between an external port (AxxxH) and an internal port (BxxxH) is performed by ICM3. The chip select signal for the external port is generated by ICK1 and ICM6, and the chip select signal for an internal port is generated by ICM4, ICK3, ICK4, ICK5, and ICK6.

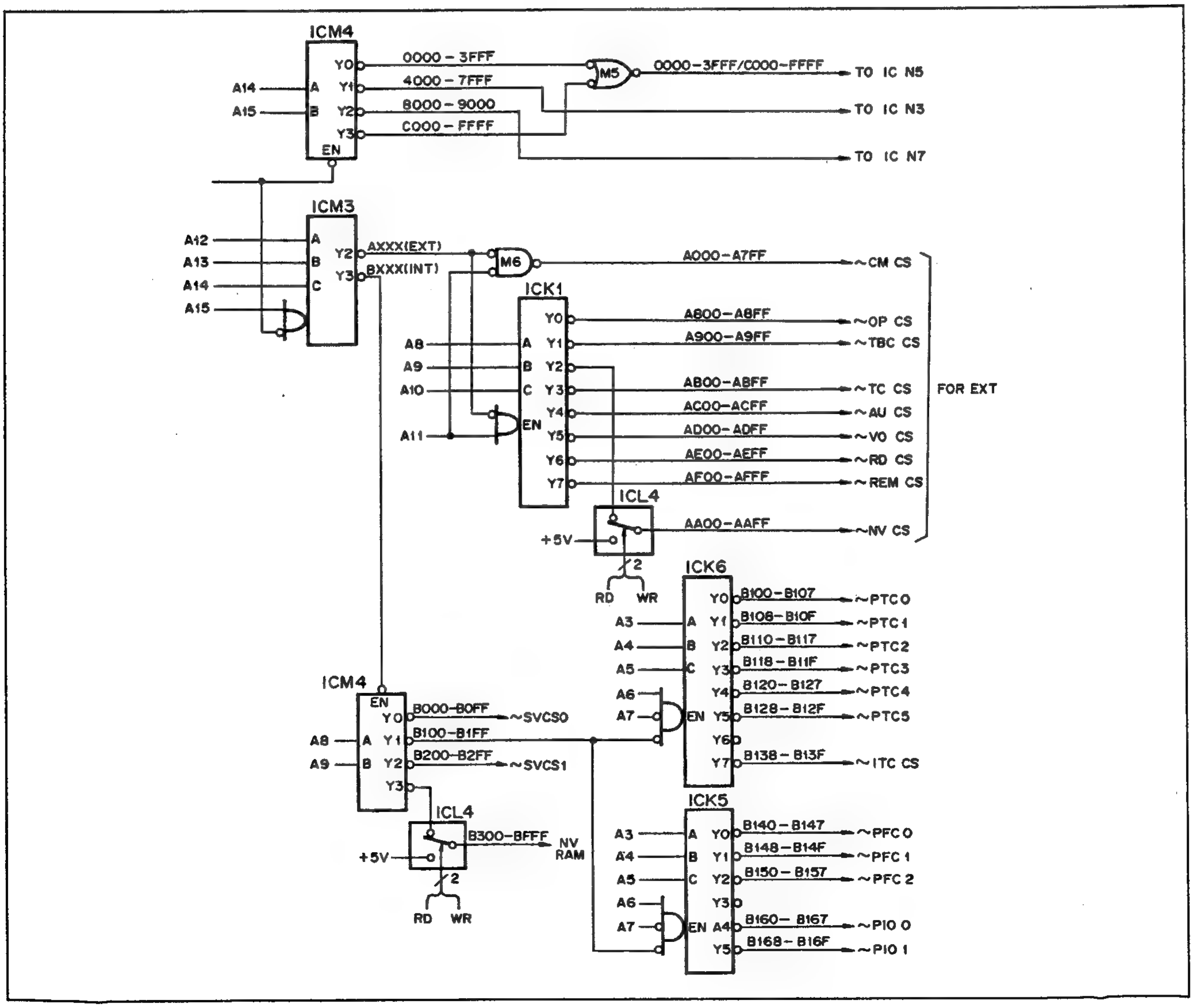


Fig. 4-6-4. Address Decoder (SV-90)

(5) Non-volatile memory (SV-90 and MB-140 boards)

A non-volatile memory (NOV RAM) is a special SRAM which can retain memorized data even after the power is switched off. The SV-90 board and the MB-140 board (mother board) each has a non-volatile memory containing the setup data.
The non-volatile memory (ICL3) on the SV-90 board contains mainly operating mode data such as remote select and the freeze mode. Non-volatile memory (IC1) on the mother board contains data related to the tape transport characteristics such as adjustment data for each motor which is necessary for processing data in the servo system. Consequently, there is no need to readjust the servo system in the event that the SV-90 board is replaced.

(6) Clock counters (SV-90 board)

Clock counters ICN8, N9 and N11 uses CMOS IC CF77074N each of which contains two 16-bit counters. These 16-bit counters count the period from the rising edge of the signal input to the START terminal to the rising edge of the signal input to the LATCH terminal, as the number of clock pulses input to the clock terminal. The count value at the timing of the rising edge at the LATCH terminal becomes 8-bit parallel data which is output from terminals D7 to D0.
Because the data output is in 8-bit parallel form and the counter and latch in the IC are 16 bit devices, the data is divided into 8 upper bits and 8 lower bits before being output. In addition, one IC contains counters for two channels, hence it selects one of four kinds of data and outputs it from the data output terminal. This selection is performed by the control logic circuit in the IC.

The functions of the input/output terminals of the clock counter are as follows.

Pin 23 CS1 : Chip select input
Pin 21 CS2 : Chip select input
Pin 22 OE : Output enable input
Pin 20 A/B : Data latch A/B select input

INPUTS					OUTPUTS
CS1	CS2	OE	A/B	L/H	D7−D0
0	X	X	X	X	HI−Z
1	0	0	0	0	CH−A LOWER BYTE
1	0	0	0	1	CH−A UPPER BYTE
1	0	0	1	0	CH−B LOWER BYTE
1	0	0	1	1	CH−B UPPER BYTE
X	1	X	X	X	HI−Z
X	X	1	X	X	HI−Z

Pin 19 L/H : Lower/upper data latch select input
Pin 10 OUT 16 : 1/16 frequency divided clock output
Pin 11 OUT 256 : 1/256 frequency divided clock output

(7) Timer counters (SV-90 board)

Timer counters ICN12, N14, N15, N17, and N19 use CMOS IC μPD71054. These timer counters are used for measuring speed and phase in the servo system. Each timer counter consists of the internal control circuit and three 16-bit counters. The 16-bit counter's functions, such as data presetting, data read-out, and operating mode assignment, are controlled by the CPU.
Each timer counter can operate in one of six modes, modes 0 to mode 5. In this unit, modes 0, 1, 2, 3, and 5 are used to perform the following eight measurements.

① Capstan FG count
(PTC-4 ICN15 : Channel 0/mode 0)
Here, the tape travel distance is measured. The condition of the channel 0/mode 0 input/output terminals of ICN15 is as follows.

GATE0 input (pin 11) : Level "H"
CLK0 input (pin 9) : Capstan 4FG (from pin 5 of ICA5)
OUT0 output (pin 10) : Not connected
Preset value : FFH

② Capstan prescaler
(PTC-4 ICN15 : Channel 1/mode 1)
The capstan speed which varies between −1 and +3 times normal speed, that is, the period of capstan FG, is measured at channel 2 of ICN14. At the capstan prescaler, a window which is equivalent to an integral multiple wavelength of capstan FG is applied to channel 2 of ICN14 to prevent overflow when measuring capstan FG and also to improve the measuring accuracy. The condition of the ICN15 channel 1/mode 1 input/output terminals is as follows.

GATE1 input (pin 14) : $\overline{\text{HCPRTR}}$ (speed measuring request signal)
CLK1 input (pin 15) : Capstan 2 FG (from pin 9 of ICA5)
OUT1 output (pin 13) : To pin 15 (LATCH B) and pin 16 (START B) of ICN8, and pin 16 (GATE 2) of ICN14

③ Capstan FG period measurement
(PTC-2 ICN14 : Channel 2/mode 0)
Here, the width of the window from the capstan prescaler is measured and the period of capstan FG calculated. The condition of the channel 2/mode 0 input/output terminals of ICN14 is as follows.

GATE2 input (pin 16) :	Capstan prescaler (from pin 13 of ICN15)
CLK2 input (pin 18) :	230.4 kHz clock (from pin 4 of ICM14)
OUT2 output (pin 17) :	Connected to ground
Preset value :	FFFFH

④ Capstan 2FG monostable multivibrator
(PTC-4 ICN15 : Channel 2/mode 1)
The output from pin 17 (OUT2) of ICN15 is used as a constant current supply control signal for the trapezoidal wave generator circuit of the capstan analog velocity loop. Pin 17 is triggered by capstan 2FG which is input to pin 16 (GATE2), and outputs pulses of approx. 96% (approx. 270 μsec) of the width of normal speed pulses. The condition of the channel 2/mode 1 input and output terminals of ICN15 is as follows.

GATE2 input (pin 16) :	Capstan 2FG (from pin 9 of ICA5)
CLK2 input (pin 18) :	7.3728 MHz clock (from pin 11 of ICM14)
OUT2 output (pin 17) :	Capstan analog velocity loop (to pin 4 of ICB5)
Preset value :	Depends on the adjustment value of the capstan velocity loop.

⑤ PG delay 1 (PTC-3 ICN12 : Channel 0/mode 5)
The delay of drum PG (preset value) is varied in steps of one wavelength of drum FG-B (approx. 220 μsec at the regular speed). The condition of the channel 0/mode 5 input and output terminals of INC12 is as follows.

GATE0 input (pin 11) :	Drum PG (from the CD-36 board)
CLK0 input (pin 9) :	Drum FG-B (from pin 12 of ICC4)
OUT0 output (pin 10) :	PG delay 2 (to pin 14 of ICN12)
Preset value :	Depends on the PG delay adjustment

⑥ PG delay 2 (PTC-3 ICN12 : Channel 1/mode 1)
The delay of drum PG which has been adjusted by the previously output PG delay 1 is accurately adjusted in 271 nsec steps. The condition of the channel 1/mode 1 input and output terminals of ICN12 is as follows.

GATE1 input (pin 14) :	PG delay 2 (from pin 10 of ICN12)
CLK1 input (pin 15) :	3.6864 MHz clock (from pin 10 of ICM14)
OUT1 output (pin 13) :	PG pulse (to pin 13 of ICN9 and pin 24 of ICG13)
Preset value :	Depends on PG delay adjustment

⑦ Tracking delay (PTC-2 ICN14 : Channel 0/mode 5)
The REF V signal is delayed in order to adjust the phase of the CTL signal. In the playback mode when the tracking control is pushed in (fixed), or in the recording mode, the delay is fixed at 1/2V. In the playback mode when the tracking control is pulled out (variable condition), the delay varies within the range 1/2V±1/4V according to the condition of the tracking control. The condition of the channel 0/mode 5 input and output terminals for ICN14 is as follows.

GATE0 input (pin 11) :	REF V (from pin 5 of ICJ5)
CLK0 input (pin 9) :	1.8432 MHz (from pin 9 of ICM14)
OUT0 output (pin 10) :	Tracking delay (to pin 14 of ICN14 and pin 1 of ICL8)

⑧ CTL REF clock generation
(PTC-2 ICN14 : Channel 1/mode 2)
The clock generator is reset by the CTL phase pulses input to the GATE0 terminal, and generates 19.2 kHz clock pulses. The generated clock pulses are used in the CF marker generator and the PB CTL phase measuring circuit. The condition of the channel 1/mode 2 input and output terminals of ICN14 is as follows.

GATE1 input (pin 14) :	Channel 0 (from pin 10 of ICN14)
CLK1 input (pin 15) :	1.8432 MHz (from pin 9 of ICM14)
OUT1 output (pin 13) :	CTL REF clock (to pin 10 of ICK9)

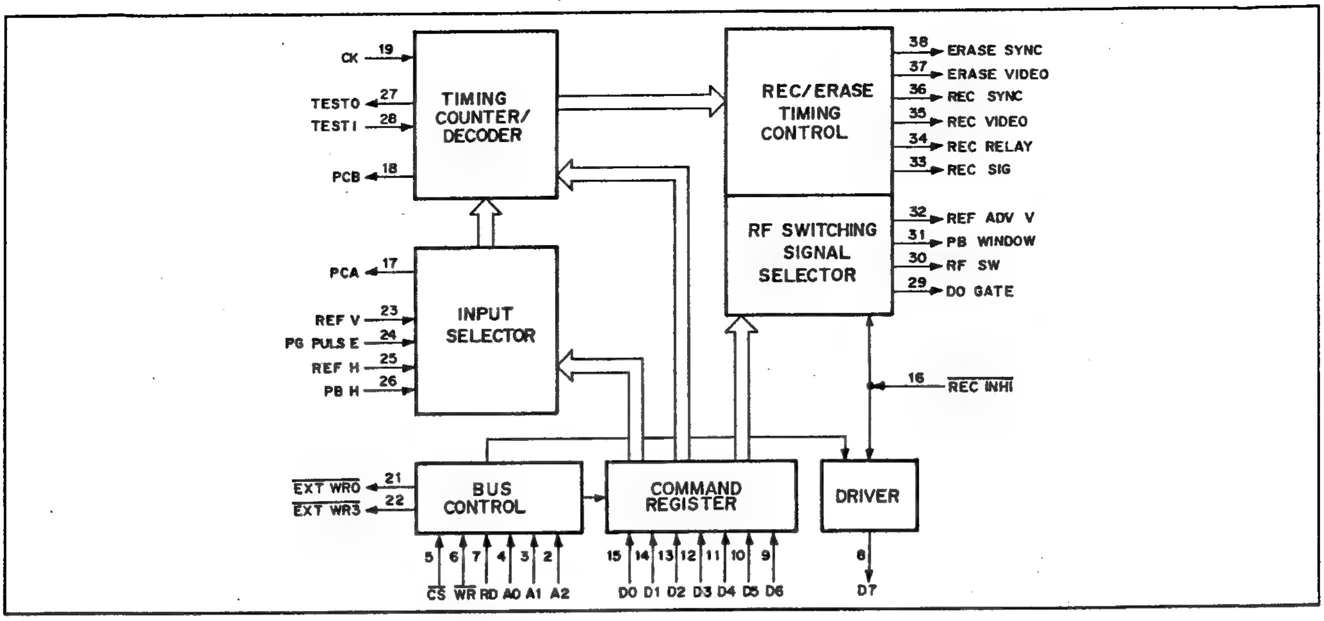


Fig. 4-6-5. Video Head Switching Logic (ICG13/SV-90)

(8) Video head switching logic (SV-90 board)

The video logic timing signals such as REC VIDEO, ERASE SYNC, and RF SW, are generated in ICG13 (CF77049N) on the SV-90 board.
The timing counter/decoder in ICG13 operate based on REF V (pin 23), PG pulse (pin 24), REF H (pin 25), and PB H (pin 26). Mode commands for the recording mode and head select are input to the command register in ICG13 from the main CPU via the data bus. The REC/ERASE timing controller and RF switching signal select circuit in ICG13 are controlled according to the control timing of ICG13 and also the mode command from the main CPU (ICK19).

(9) Reference pulse generator (SV-90 board)

This circuit generates the REF V signal and REF2 signal based on the SEL FRAME signal supplied from the RD-6 board (RD-7 board for the PS model), and also generates the REF4 and REF8 signals using the SEL CF signal.
The channel 1 of the ICL12 interval timer operates in mode 3, and outputs the 50% duty V×128 pulses from pin 13. ICK14 and ICJ10 divides the 128V pulses by 1/128, resulting in the REF V signal. In addition, the REF2, REF4, and REF8 signals are obtained by frequency dividing REF V in ICJ10.
The SEL FRAME signal supplied by the RD board and the REF 2 signal obtained by frequency dividing the 128V pulses output from ICL12 are synchronized as shown below.

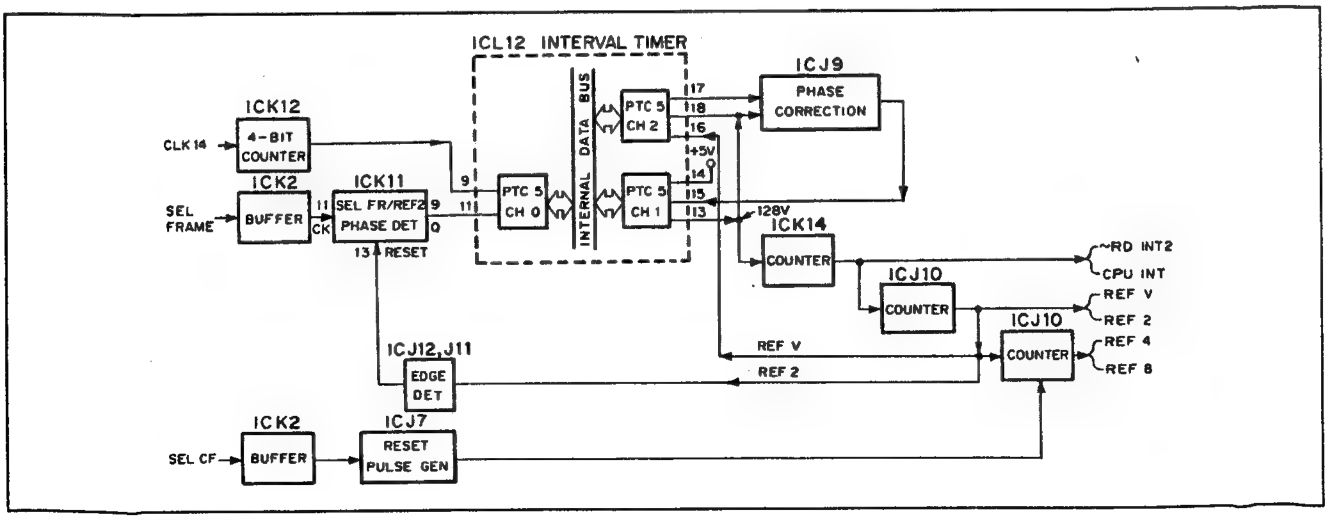


Fig. 4-6-6. Reference Pulse Generator (SV-90)

The SEL FRAME signal is input to pin 11 (clock terminal) of D flip-flop ICK11 via buffer ICK2. The REF2 signal is supplied to the reset terminal of ICK11 via the edge detection circuit consisting of NAND gate ICJ11 and latch ICJ12. The $\overline{\text{HREFMR}}$ signal output from pin 14 of address decoder ICK4 is input to pin 4 (set terminal) of ICK11, causing pin 12 (data input terminal) of ICK11 to be set to "H" level. As a result, a pulse of width equal to the period from the rising edge of the clock input to the rising edge of the reset input, that is, the phase difference between the SEL FRAME signal and the REF2 signal, is output from pin 9 (Q output terminal) of ICK11. The pulse width corresponding to the phase difference is measured at channel 0 of ICL12. In order to increase measuring accuracy, CLK14 (14.7456 MHz) is used as a clock in ICL12. In order to obtain 20-bit resolution, the lower 4 bits are measured by the 4-bit counter ICK12, and the upper 16 bits are measured by the 16-bit counter in ICL12. The measured phase data is applied to ICL12, and channel 1 of ICL12 is operated in mode 3, causing a 50% duty clock of frequency V×128 to be generated.
The generated 128V clock is frequency divided by counters ICK14 and J10, resulting in $\overline{\text{RD INT2}}$ of frequency V/32, CPU INT of frequency V/4, REF V of frequency V, and REF2 of frequency 2V. Counter ICJ10 which uses REF2 as the clock is reset by the SEL CF signal supplied from the RD board, and generates the REF4 and REF8 signals.
Channel 2 of ICL12, latch ICJ9 and NOR gate ICH10 operate as a phase adjustment circuit for the 128V signal. The clock input to the 128V signal generator circuit (channel 1 of ICL12) is gated by ICH10 and the number of clock pulses controlled, thus controlling the phase of the 128V signal.

(10) Sub CPU (SV-90 board)

The sub CPU (ICB15 : μPD78C10) is an 8-bit CPU which contains an A/D converter. It operates on the same 7.3728 MHz clock as that of the main CPU (ICK19). The sub CPU contains a 256 byte RAM. Also, an external 8k byte ROM (ICE15) and a 2k byte RAM (ICE16) are connected to it. RAM ICE16 is used as a common memory for communication with the main CPU.
Port A (PA7 to PA0) and port B (PB7 to PB0) of the sub CPU are general purpose input/output ports. Inputs and outputs can be specified in bit units. Port C (PC7 to PC0) functions as a general purpose input/output port, and can also be used as a control signal. In this unit, port C is used as an output port and also as a serial communication port. Port D (PD7 to PD0) is used as a multiplex address bus for an external memory. Port F (PF7 to PF0) is used as an input/output port and also as an address bus.
The data terminal (D7 to D0) of the RAM (ICE16) is connected to the data bus of the main CPU (ICK19) and the data bus of the sub CPU via bi-directional bus transceivers ICD17 and ICD16.
The switchover between ICD16 and ICD17 is performed by the V/4 rate CPU INT signal output from pin 5 of ICJ12, thus preventing a collision between the data buses of the main CPU and the sub CPU.
The address bus and the control signal of the RAM (ICE16) are selected by selector ICD13, ICE17 and ICF17. Also, switching between ICD13, ICE17 and ICF17 is performed by the CPU INT signal in the same way as the data bus.

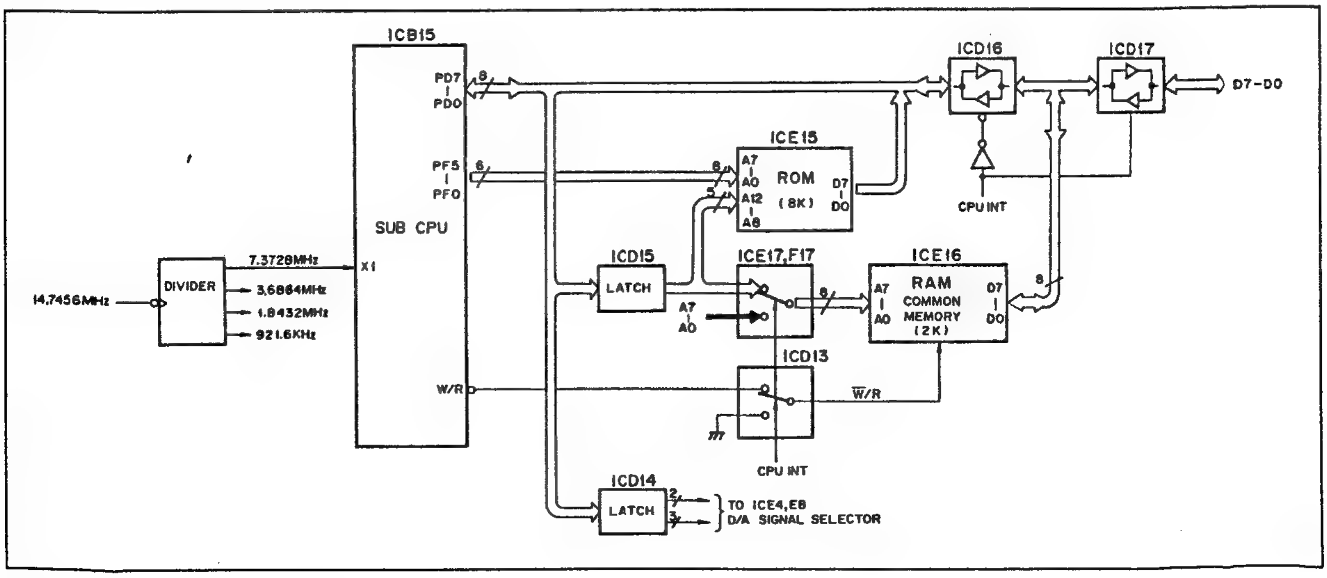


Fig. 4-6-7. Sub CPU (SV-90)

(11) D/A converter (SV-90 board)

The upper 12 bits of the 16-bit data processed in sub CPU ICB15 are supplied to the D/A converter (ICA16) from PB7 to PB0 and PA7 to PA4 of the sub CPU. The offset level of the analog signal output from ICA16 is adjusted by RV2 and the conversion gain adjusted by RV3. The resulting signal is current /voltage converted by IC11, and output to the analog switcher ICE4 and ICE8 in the next stage.
The analog signal which is output from the D/A converter is used not only as a motor driver signal but also as an offset compensation signal and a gain control signal. These analog data are stored in non-volatile memory IC1 on the mother board as data which indicate the mechanical characteristics of the tape transport system, and are read out when the CPU is initialized. After replacing a part such as the tension arm, change the adjustment data saved in the non-volatile memory IC1, using "T17. MAINTENANCE" of the setup menu.

4-6-3. Drum Servo System (SV-90 Board)

Each time the drum makes one revolution, 76 pulses of the FG (Frequency Generator) signal and one pulse of the PG (Pulse Generator) signal are generated. The 2-phase FG signals (DRUM FGA and DRUM FGB) are used for detecting the rotational speed and direction of the drum, and the DRUM PG signal is used for detecting the rotating phase of the drum.
The DRUM FGA and DRUM FGB signals which are supplied to the SV-90 board are converted to TTL level by ICC1, D1, and C4, and input to ICA5. ICA5 outputs the DIR signal which indicates the direction of rotation of the drum, and also the 2FG signal which has a frequency of twice that of the FG signal. The DIR signal is output from pin 3 of ICA5, then supplied to pin 64 (PB0) of the I/O expander (ICG15). The 2FG signal which is obtained by EX-OR gating in ICA5 is supplied from pin 15 of ICA5 to pin 16 (GATE2) of ICN12. When the CPU starts speed measurement, pulses of width 105 μ sec (388 clocks)

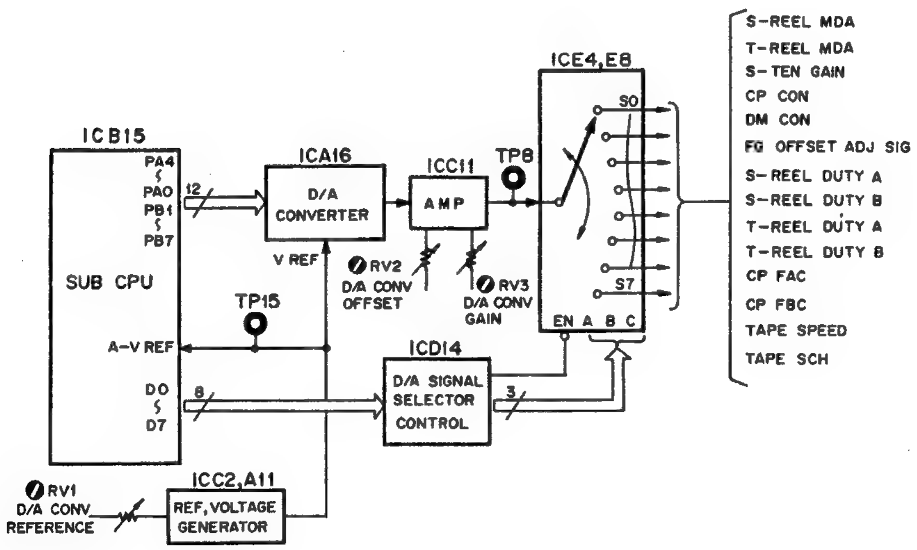


Fig. 4-6-8. D/A Converter (SV-90)

are output to pin 17 of ICN12. These pulses are used in the T/V converter circuit in the analog servo system.
The analog servo system converts the pulse width of the FG signal into a voltage, in the following way:
The 2FG signal output from pin 15 of ICA2 and also the output of pin 17 (OUT2) of ICN12 are AND-gated in ICB5. The pulse width of the OUT2 signal from pin 17 is 105 μ sec. This is equivalent to about 96% of the pulse width (109.6 μ sec) corresponding to normal speed. A pulse of width equal to the difference between the widths of both pulses is output from pin 3 of AND gate ICB5, and C14 is charged by constant current source Q3 for exactly the duration of this pulse. The voltage to which C14 is charged is applied to sample hold ICB7 in the next stage. The DRUM FGB signal is delayed by ICC5, ICB6 and ICB5 and input to pin 8 of ICB7.
ICB7 sample-holds the stabilized DC voltage obtained after C14 is charged rather than the voltage obtained while it is still charging. In this way, the width of the sample pulse can be increased, and a stable output obtained. C14 is charged each time a pulse of the double frequency FG signal is input, and immediately after ICB7 samples the charge voltage, C14 is discharged by analog switcher ICC7. Diode D5 operates as a limiter to limit the charging voltage of C14 to a maximum of +5V. The analog velocity error compensation voltage which was sample-held by ICB7 is added to the digital servo signal (DMCON), and output from pin 7 of ICD7. Analog switch ICC7 selects either the digital servo signal to which the analog velocity error compensation voltage has been added, or the digital servo signal to which the compensation voltage has not been added (DMCON).
The selected signal is amplified by operational amplifier ICD7, then supplied to the drum drive circuit of the CD-36 board as the DRUM MDA signal. ICC6 is a circuit which forcibly stops the drum motor while the analog velocity loop is operating, to prevent a negative voltage corresponding to a reverse command from being output as a DRUM MDA signal.
Each time the upper drum makes one revolution, a single pulse of the PG signal is output from the head drum. This pulse is converted to TTL level in voltage comparator IC16 on the CD-36 board, then supplied to the SV-90 board. The DRUM PG signal is generated when the magnet installed in the upper drum passes over the detector device in the lower drum. The magnet is installed slightly ahead (in terms of phase) of the R/P head for the video channel. The generated DRUM PG signal is electrically delayed to align it with the V phase of the R/P head output signal for the video channel. If the upper drum is replaced, adjust the delay of the DRUM PG signal from the control panel, using "T17. MAINTENANCE" of the test menu.
The SV-90 board applies a phase servo which maintains the correct phase relation between the REF V signal and the Delayed PG signal (consists of a delayed DRUM PG signal).

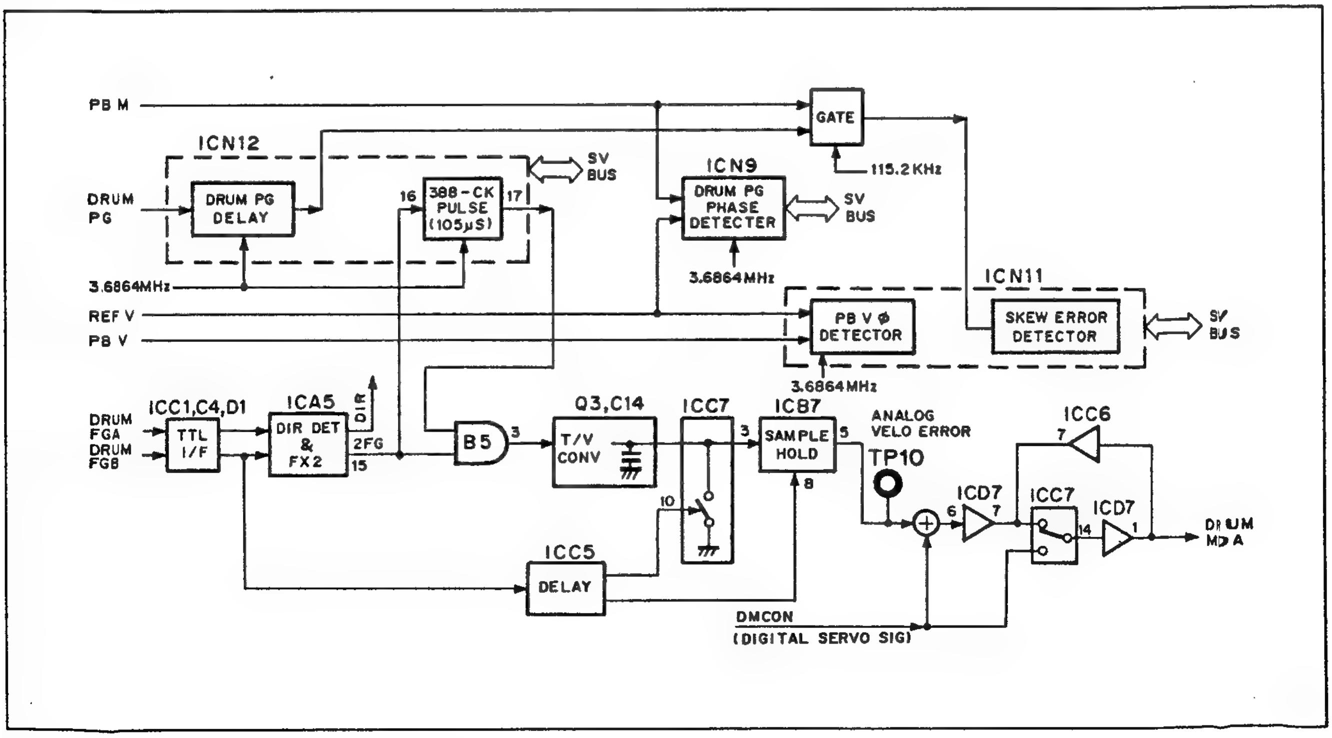


Fig. 4-6-9. Drum Servo System (SV-90)

4-6-4. Capstan Servo System (SV-90 Board)

The capstan servo has the following three purposes.

1. Fixing the tape speed during recording.
2. Aligning the phases of the CTL signal generated from the REF V signal, and the PB CTL signal played back from the tape, to ensure tracking during normal speed playback.
3. Controlling the tape speed during variable playback (−1 to +3 times normal speed).

The above control takes place when the pinch roller is pressed against the capstan (ON). Like the drum servo, the capstan servo is divided into a digital servo area and also analog velocity loop. The analog velocity loop is used in the PLAY, REC, and P-PLAY modes, and the digital servo is used in the variable mode. In the ultra low speed variable mode, the interval between FG pulses increases, hence the FG pulses are A/D converted in the sub CPU, utilizing the fact that the FG signal is a sine wave, and from the resulting data the rotational speed is calculated to a greater degree of precision.
The 2-phase FG signals, of which 96 pulses are output each time the motor makes one revolution, pass through operational amplifiers ICA1 and B1, and buffer amplifier ICB4, then to signal selectors ICF11 and F10 for the D/A converter of sub CPU ICB15.

The DC offset compensation voltages (CPFAC and CPFBC) of the motor FG output are applied to the FG input terminals of ICA1 and ICB1. The offset compensation voltage data is stored in the non-volatile memory (IC1) on the mother board, and is supplied via sub CPU ICB15 and D/A converter ICA16. The outputs of operational amplifiers ICA1 and B1 are supplied to voltage comparator ICA4. FGA and FGB which are output from ICA4 are supplied to the motor rotational direction detection circuit (ICA5).
The following signals are output from ICA5.

- DIR (pin 6) :

This signal indicates the direction of rotation of the motor. It is supplied to port PB1 of I/O expander ICG15.

- 2FG (pin 9) :

This signal, which is obtained from the EX-OR gate of FGA and FGB is twice the frequency of the FG signal. It is supplied to channels 1 and 2 of PTC4/ICN15 and also the analog velocity loop.

- 4FG (pin 5) :

This signal is obtained by sampling FGA and FGB with the 921.6 kHz clock input to pin 7, then EX-OR-gating them, and outputting pulses of one clock width at each rising and falling edge. Consequently, the frequency of this signal is four times that of FG. This 4FG pulse is supplied to channel 0 of PTC4/ICN15.

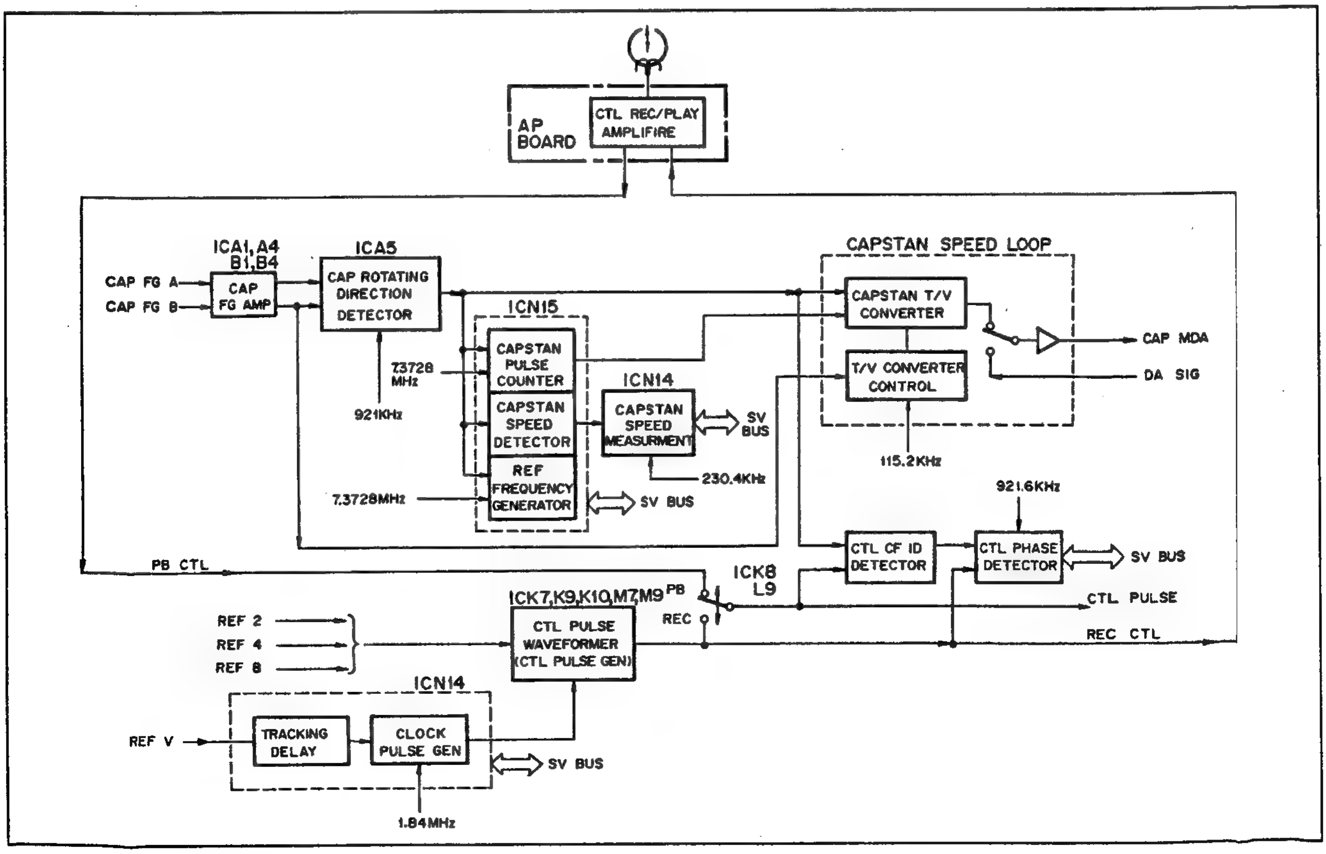


Fig. 4-6-10. Capstan Servo (SV-90)

4-6-5. CTL Processing System (SV-90 Board)

The CTL signal is recorded and played back by the stationary head. The recording amplifier and playback amplifier are located on the AP-15 board. The circuit which detects the color framing data and CTL phase from the CTL signal is located on the SV-90 board.

(1) CTL pulse generator (SV-90 board)

The CTL signal is obtained by delaying the REF2 signal created from the servo reference signal by the specified phase then inserting a color frame marker into it.
The REF2 signal is input to latch ICK10 together with the REF4 signal and REF8 signal which contain the color frame information. The time difference (tracking delay) between the input data and output data of latch ICK10 depends upon the timing of the rising edge of the clock signal input to pin 9. In other words, the CTL phase is determined by the phase of the clock signal.
The clock signal is generated at channel 0 of PTC-2/ICN14.The phase of the clock signal is determined by delaying the phase of REF V input to pin 11 (GATE 0) of ICN14 by an interval determined by the CPU.
The counter in ICN14 is preset by CPU ICB15. This preset value, that is, the clock delay, is fixed during recording, and depends on the setting of the tracking control on the level control panel during playback. The adjustment value set by the tracking control, that is, the preset value, is A/D converted by sub CPU ICB15. The A/D converted preset value is processed by software, then preset in the counter used in channel 0 of ICN14.

(2) Color frame marker generator (SV-90 board)

The color frame marker is a signal which indicates the phase relation between the sub carrier of the recording signal and the H sync signal. If the phase relationship between SC and H changes, the continuity of the sub carrier will be lost, that is, color framing will get out of step, which may cause misoperation of the time base corrector.
Color frame detection is performed by the RD board. The SEL CF signal which indicates the result of detection is input to the SV-90 board. At the SV-90 board, reference pulse signals REF4 and REF8 which contain color frame data are generated based on the CF signal, and are latched together with REF2 by ICK10. The REF2 and REF4 outputs from latch ICK10 are AND-gated by ICK7 to become a color frame marker window for an NTSC signal. ICK9, ICL9 and ICM9 constitute a marker pulse generator circuit. The output from this circuit is AND-gated with REF2 and REF4 by ICK7, resulting in a color frame marker signal for an NTSC signal at pin 12 of ICK7. This color frame marker is input to pin 11 of ICK7, then gated by the REF8 signal output from pin 7 of ICK10, resulting in an 8-field sequence color frame marker signal for a PAL signal.
Channel 1 of ICN14 is a clock generator used for marker pulse generation. The REF V signal which is delayed in channel 0 is input to the GATE 1 terminal, and a 19.2 kHz clock which is reset at that timing is output from OUT1. This clock is frequency divided by counter ICK9, resulting in the timing signal for the marker pulse generator circuit.

4-6-6. Reel Servo System (SV-90 Board)

The reel servo system performs control to obtain a stable tape tension regardless of the mode in which the VTR is operated. The reel servo system uses the maximum software area for the servo system, and performs the following processing using the CPU.

1. Detection and control of tape winding diameter.
2. Tape speed control from very slow, such as in the JOG mode, to a maximum of 50 times normal speed, as in the SHUTTLE mode.
3. Detection and control of load fluctuations due to differences in tape length and reel diameter.

Data concerning the rotational speed and direction of rotation of the reel motor are obtained from the FG signal. The FG signal is output at the rate of 700 pulses per revolution of the reel motor, converted to TTL level at the RM-43 board, then sent to the SV-90 board.
The direction of rotation is detected by ICH6 using S and T reel FG signals. The speed of rotation of the S reel is detected by channel 0 of timer counter PTC-0/ICN17, and that of the T reel is detected by channel 1.
The T reel motor is controlled by an open loop. The data calculated by the CPU from the tape diameter and the rotational speed of the motor is D/A converted to become the T-REEL MDA signal. This signal is input to the T reel motor drive circuit on the RM-43 board, causing the T reel motor to be driven so that the tape tension is the correct value for each mode.
The S reel motor is controlled by a similar open loop to that used for the T reel motor, and also by a feedback loop which maintains the tape tension detected by the tension arm constant. The tension arm signal amplifier circuit (ICG2 and G4) also functions as a filter which removes the inherent vibration component due to the tension arm from the tension arm signal.

4-6-7. Skew Detector (SV-90 Board)

Skew is a phenomenon whereby the tape stretches or contracts due to changes in ambient temperature and tape tension during recording and playback, causing the playback time per field to vary, which in turn results in distortion at the top of the monitor screen.

The output from pin 10 (OUT 0) of PG delay 1 circuit ICN12 is supplied to ICH8, the window pulses obtained are latched in ICM10 by the PB H signal, and the output pulse width is measured in the B channel of ICN11. Although the pulse width of the PB H signal is measured, the width of the window is made 1.38 msec (21H+ α) because if only one period of H were to be measured the effect of velocity errors would become significant and also the amount of change would be very small, making measurement difficult.

4-6-8. Servo Reference Signal Generator (RD-6/RD-7 Board)

(1) Input select circuit and video amplifier (RD-6/RD-7 board)

In the servo reference section, the signals input to the VIDEO INPUT terminal and the REF VIDEO INPUT terminal of the connector panel are 0.5 Vp-p. One of these signals is selected by the "S40. SERVO REF SELECT" select menu. The selected signal is amplified by a factor of about 7 to 8 by the video amplifier in the next stage.

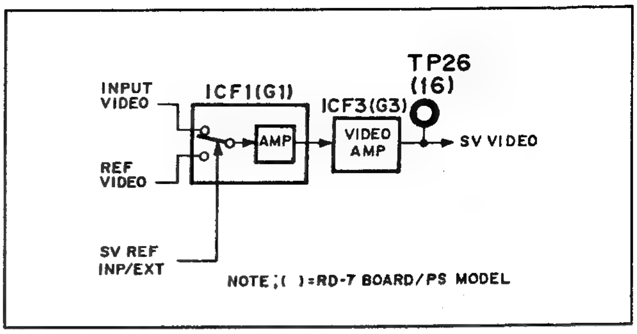


Fig. 4-6-11. Input Selector and Video Amplifier (RD-6/RD-7)

(2) Sync separator (RD-6/RD-7 board)

This circuit separates the sync signal, which is used for frame detection and SC-H phase detection, from the video signal.

The Y signal is taken off from the SV video signal (servo reference signal), which is output from the video amplifier, by a low-pass filter, and the pedestal level is clamped to 0 V by Q15 (Q3). Next, the sync tip is sample-held by ICF9 and IC2 (ICG8 and G9), and the level of the sync signal detected. The level of the detected sync signal is voltage-divided by resistors, resulting in a voltage of 1/2 the sync signal level. The sync signal is separated by comparing the Y signal, the pedestal of which is clamped to 0V, and the 1/2 sync tip level voltage in voltage comparator ICF13 (ICG10).

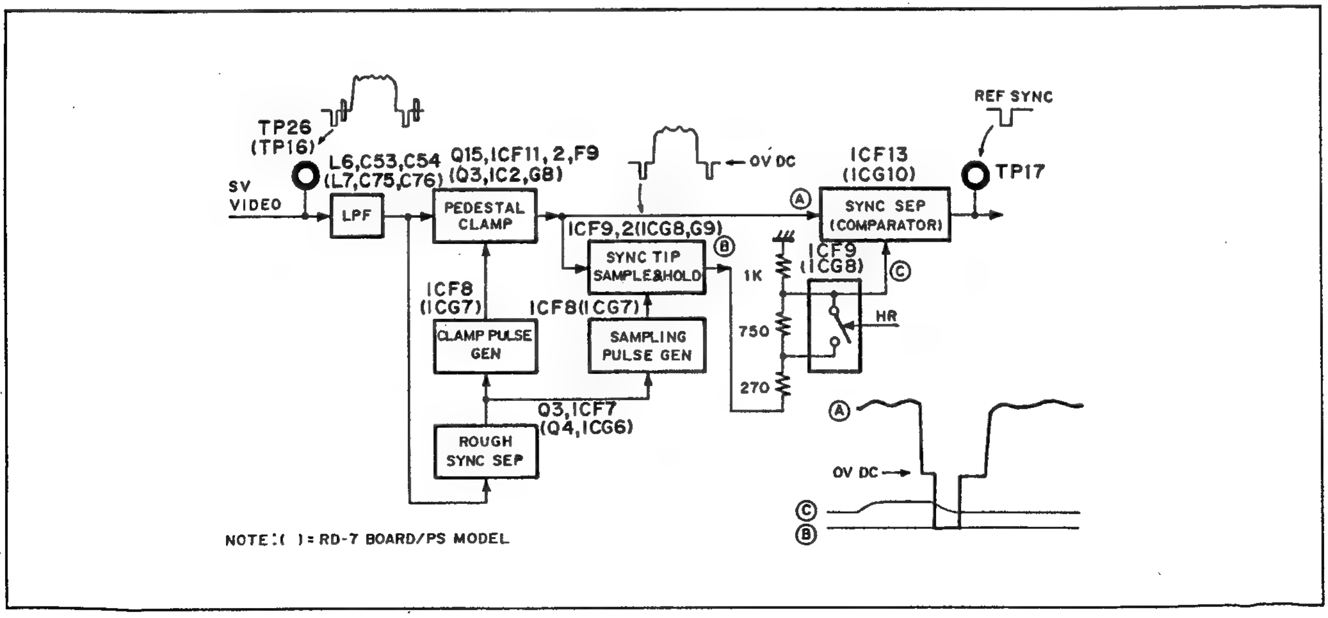


Fig. 4-6-12. Sync Separator (RD-6/RD-7)

ICF9 (ICG8) switches the voltage division ratio of the sync signal level. The voltage compared in ICF13 (ICG10) approaches the sync tip level other than at the leading edge of the sync signal, thus providing noise immunity.
ICF7 (ICG6) is a rough sync separator. Clamp pulses and sync tip sampling pulses are generated from the sync signals generated here.

(3) Burst APC (4Fsc VCO) (RD-6/RD-7 board)

This circuit generates a continuous subcarrier locked to the burst signal, in order to detect the SC-H phase. The signal from the video amplifier is passed through a bandpass filter where the chroma component is taken off, then converted to TTL level by a zero-cross detector. The converted signal is input to PLL, resulting in a continuous 4Fsc signal which is locked to the burst signal. This signal is frequency divided by 1/4, then supplied to the SC-H phase detection circuit as a signal which indicates the SC phase.

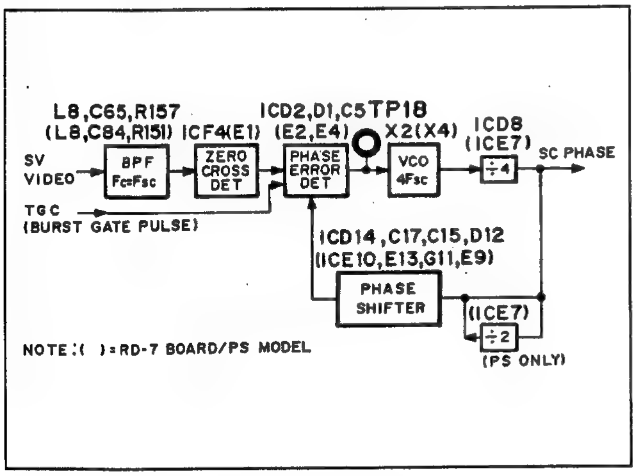


Fig. 4-6-13. Burst APC (RD-6/RD-7)

(4) Field 1/2 detection : NTSC model (RD-6 board)

When the REF SYNC signal is input to pin 15 (EXT SYNC terminal) of ICD9 (CX7903), the VR (REF V) signal is output from pin 7, and the HR (REF H) signal is output from pin 6. The VR signal is output at the fall timing of the 1st pulse in the vertical sync pulse interval. The VR signal is frequency divided by 2, resulting in the REF FRAME signal. Since the REF FRAME signal must be "L" in the 1st field interval, field 1/field 2 is detected and the detector output resets the frequency divider. Field 1/field 2 detection takes place utilizing the fact that the phase relationship between the VR signal and the HR signals in the 1st and 2nd fields are different.

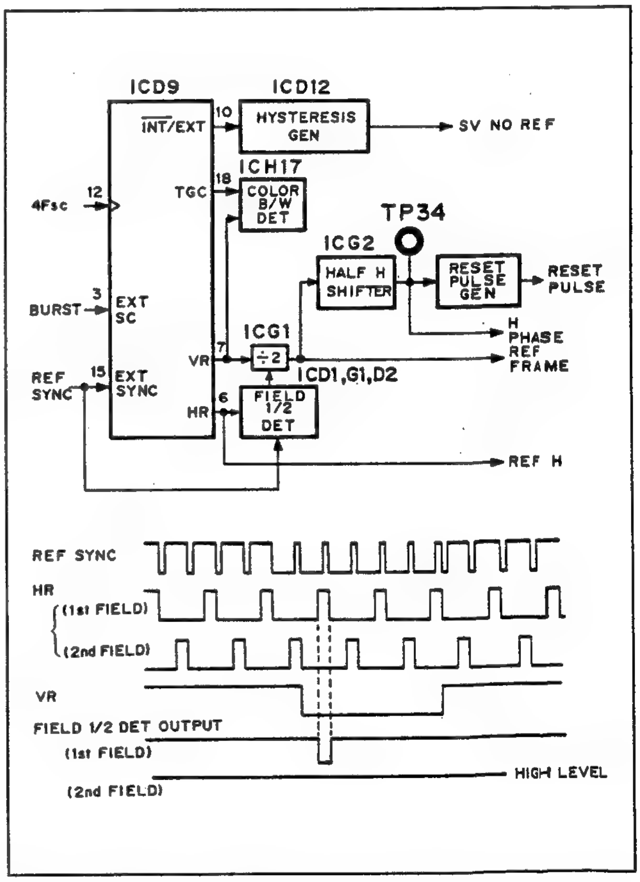


Fig. 4-6-14. Field 1/2 Detector : NTSC Model (RD-6)

(5) Field 1/2, 1/3 detection : PS model (RD-7 board)

Field 1/field 2 detection takes place in a similar way to that of the NTSC model. In the PS model, the REF FRAME signal obtained by field 1/field 2 detection is once again frequency divided by 2, and field 1/field 3 detected. The field 1/3 detection formats for PAL and SECAM are different. In the case of PAL, the field is judged according to whether or not the burst signal of line 6 exists (if there is a burst signal, the field is field 3) ; in the case of SECAM, detection, the field is judged according to whether or not the ID signal of line 8 is DR or DB (if it is DR, the field is field 3).

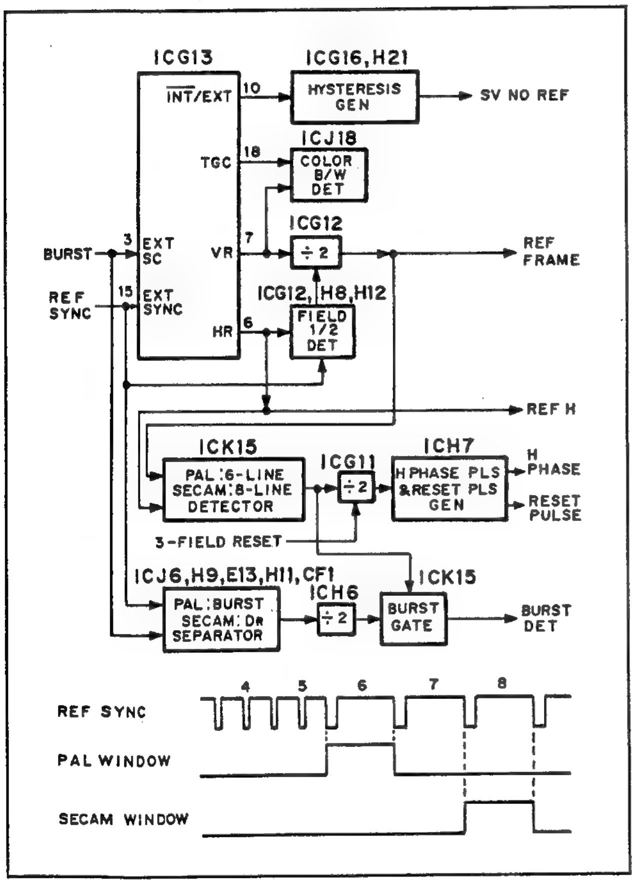


Fig. 4-6-15. Field 1/2 and 1/3 Detectors : PS Model (RD-7)

(6) SC-H phase detection (RD-6/RD-7 board)

The SC-H phase is detected by measuring the phase difference between the falling edge of the H PHASE signal and the SC PHASE signal. The H PHASE signal is inverted at the following timing each field (or every second field in the case of the PAL format).

- NTSC : Fall of the 3rd vertical sync pulse
- PAL : Fall of H sync of line 9

SC PHASE is the output signal of burst APC. The pulses of this signal are generated at the same frequency as the sub carrier.

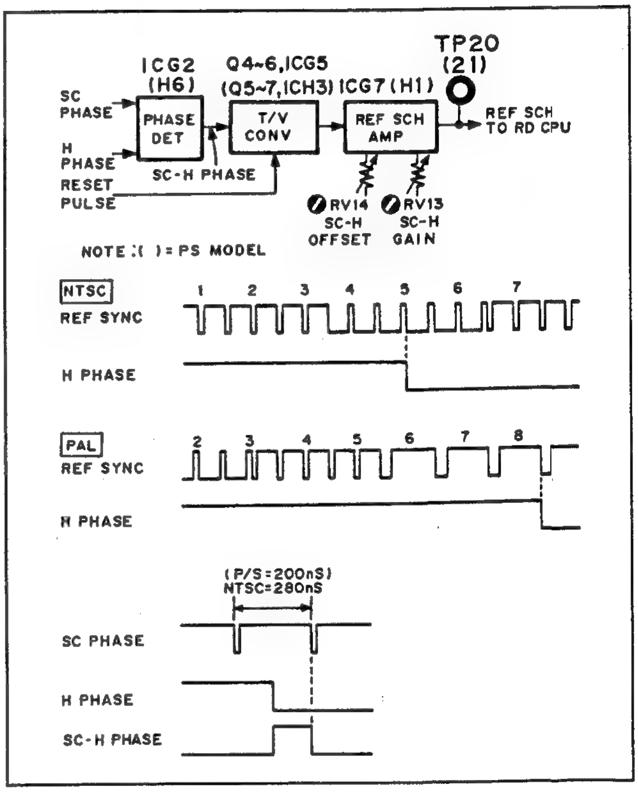


Fig. 4-6-16. SC-H Phase Detector (RD-6/RD-7)

The phase difference between H PHASE and SC PHASE (SC-H PHASE signal) detected by ICG2(ICH6) is T/V converted and adjusted so that the voltage is 0V at −180° and 5V at 180°, where the period of the sub carrier is defined as 360°. In the NTSC signal, if the SC-H phase of field 1 is 0°, the phase of field 3 will be 180° (in the PAL signal, the phase of field 5 is 180°), hence the voltage of the waveform at this time will be 2.5V for fields 1 and 2 (or fields 1, 2, 3, and 4 in the case of the PAL signal), and 0V or 5V for fields 3 and 4 (or fields 5, 6, 7, and 8 in the case of the PAL signal). By inputting a reference signal so that the SC-H phase of field 1 becomes 0, and carrying out the abovementioned adjustment, a voltage waveform which always matches the SC-H phase will be obtained.

This waveform (REF SCH) is input to the analog port of the CPU and the voltage measured and displayed on the SC-H meter on the meter panel. At the same time, field 1/field 3 detection (or field 1/field 5 detection in the case of the PAL signal) takes place.

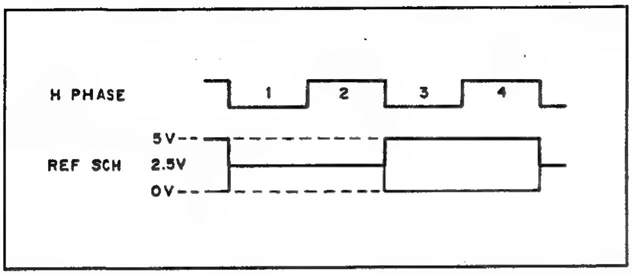


Fig. 4-6-17. SC-H Phase T/V Conversion Level: NTSC (RD-6)

The 4-field sequence of the NTSC signal, and the 8-field sequence of the PAL signal, are prescribed as follows.

NTSC signal (U.S. EIA RS-170A)
The field at which the phase of the subcarrier at the center of the falling edge of H sync of line 10 is 0° is defined as field 1, and a phase difference of up to ±40° is allowed.

PAL signal
The field at which the phase of the subcarrier which has the same phase as the U axis color signal at the center of the falling edge of H sync of line 1 is 0° is defined as field 1, and a phase difference of up to ±90° is allowed.

In both the NTSC and PAL signals, the RD board judges the field in which the SC-H phase is ±70° to be field 1, and outputs the SV CF signal. Also, the range of field 1 can be changed to "−25° to +115° " or "−125° to +25° by setting "S43. SERVO CF DET SHIFT" of the menu to either "+45 DEG" or "−45 DEG".

4-7. SYSTEM CONTROL AND TIME CODE SYSTEM

The main circuitry configuring the system control and time code system is housed on the SY-103 board and control panel. The SY-103 board has the following functions.

(a) Control of the man/machine interfaces and interfaces such as that with an editor (system control)
(b) Time code reader/generator and its control

The above circuitry operates independently. The function described in (a) is carried out by the CPU on the SY-103 board while the function in (b) is controlled by the CPU on the SV-90 board. The time code system circuitry on the SY-103 board can be considered as part of the SV-90 board.

4-7-1. System Control Circuit (SY-103 Board)

CPU ICH14 on the SY-103 board serves to receive both the control signals from the external equipment which are supplied to the REMOTE-1, 2A and 2B connectors and the button signals from the control panel, convert these signals into the VTR control signals and write the data into common RAM ICJ3 which is used for communication with the CPU on the SV-90 board. CPU ICK19 on the SV-90 board serves to decode the commands from the SY-103 board into port information for each of the boards and to transfer this information to the video/audio/TBC and other boards.

(1) CPU and its peripheral circuits (SY-103 board)

In the CPU on the SY-103 board, the internal 16-bit/external 8-bit V20 (μ PD70108D-8) is used in the minimum mode. The 64k-byte ICH11 and ICH12 are used as the external ROMs of the CPU. The 8k-byte ICH10 is used as the external RAM. The 7.3728 MHz frequency signal from ICG14 is used as the CPU clock signal.
The signal with a 14.7456 MHz frequency is divided by ICG13 and ICF14 and used for the peripheral ICs of the CPU. The signal with the 0.3072 MHz frequency in the clock signal provided is further divided down by ICF14 and ICF15 and "READY" display LED D8 is controlled. While ICF14 and ICF15 are counting, D8 blinks on and off at a frequency of 9.375 Hz (106.67 msec). If the counter reset signal from the CPU which is supplied to pins 7 and 15 of ICF15 is interrupted, D8 goes off after approximately 53.3 msec.
In order to read and write data into a slow device from the CPU, a READY signal is generated by ICG12 so that the CPU is made to wait for the equivalent of a clock cycle and this signal is supplied to the RDY1 pin of ICG14. The waiting request signal is supplied to the RDY2 pin of ICG14. In order for the CPU to be made to wait, RDY2 must be off (low level).

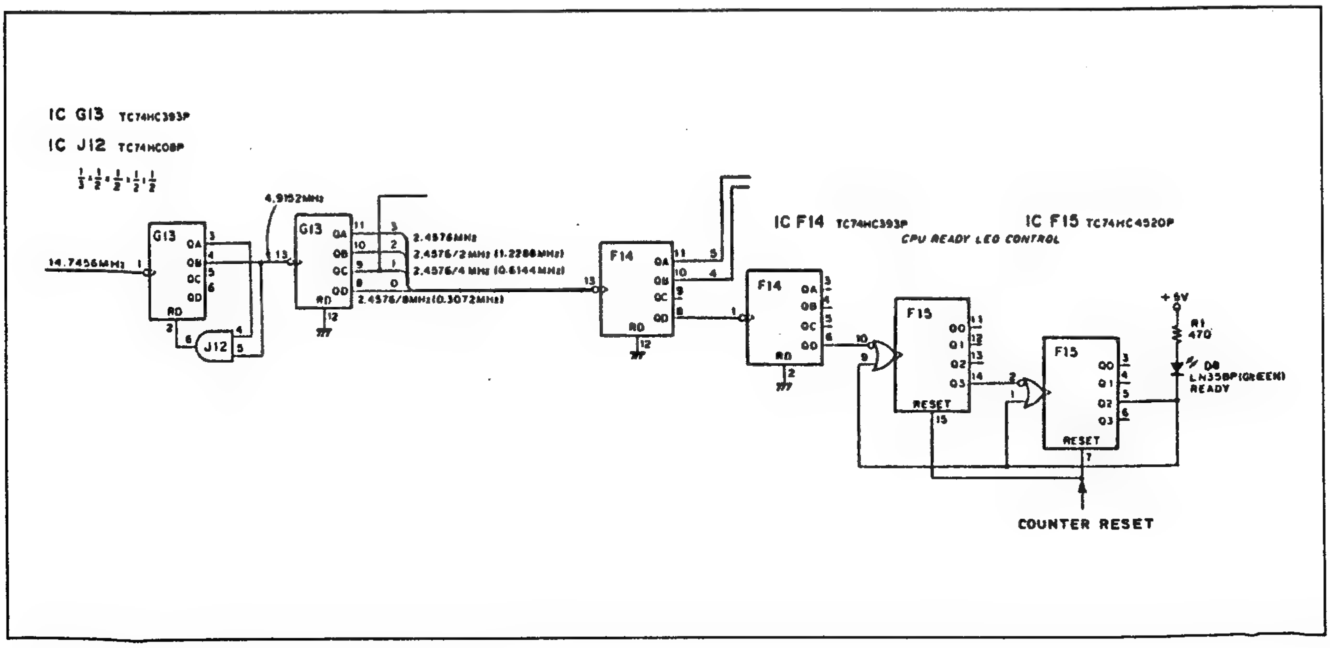


Fig. 4-7-1. Clock Frequency Divider (SY-103)

The timing operations shown in Fig. 4-7-2 are described in detail below.

(a) Since the RDY2 pin (pin 6) of ICG14 is on (high level), the READY pin (pin 5) is also set high and there is no CPU transition to the waiting operation. The CPU enters the READY state only when pins RDY1 and RDY2 are both low.

(b) The RDY2 pin is off (low level) and so READY control is enforced.

(c) The READY signal is now transferred to the CPU. At the timing of the clock T2 fall edge, the CPU checks whether the waiting request is present.

(d) RDY1 is reset after a half clock cycle has elapsed and ICG14 is advised of the termination of READY control. RDY1 is used with each CPU cycle in order to control the waiting which is equivalent to a clock cycle. At the timing of the clock Tw rising edge, the CPU judges whether it should exit or not from the waiting status.

(e) It is now detected that RDY1 is set to high level and the READY status is set on after a half clock cycle.

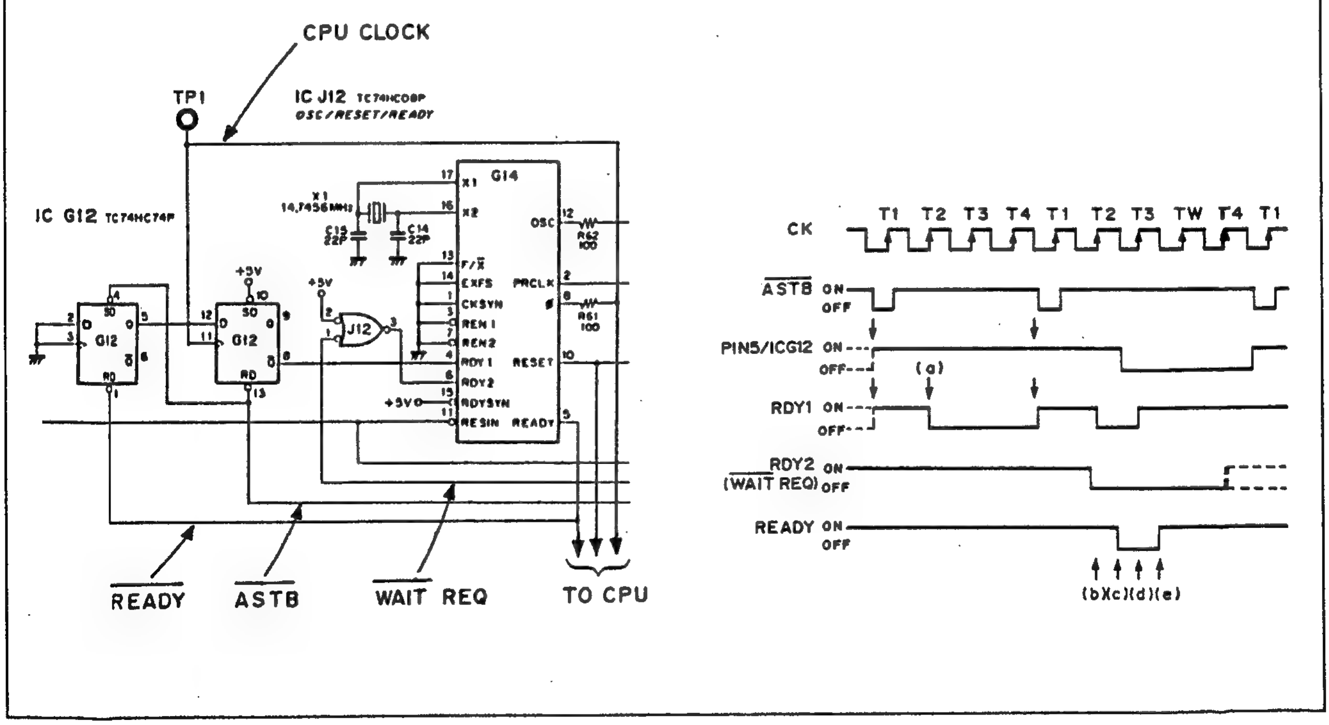


Fig. 4-7-2. Waiting Control Circuit (SY-103)

(2) Address decoder (SY-103 board)

The address decoder is composed of ICK9, K10, K11, K12, J10 and J12. Table 4-7-1 shows the addresses of the various devices mounted on the SY-103 board. The ICH12 (ROM0) addresses are separated into 0000H–3FFFH and C000H–FFFFH so that the start addresses at the time of resetting and the interrupt table can be housed in the same ROM. The reason for this is that if the two sets of addresses are separated in the two ROMs, then the probability that the CPU will operate out of control when a ROM error is detected is doubled, and difficulties arise in remedying the error.
ICH11 (ROM1) has a bank selection capability and two 16k-byte ROM areas.
ICH10 (RAM0) has an 8k-byte memory size. The contents of this RAM are not backed up and all its data will be lost when the power is turned off.
ICJ3 (common RAM) also has an 8k-byte memory size although in actual fact only 2k bytes of this capacity are used. The common RAM is backed up by C38 and data can be retained for at least one week.
Each of the ICH7, H8, J9, H6 and F13 CPU peripheral ICs are allocated a 1k-byte address area although the maximum address area actually used by the software is 9 bytes. Table 4-7-2 lists the peripheral IC addresses.

ADDRESS	CATEGORY	
0000H–3FFFH	ICH12 ROM0 LOWER BYTE	
4000H–7FFFH	ICH11 ROM1 BANK0	ICH11 ROM1 BANK1
8000H–9FFFH	ICH10 SELF RAM	
A000H–A7FFH	ICJ3 COMMON RAM	
A800H–ABFFH	ICH7	
AC00H–AFFFH	ICH8	
B000H–B3FFH	ICJ9	
B400H–B7FFH	ICH6	
B800H–BBFFH	NOT USED	
BC00H–BFFFH	ICF13	
C000H–FFFFH	ICH12 ROM0 HIGHER BYTE	

ADDRESS	CATEGORY
BC00H	PA0–PA7 (INPUT)
BC01H	PB0–PB7 (INPUT)
BC02H	PC0–PC7 (OUTPUT)
BC03H	PD0–PD7 (OUTPUT)
BC04H	PX0–PX3 (OUTPUT)
BC05H	REGISTER 1
BC06H	REGISTER 2
BC07H	NOT USED (DON'T USE)
BC08H	RESET START TRIGGER

Table 4-7-1. Address Map (SY-103)

REF NO.	ADDRESS	FUNCTION
ICH7 (RS-422)	A800H A801H A802H A803H	A-CH I/O DATA A-CH CONTROL REGISTER B-CH I/O DATA B-CH CONTROL REGISTER
ICH8 (COUNTER)	AC00H, AC01H AC02H, AC03H AC04H, AC05H AC06H	COUNTER-0 PRESET WORD DATA COUNTER-1 PRESET WORD DATA COUNTER-2 PRESET WORD DATA CONTROL WORD REGISTER
ICJ9 (INTERRUPT CONTROLLER)	AC00H AC01H	CONTROL REGISTER FOR A0=0 CONTROL REGISTER FOR A0=1
ICH6 (RS-232C)	B400H B401H	SERIAL I/O DATA CONTROL REGISTER
ICF13 (I/O)	BC00H–BC08H	SEE TABLE 4-7-1.

Table 4-7-2. Address Map of Peripheral CPU ICs (SY-103)

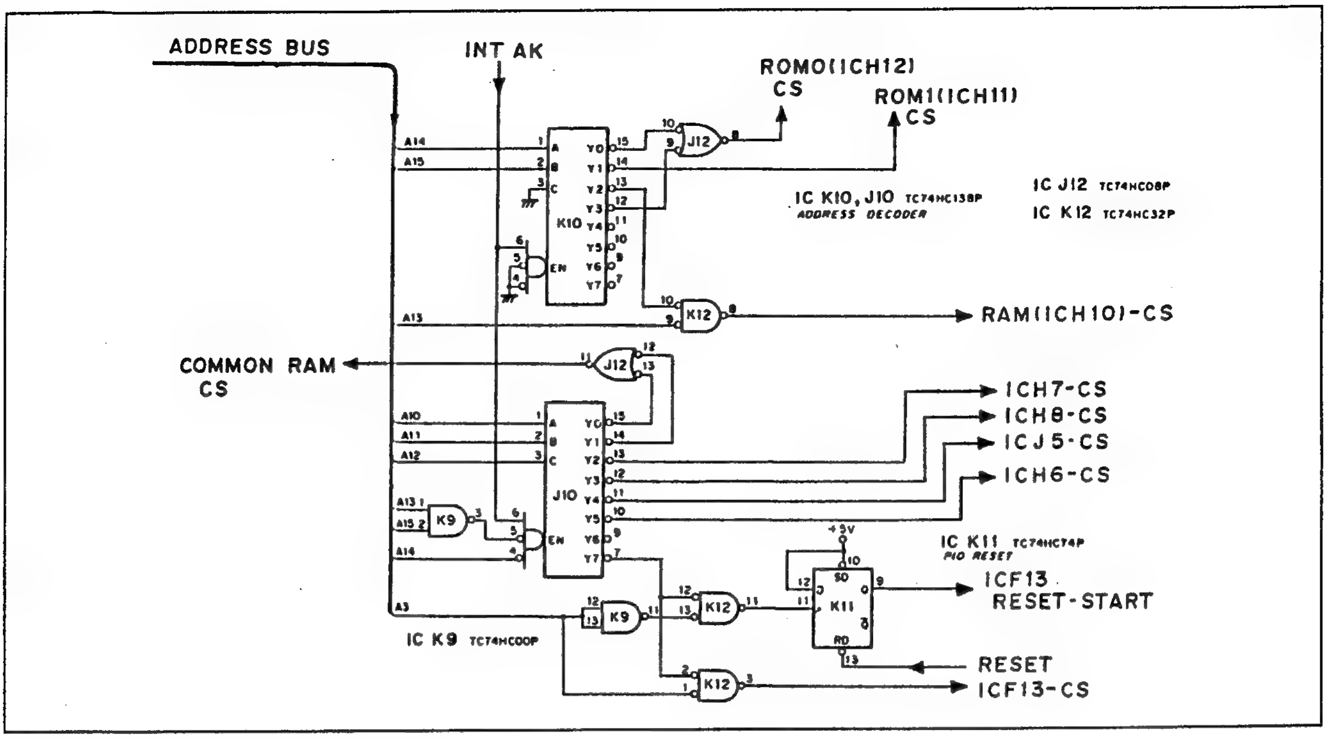


Fig. 4-7-3. Address Decoder (SY-103)

(3) Common memory and peripheral circuitry (SY-103 board)

Interfacing between the SY-103 board and SV-90 board is provided by common memory (RAM) ICJ3. In order for the common RAM ICJ3 to be accessed from both the CPU on the SY-103 board and the CPU on the SV-90 board, one CPU must be made to wait while the RAM is being accessed by the other. For instance, when the CPU on the SY-103 board is to access the common RAM, pin 5 of gate ICG10 is set high by the "~COMMON MEMORY REQUEST" signal created from the output of pins 14 and 15 of address decoder ICJ10. Since common RAM ICJ3 is not being accessed from the SV-90 board, the "~CM CS" signal of pin B18C on the SY-103 board is set high (inactive) and pin 4 of ICG10 is set high. Consequently, pin 8 of flip-flop ICG10 is set high and pin 11 (TP5) of ICG10 is set low.
The high level output of flip-flop ICG10 pin 8 is supplied to common RAM address selector ICH2, H3 and H4 through pin 2 of inverter ICF7, and the SY-103 board address bus is selected. Further, the pin 8/ICG10 output passes through inverter pin 12/ICF7 and gate pin 11/ICF5 to set bus buffer pin EN/ICK1 to high (disable) and isolate the SV-90 board data bus from the common RAM data bus. The low level which is output from pin 11 (TP5) of flip-flop ICG10 sets pin EN of bus buffer ICJ4 to low (enable), thereby connecting the SY-103 board data bus to the common RAM.
When the SY-103 board CPU is accessing the common RAM, the "~CM CS" signal from the SV-90 board is supplied to pin B18C on the SY-103 board if the SV-90 board CPU has attempted to access the common RAM. The "~CM CS" signal passes through pin 10 of inverter ICH1 to set pin 1 of ICG10 to high. However, since pin 8 of flip-flop ICG10 has been set high, pin 8 of ICF8 is set low, the signal returns to the SY-103 board from pin B18a on the SY-103 board as "~SV WAIT" and the SV-90 board CPU is set to the waiting status.
When the SY-103 board CPU has finished accessing the common RAM, the "~COMMON MEMORY REQUEST" signal created from the output of pins 14 and 15 of address decoder ICJ10 is set high and the flip-flop ICG10 status is inverted. If the "~CM CS" signal from the SV-90 board is active at this time, the common memory is accessed by the SV-90 board CPU.

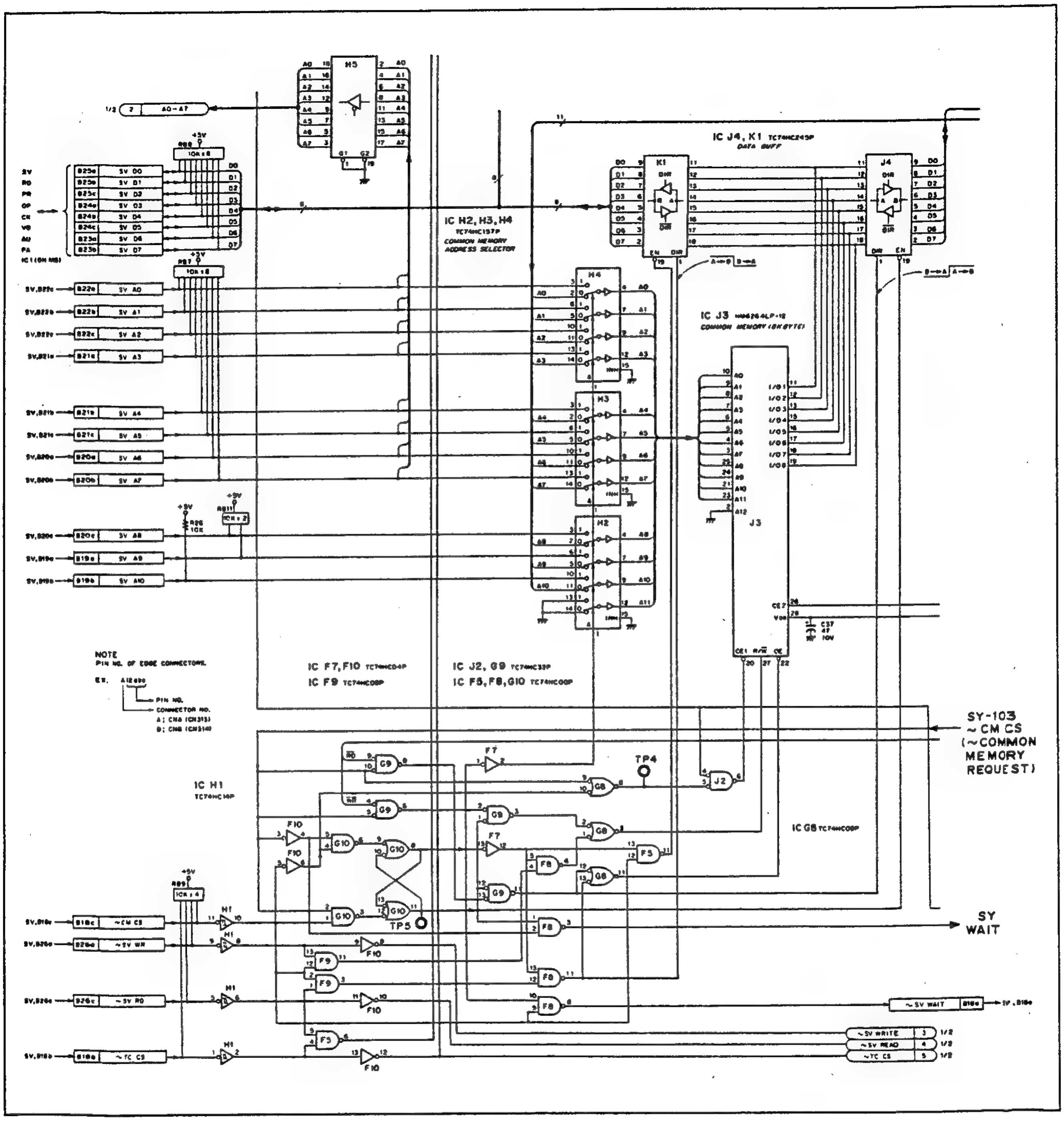


Fig. 4-7-4. Common RAM (SY-103)

The common RAM ICJ3 power supply is backed up by capacitor C38 so that the data are retained for more than 1 week even when the the VTR power is switched off.
When the power switch is set on, a +5V or +12V voltage, whichever is made available faster, is supplied to C38 and C38 is charged by the voltage equivalent to the +5V voltage minus the D3 forward voltage (max. 1.3V). Applied to the D4 anode is the voltage equivalent to +5V plus the D4 forward voltage (max. 0.8V). A common connection is featured for the D4 and D5 anodes and so the voltage drop at both is identical. This means that C38 is charged through the +12V until the D5 cathode voltage reaches +5V and the common RAM ICJ3 is backed up.

When the power switch is set off, the +5V voltage drops, the Q1 base voltage also drops and Q1 goes off. As a result, the voltage at the common RAM CE pin falls below 0.4V before the CPU supply voltage drops below the operating range, and the common RAM retains its data.

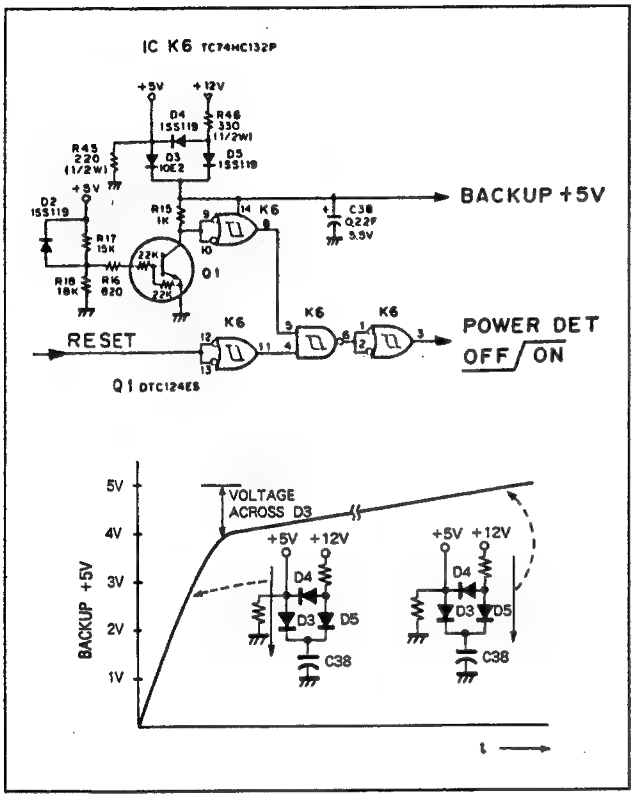


Fig. 4-7-5. Common RAM Back-up Circuit (SY-103)

(4) Interrupt controller (SY-103 board)

Interrupt controller ICJ5 (μ PD71059) can accept 8 types of interrupt request signals. In order to enhance the program efficiency, the interrupt request signals are allocated as shown in Table 4-7-3. The sequence of priority for the interrupts is defined by the software as "INT P7→INT P0→INT P1→···→INT P6." The RS-422 interrupt based on INT P7 is given top priority so that the commands from the remote controller are not lost. ICJ5 and ICH7 stand in a master/slave relationship, and the interrupt vectors based on INT P7 are generated by ICH7. In other words, when the INT P7 interrupt is requested, ICJ5 merely issues the interrupt request to the CPU and the actual interrupt vector is generated by ICH7.
D-type flip-flop ICJ9 is a latch circuit for the slave signals and its output is supplied to pin 19 (pin PRI) of ICH7. When, for instance, an interrupt request for an interrupt other than INT P7 is issued, the INT signal output from pin 17/ICJ5 is latched by both the ASTB signal output from pin 25/ICH14 and the INTAK signal output from pin 24, and a high level is supplied to pin PRI/ICH7. As a result, ICH7 recognizes that the INTAK signal from the CPU has been output to another device. With an interrupt based on INT P7, ICJ5 "SA0, SA1 and SA2" decoded by ICJ8 and ICG8 serve to reset latch ICJ9. Consequently, pin 29 (pin PRI) /ICH7 is set low, ICH7 generates the interrupt vector and the CPU processes the data which correspond to the vector.

Priority	ICJ5	Interrupt request signal
1	INT P7	ICH7 RS-422 transmission/reception
2	INT P0	(Not used)
3	INT P1	REF V detection
4	INT P2	TIMER-0/ICH8 (V timing generation)
5	INT P3	(Not used)
6	INT P4	TIMER-2/ICH8 (RS-422 10 msec detection)
7	INT P5	ICH6 reception
8	INT P6	ICH6 transmission

Table 4-7-3. ICJ5 Interrupt Request Signals (SY-103)

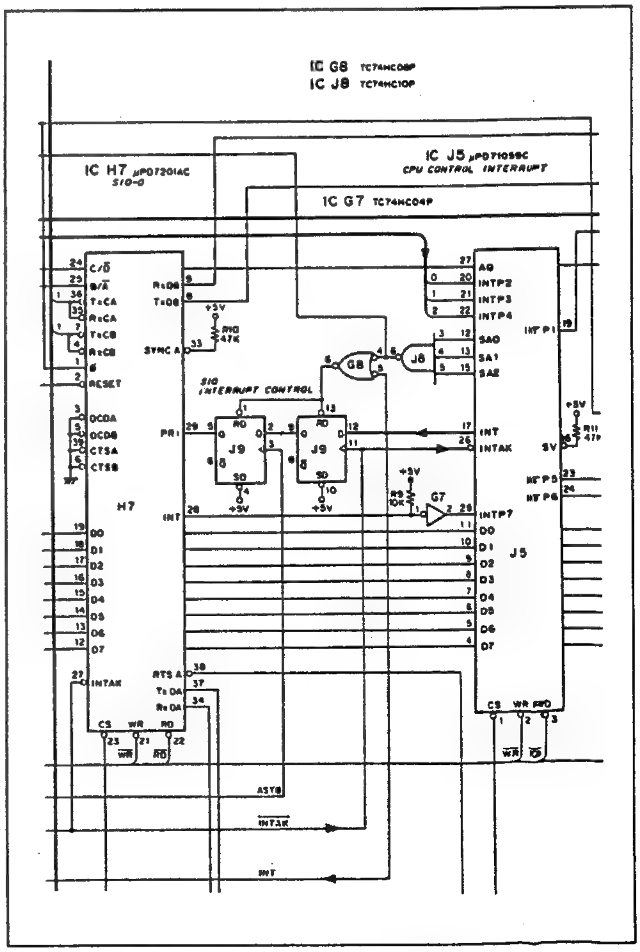


Fig. 4-7-6. Interrupt Controller (SY-103)

The various ICH7 and ICJ5 timing operations shown in Fig. 4-7-7 are now described.

(a) The interrupt request generated by ICH7 is transferred to pin INT P7 of ICJ5 and ICJ5 generates the interrupt request and advises the CPU that the interrupt request is present.
(b) The first $\overline{\text{INTAK}}$ signal is sent to ICJ5 from pin 24 of CPU ICH14. Depending on this signal, ICJ5 judges whether it is to serve as master or slave, and if it is to serve as the slave, the processing that follows is transferred to ICH7.
(c) Since pin 29 (pin PRI) of ICH7 is set high by ICJ9, ICH7 judges that the interrupt request is for another device and it does not generate the interrupt vector.
(d) Since pin 29 (pin PRI) of ICH7 is set low by ICJ9, ICH7 judges that an interrupt with a higher priority than itself is not being requested, and it undertakes the processing of its own interrupt.
(e) The signal produced by AND gate processing the ICJ5 SA0, SA1 and SA2 outputs is supplied to waiting control circuit ICG12 and since the CPU is made to wait for a period equivalent to 1 clock cycle, the TW state is generated once.

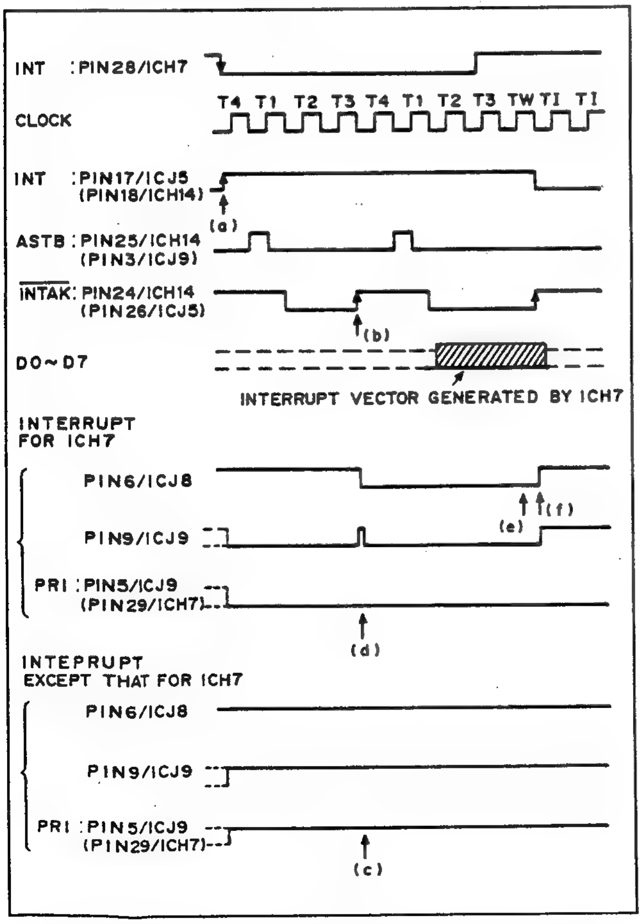


Fig. 4-7-7. Master/Slave Timing Chart (SY-103)

(f) When ICH7 receives the second $\overline{\text{INTAK}}$ signal output from the CPU, it generates the interrupt vector. The CPU executes the transmission/reception processing program in accordance with the contents of the interrupt vector.

(5) REMOTE-1/2A/2B selector (SY-103 board)

ICH7 is used for REMOTE-1/2A/2B connector communication based on RS-422 as well as for data communication between the system control system and the control panel. Channel B is allocated to the control panel and used with a baud rate of 38.4 kbps. ICJ1 is a buffer for communication with the control panel. Channel A is used for the REMOTE-1/2A/2B connectors and it conducts interfacing with external equipments.
REMOTE-1/2A/2B selector ICF6 and ICG6 are selected by the nature of the software using the select signal and priority signal from the CPU, select the signal required from among the REMOTE-1/2A/2B connectors in accordance with the menu instruction, and supply this to ICH7 RXDA/TXDA.
A 0.6144 MHz frequency signal is supplied as the transmission/reception clock signal for channel A of ICH7, and a baud rate of 38.4 kbps is obtained by dividing it down to 1/16 as per the nature of the software using ICH7. When the RS-232C interface kit BKH-3002 (SE-56 board) is employed, the preset data are changed and an RS-232C baud rate is provided so that the transmission/reception clock signal is divided down to 1/32 (19.2 kpbs) or to 1/64 (9.6 kbps) by the CPU.
ICG6 is the REMOTE-1/2A/2B output selector and REMOTE-2A/2B priority signal input selector. REMOTE-1 is fixed as the slave. ICF6 is the REMOTE-1/2A/2B input selector and it selects the input signal based on the select signal from the CPU and the input signal from the master/slave information.

The gate of ICF5 pins 1 and 2 is the master/slave detector circuit. When the CONTROL P or CONTROL R buttons are pressed on the control panel, the high-level master request signal is supplied from the CPU to pin 1 of ICF5. At this time, the PRIORITY 2A or PRIORITY 2B signal has been supplied to pin 2 of ICF5, and pin 3 of ICF5 is turned to high or low by this signal. The CPU detects whether its machine is the master or slave by the state of the inverter ICG7 pin 8 output. When other machine is already being used as the master, it abandons the process of serving as the master, and "LINE ERR" appears on the display of the function control panel.

Tri-state control gate ICG4 and ICF4 set only the output buffer which is being used to the enable status and the other output buffers are placed in the high-impedance state. The buffers for the CCJ RX input pin and CCJ TX output pin are housed on the SE-49 board.

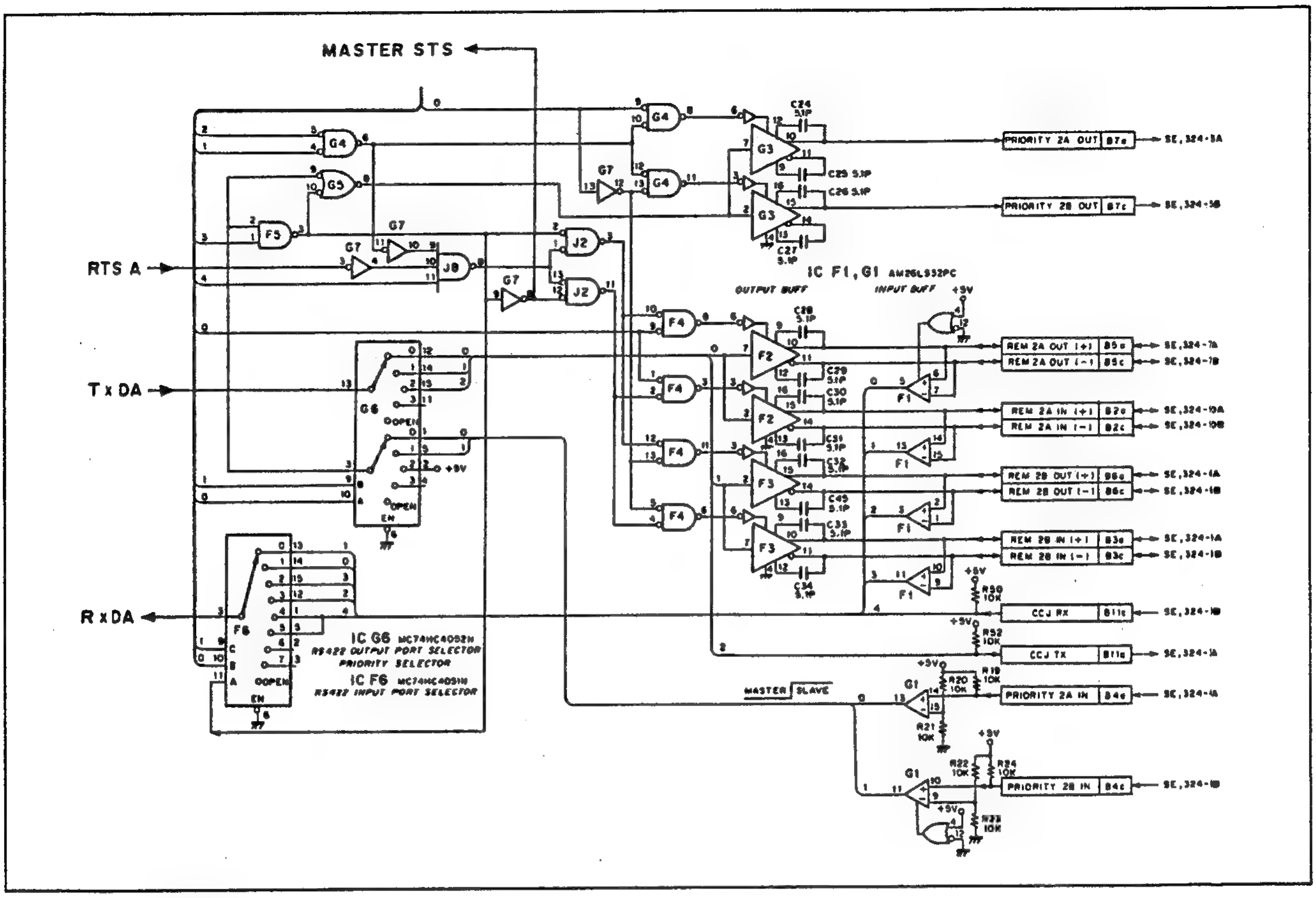


Fig. 4-7-8. REMOTE-1/2A/2B Selector (SY-103)

(6) Programmable timer/counter (SY-103 board)

Programmable timer/counter ICH8 contains three counters, two of which are used in this machine to generate the timing signals in the REF V period and to detect the RS-422 time-out relating to REMOTE-2A and REMOTE-2B. A signal with a 2.4576 MHz frequency is used as the ICH8 reference clock signal and timer detection is possible from 0 to 26.67 msec.

Counter 0 : Generation of timing signals in REF V period
Main processing in V period in REF V+3 msec
· Processing of communication with control panel in REF V+11 msec

Counter 1 : Not used

Counter 2 : REMOTE-2A/2B 10 msec time-out detection

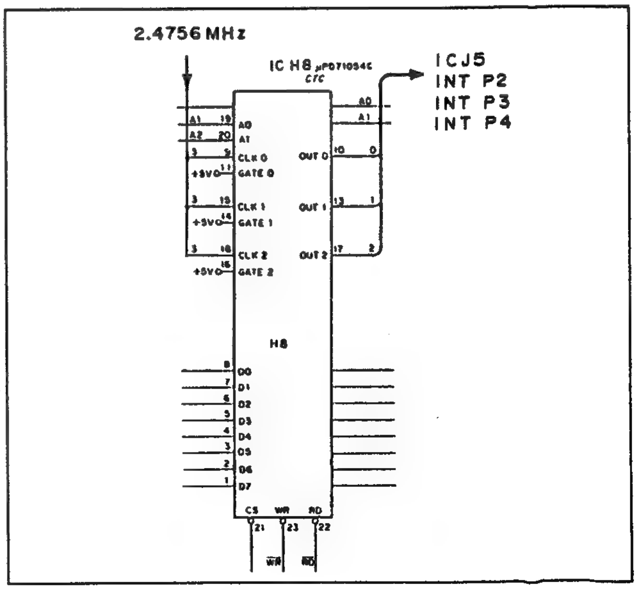


Fig. 4-7-9. Programmable Timer/Counter (SY-103)

(7) Serial control unit (SY-103 board)

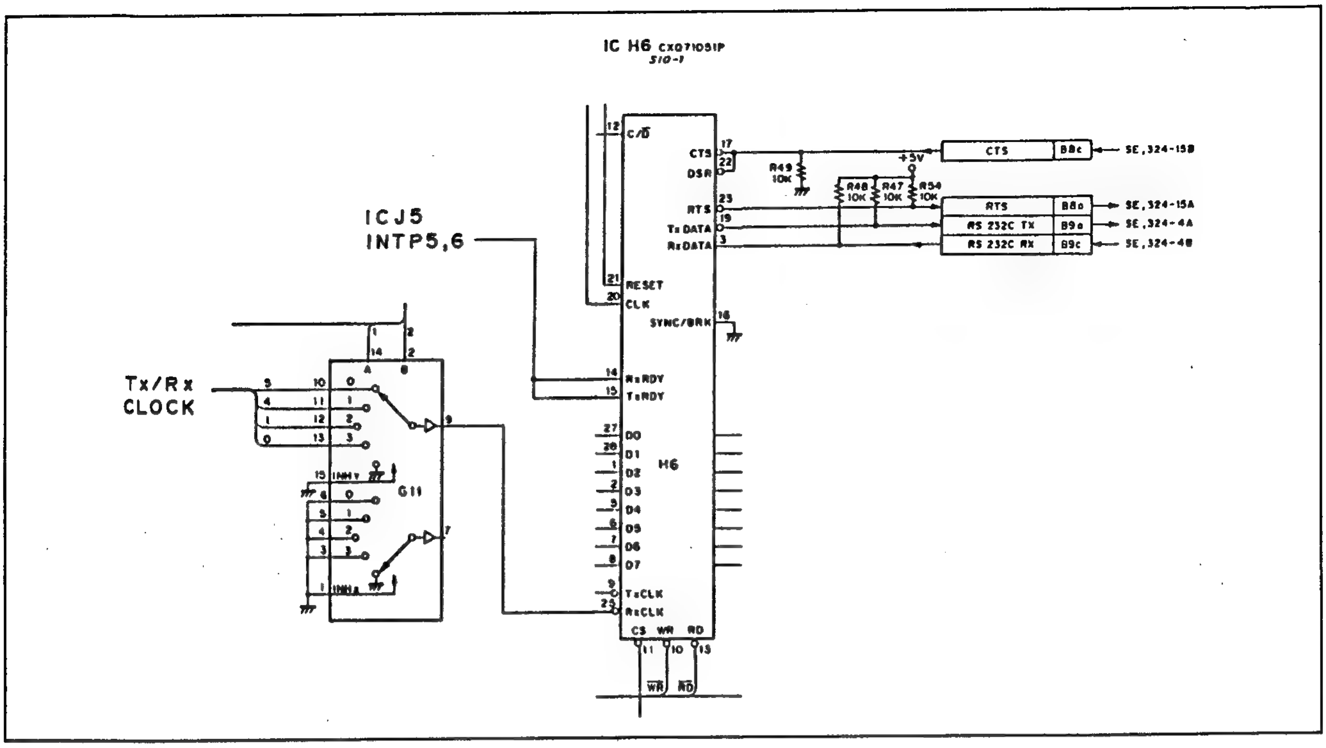


Fig. 4-7-10. Serial Control Unit (SY-103)

Serial control unit ICH6 is provided in order to establish an RS-232C interface between the VTR and a personal computer or other such unit.
There are 4 kinds of communication clock signals : 614.4 kHz, 307.2 kHz, 153.6 kHz and 76.8 kHz. These signals are selected by ICG11. It is possible to assign a baud rate ranging from 38.4 kbps to 1.2 kbps.
Pins RxRDY and TxRDY of ICH6 are connected to pins INT P5 and INT P6 of ICJ5 and this enables the CPU to process the transmission/reception interrupts efficiently.
The CTS (clear to send) signal is supplied to the B8c pin on the SY-103 board and the RTS (request to send) signal is output from pin B8a. These signals can be used as the control line when transmitting or receiving.

(8) I/O port expander (SY-103 board)

ICF13 (CXD1095Q) is an input/output device for enabling the CPU to make full use of the external/internal information.
ICF13 has four 8-bit I/O ports and one 4-bit I/O port, making a total of 36 bits for the I/O ports. On the SY-103 board, the 16 bits of "PA0−PA7" and "PB0−PB7" are used as the input ports and the 20 bits of "PC0−PC7," "PD0−PD7" and "PX0−PX3" are used as the output ports.

PORT	7	6	5	4	3	2	1	0
PA (input)	NO USE	NO USE	NO USE	NO USE	NO USE	NO USE	NO USE	NO USE
PB (input)	TEST SW	RS-232C SENSE	NO USE	NO USE	REF 2	NO USE	NO USE	MASTER STATUS
PC (output)	REM 3 SEL	REM 1 SEL	REM 2 A/B SEL	RS-232C SEL	NO USE	NO USE	μ PD71051 BAUD RATE	
PD (output)	BANK ROM SELECT		NO USE	NO USE	NO USE	NO USE	RS-422 TX ENABLE	MASTER REQUEST
PX (output)	NO HARD	NO HARD	NO HARD	NO HARD	NO USE	NO USE	NO USE	CPU READY

Table 4-7-4. I/O Port Expander Bit Allocation (SY-103)

The bits are defined as follows.

PB7 : TEST SW
Status of TEST switch S2 (SY-103 board)

PB6 : RS-232C SENSE
RS-232C select signal from BKH-3002 (RS-232C interface : SE-56 board)

PB3 : REF2
REF2 information (low=field 1 ; high=field 2)

PB0 : MASTER STATUS
Status signal for advising whether the device connected to the 9-pin connector (RS-422) has output the master signal

PC7, 6 : REM 3 SEL, REM 1 SEL
REMOTE-1/2/3 select signal

PC7	PC6	SELECTION
0	0	REMOTE-2
0	1	REMOTE-1
1	0	REMOTE-3
1	1	UNDEFINED

UNDEFINED : Not output by software

PC5 : REM 2 A/B SEL
REMOTE-2A/2B select signal
(high=REM-2A ; low=REM-2B)
Valid when PC7 and PC6 bits are both low.

PC1, 0 : BAUD RATE
ICH6 baud rate assignment

PC1	PC0	DIVISION	BAUD RATE
0	0	1/64	2.4 kbps
0	0	1/16	9.6 kbps*
0	1	1/64	1.2 kbps
0	1	1/16	4.8 kbps*
1	0	1/64	9.6 kbps
1	0	1/16	38.4 kbps
1	1	1/64	4.8 kbps
1	1	1/16	19.2 kbps

*Not used by software.

PD7, 6 : BANK ROM SELECT
ICH11 bank ROM select signal (1 bank=16k bytes)

PD7	PD6	BANK ROM
0	0	BANK 0
0	1	BANK 1
1	0	BANK 2
1	1	BANK 3

PD1 : RS-422 TX ENABLE
This bit enables REMOTE-2A/2B (RS-422) data transmission. When it is disabled, all the REMOTE-2A/2B transmission lines are placed in the high-impedance state.

PD0 : MASTER REQUEST
This bit is set on by the CPU when its own machine serves as the master. When the controller is connected to the 9-pin RS-422 side and the priority is set to master, the PB 0 bit (master status) is not set on and the CPU is no longer set to serve as the master. In other words, by setting this bit on, the CPU detects the status of the 9-pin connector (high=MASTER ; low=SLAVE).

PX0 : CPU READY
This is the control bit for the LED which displays CPU READY. When it is set on by the CPU, the READY LED lights. When this bit is not accessed for over 106.7 msec, the READY LED goes off.

4-7-2. Time Code Circuit (SY-103 Board)

In the BVH-3000/3100, the time code signals are written and read out directly by the CPU. All the time code system control is exercised by the CPU on the SV-90 board, and the CPU on the SY-103 board gets the necessary data through the common memory (RAM) ICJ3.

(1) Address decoder (SY-103 board)

A total of 256 bytes for addresses "AB00H–ABFFH" are allocated as the time code addresses by the "~TC CS" signal which is supplied from the SV-90 board. The addresses are decoded by ICA13, B13 and C13 on the SY-103 board, and the read and write signals are sent to the various ICs.

ADDRESS	MODE	DEVICE	FUNCTION
AB00H–AB0FH	WRITE	ICE3	I/O PORT EXPANDER
AB10H–AB17H	WRITE	ICC10	TC GENERATOR (LTC)
AB18H–AB1FH	WRITE	ICC10	UB GENERATOR (LTC)
AB20H–AB27H	WRITE	ICE8	TIMER 1
AB28H–AB2FH	WRITE	ICE8	TIMER 2
AB30H–AB3FH	WRITE	ICC10	TCG CONTROL REGISTER
AB40H–AB4FH	WRITE	ICA4	CHARACTER GEN CONTROL
AB00H–AB0FH	READ	ICE3	I/O PORT EXPANDER
AB10H–AB17H	READ	ICC10	TC GENERATOR
AB18H–AB1FH	READ	ICC10	UB GENERATOR
AB20H–AB27H	READ	ICC6	TC READER (LTC)
AB28H–AB2FH	READ	ICC6	UB READER (LTC)
AB30H–AB37H	READ	ICC3	TC READER (VITC)
AB38H–AB3FH	READ	ICC3	UB READER (VITC)

Table 4-7-5. Time Code Address Map (SY-103)

The bit allocation of the I/O port expander ICE3 (CXD1095Q) is described next.
ICE3 has four 8-bit I/O ports and one 4-bit I/O port, making a total of 36 bits for the I/O ports. ICE3 "PA0–PA7," "PB0–PB7" and "PC0–PC7" are used as the output ports, and "PD0–PD7" and "PX0–PX3" are used as the input ports.

PA7 : CHARACTER ENABLE
This enables the TC data of the monitor system to be displayed.

PA6 : VITC ENABLE
This enables VITC to be inserted into the video signal.

PA5 : LTC ENABLE
This inserts the LTC generator signal into audio channel 3.

PA4 : REMOTE-3 TIMER OUT
This activates the timer gate pulse for outputting the TIMER-1/TIMER-2 data to the REMOTE-3 connector.

PA3 : LTC ERROR BYPASS
This sets the error bypass function of the time code reader to ON.

PA0 : CHARACTER RECORD ENABLE
This enables the character display data to be recorded on the tape when REC/EDIT is conducted.

PB6 : VITC FIELD POSITION SELECT
This selects the VITC field position.

PORT	7	6	5	4	3	2	1	0
PA (output)	CHARACTER ENABLE	VITC ENABLE	LTC ENABLE	REMOTE-3 TIMER OUT	LTC ERROR BYPASS	NO USE	NO USE	CHARACTER REC EN
PB (output)	NO USE	VITC FIELD POSITION SELECT	VITC TIME CODE FORMAT SELECT		NO USE	NO USE	LTC TIME CODE FORMAT SELECT	
PC (output)	CHARACTER SYNC SELECT		NO USE	NO USE	NO USE	NO USE	NO USE	CHARACTER IC STROBE
PD (input)	NO USE	VITC ASSIGN 3 BIT (SMPTE)	VITC ASSIGN 6 BIT (EBU)	VITC FIELD DATA	NO USE	LTC BI–PHASE ERROR	VITC READ ERROR	LTC READ ERROR
PX (input)	NO HARD	NO HARD	NO HARD	NO HARD	CFSD–CFSA			

Table 4-7-6. I/O Expander Bit Map (SY-103)

PB5, 4 : VITC TIME CODE FORMAT SELECT
These select the VITC signal format.

PB5	PB4	FORMAT
0	0	PAL, SECAM
0	1	(PAL-M)
1	0	NTSC/PAL-M NDF
1	1	NTSC/PAL-M DF

PB1, 0 : LTC TIME CODE FORMAT SELECT
These select the LTC signal format.

PB1	PB0	FORMAT
0	0	PAL, SECAM
0	1	(PAL-M)
1	0	NTSC/PAL-M NDF
1	1	NTSC/PAL-M DF

PC7, 6 : CHARACTER SYNC SELECT
These select the composite sync signal supplied to character generator ICA4 in accordance with the monitor select or recording mode status.

PC7	PC6	COMPOSITE SYNC SIGNAL
0	0	CHARACTER SYNC
0	1	TBC SYNC
1	0	REF SYNC
1	1	NO SYNC

PC0 : CHARACTER IC STROBE PULSE
The strobe pulse is for transferring data to the register inside character generator ICA4, and it is generated because of the nature of the software by the CPU on the SV-90 board.

PD6 : VITC ASSIGN 3 BIT
This signal indicates the status of VITC ASSIGN 3 BIT (No.35). With the SMPTE time code, it is assigned to the VITC MARK.

PD5 : VITC ASSIGN 6 BIT
This signal indicates the status of VITC ASSIGN 6 BIT (No.75). With the EBU time code, it is assigned to the VITC MARK.

PD4 : VITC FIELD DATA
This denotes the status of the VITC field data specified by the SMPTE or EBU time code.

PD2 : LTC BI-PHASE ERROR
The bi-phase error is detected when the regularity in the BI-PHASE MARK modulation of the LTC playback signal is lost and the data will not be played back properly, and this bit is set on.

PD1 : VITC READ ERROR
This bit is set on when the VITC signal is not played back properly or when a tape with no VITC signal recorded at all has been played back.

PD0 : LTC READ ERROR
This bit is set on when the demodulated time data do not match the regularity of the advance.

PX3－0 : CFSD－CFSA
These indicate the demodulated color frame information from the playback VITC signal. Field 1 and field 2 are identified by the VITC FIELD MARK information.

CFSD	CFSC	CFSB	CFSA	FIELD INFORMATION	
				NTSC	PS
1	1	1	1	F1 & F2	F1 & F2
1	1	0	0	F3 & F4	F3 & F4
0	0	1	1	F1 & F2	F5 & F6
0	0	0	0	F3 & F4	F7 & F8

(2) Clock generator (SY-103 board)

The reference clock signal for the time code reader/generator and the system clock signal for outputting the time data to the REMOTE-3 connector are generated by crystal oscillators X3 (14.31818 MHz for SMPTE) and X2 (14.5 MHz for EBU). I/O port expander ICE5 is accessed and SMPTE/EBU is selected by the CPU on the SV-90 board.

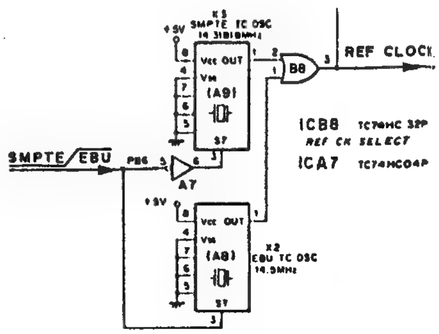


Fig. 4-7-11. Clock Generator (SY-103)

(3) **Time code generator (SY-103 board)**

REGISTER	7	6	5	4	3	2	1	0
SWC	NO USE	NO USE (SLAVE LOCK)	NO USE (DATA LOAD)	TCG HOLD/RUN	NO USE (RESET)	NO USE	NO USE (TICT)	NO USE (TIUB)
SWM	CF CTL OFF/ON	FIELD-1 IN	ASSIGN-6 BIT	ASSIGN-5 BIT	ASSIGN-4 BIT	ASSIGN-3 BIT	ASSIGN-2 BIT (CF)	ASSIGN-1 BIT (DF)
SWS	NO USE	TIME CODE FORMAT			PHASE CORRECTION ON/OFF	VITC FIELD MARK POSITION SELECT		
SWV	VITC POSITION 2				VITC POSITION 1			

Table 4-7-7. TCG Control Signals (SY-103)

Time code generator ICC10 is characterized by free-running operation based on the reference clock input. In order to synchronize the time code signal with the video signal, the REF SYNC signal is supplied to the CS IN pin (pin 27) and ICC10 uses the REF SYNC and reference clock to generate the VITC and LTC time code data.
ICE10, E11, E12 and E13 convert the parallel data from the CPU into serial data. The control signal is read into the register inside ICC10 by the SCK0 clock signal which is output from pin 4 of ICC10.

SWC4 : TCG HOLD/RUN control
This controls the HOLD/RUN status of the time code generator.

SWM7 : CF CTL ON/OFF
When this bit is set on, the time code signal which is generated is locked to the SWM6 color frame information.

SWM6 : FIELD-1 IN
This is the color frame information ; it is set high in field 1.

SWM5−0 : ASSIGN-6−ASSIGN-1
These assign bits are for setting the time code signal on or off. SWM5, 4, 3 and 2 are null bits.
SWM1 : Color frame bit
SWM0 : Drop frame bit

SWS6−4 : TIME CODE FORMAT
These bits are for selecting the time code format select signals.

SWS6 (S4)	SWS5 (S2)	SWS4 (S1)	FORMAT
1	1	1	NTSC/PAL-M DF
1	1	0	NTSC/PAL-M NDF
1	0	1	(PAL-M)
1	0	0	PAL/SECAM
0	0	0	FILM

SWS3 : PHASE CORRECTION ON/OFF
This controls the PHASE correction bit for parity checks.

SWS2−0 : VITC FIELD MARK POSITION SELECT
These bits select the VITC field mark position.
SMPTE time code : bit 27 (corresponds to ASSIGN3)
EBU time code : bit 59 (corresponds to ASSIGN6)

SWV7−4, SWV3−0 : VITC POSITION-2, 1
These bits select the insertion lines for the VITC signal.
NTSC : Lines 10−25 (standard setting : lines 12 and 14)
PAL/SECAM : Lines 7 (320) −22 (335) (standard setting : lines 19 and 21)

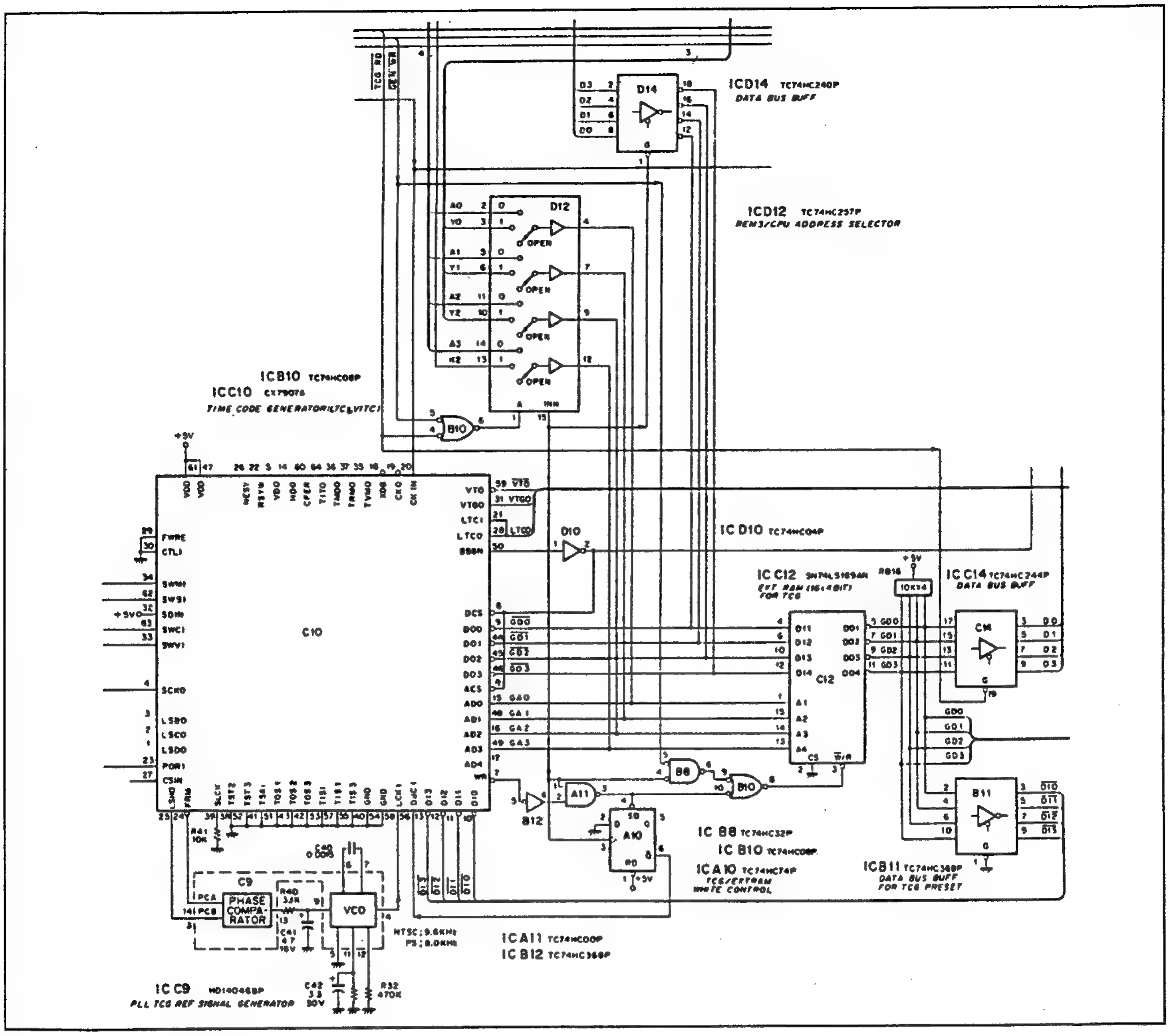


Fig. 4-7-12. Time Code Generator (SY-103)

The time code generator circuit is now described. The basic LTC clock signal is generated by ICC10 and ICC9. The SMPTE LTC clock signal has a frequency of 9.6 kHz (80 bits×30 Hz×4) while the EBU LTC clock signal has a frequency of 8 kHz (80 bits×25 Hz×4). ICC10 generates the 30Hz/25Hz SYNC WORD signal and outputs it from the LSHO pin (pin 25). ICC10 decodes the REF SYNC signal supplied externally and converts it into the frame signal which it then outputs from the FRM pin (pin 24). ICC9 compares the phases of these two signals, drives the VCO with its output and generates the reference clock signal (9.6 kHz for SMPTE ; 8 kHz for EBU) which is synchronized with the video signal. The data arriving from the CPU are preset as follows into time code generator ICC10. All the data are input into, and output from, ICC10 via memory (RAM) ICC12. ICC10 operates in synchronization with the video input signal in frame units and data are input or output once per frame.

CPU ICH14 reads the data while avoiding the input/output timing (FRAME TOP+approx. 29.5 msec) of time code generator ICC10 and when preset data are present, it writes them into ICC12. The data are read at a timing of "V+approx. 1.5 msec" while they are written at a timing of "V+approx. 8.5 msec." ICC10 reads the memory data from ICC12 once per frame and accepts them into its own register. The accepted data are immediately written again into memory ICC12.

When the data from the CPU are written into memory ICC12, time code generator ICC10 accepts the data immediately from ICC12 and sets them into the register inside ICC10. When the data from the CPU have not been set in ICC12, ICC10 repeats the read/write operation of the data applying to the previous frame. Fig. 4-7-14 is the read/write timing chart of external memory ICC12 based on ICC10.

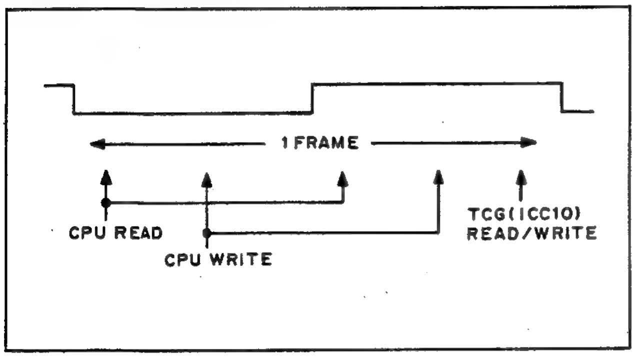


Fig. 4-7-13. TCG CPU Read/Write Timing (SY-103)

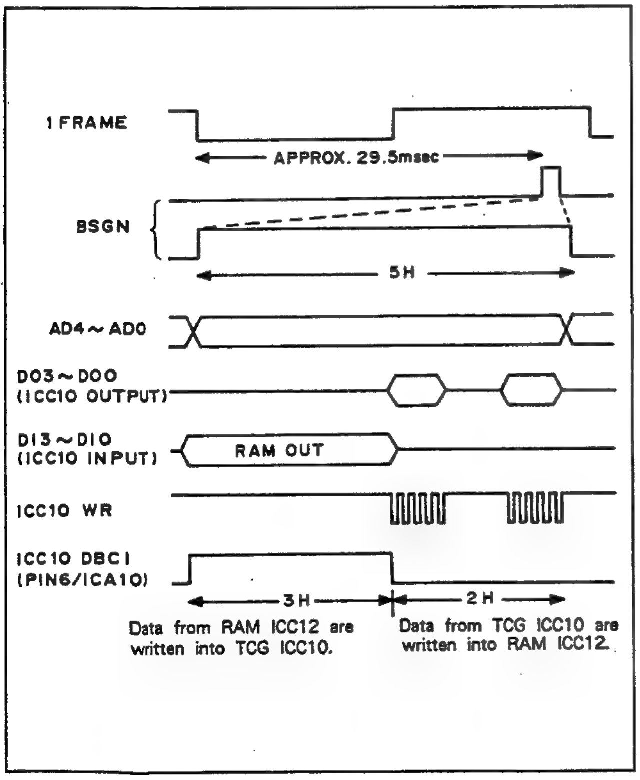


Fig. 4-7-14. External Memory Read/Write Timing (SY-103)

The data interfacing of above-mentioned time code generator ICC10 can be summarized as follows.

- CPU ICH14 reads out the TCG data which are stored in memory (RAM) ICC12 at the "V+1.5 msec" timing.
- CPU ICH14 writes the TCG data into ICC12 at the "V+8.6 msec" timing.
- Time code generator ICC10 reads out the TCG data from memory ICC12 within the time corresponding to 3H from the "frame+29.5 msec" timing, it sets them into its own register and then writes the TCG data into ICC12 in the following 2H.
- Time code generator ICC10 outputs the necessary data to REMOTE-3 immediately after it has output the data to memory ICC12.

(4) LTC reader (SY-103 board)

LTC reader ICC6 (CX7912A) contains most of the circuitry required to read the LTC signal. It operates in synchronization with the time code pulse played back from the tape, and CPU ICH14 is synchronized with the REF V signal. As a result, the ICC6 output is temporarily stored in memory (RAM) ICD7, and the CPU reads out the stored data at the timing which is synchronized with the REF V signal.

The series of operations starting with tape playback and ending with readout by the CPU are processed in the following way.

- LTC reader ICC6 transfers the data which it has read out from itself to memory ICD7 once per field, and it does this at the timing of the fall edge of the V pulse (REF V) which is input to pin 13 of D-type flip-flop ICA10.
- It outputs the time code data to the REMOTE-3 connector at the timing of the rise edge of the memory WR signal which is input to pin 3 of memory ICD7.
- It sets the $\overline{\text{TC BUSY}}$ signal of the CPU to the enable status at the timing of the completing edge (rise edge) of the signal output to the REMOTE-3 connector. The CPU then accesses the memory at a certain timing from the REF V signal, it checks that the TC ERR/BUSY signal is off and it transfers the data to its own memory. When the TC ERR/BUSY signal is on, the data are held or updated by software.

(a) The signal (ICA10 pin 9) indicating whether the time code data have been transferred once per field is reset by the REF V signal.

(b) ICC6 outputs the BSRL signal (pin 50) for outputting the LTC data. The BSRL signal is supplied through ICC2, A12 and B12 to pin 6 of ICC14 to serve as the $\overline{\text{TC BUSY}}$ signal for the CPU. The $\overline{\text{TC BUSY}}$ signal is sent through the data bus to the CPU and the CPU is advised that the LTC data are being read out.

(c) The data output from LTC reader ICC6 are stored by the memory $\overline{\text{W}}$/R signal in memory ICD7. Pin 8 of ICB12 is set high and REMOTE-3 TC gate ICB5 is triggered.

(d) The REMOTE-3 TC OUTPUT STS signal (pin 9 of ICB5) is set high and supplied to pin 11 of ICA10, and the signal (pin 9 of ICA10) indicating that the data have been transferred once per field is set high. As a result, data writing into the memory is prohibited and the data are not written until the next field even if the memory WR signal is output from LTC reader ICC6.

(e) The $\overline{\text{TC BUSY}}$ signal is low and so the CPU does not read out the LTC data.

(f) The $\overline{\text{TC BUSY}}$ signal is high and so the CPU reads out the LTC data.

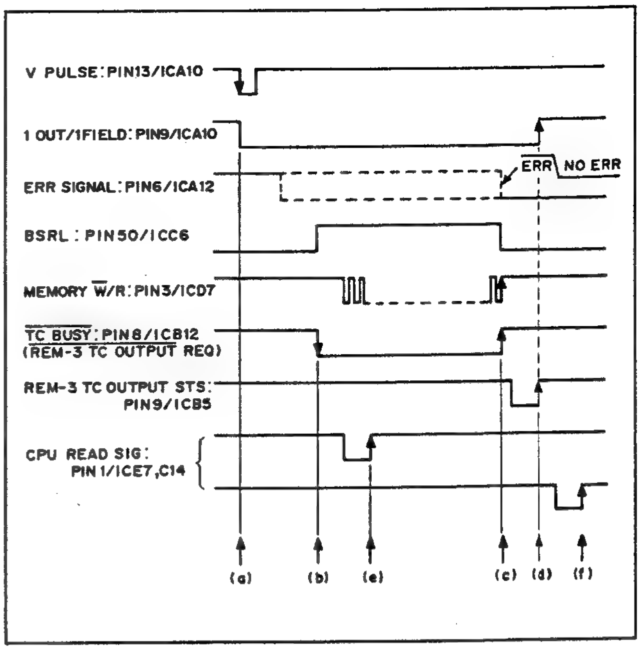


Fig. 4-7-16. LTC Reader Timing Chart (SY-103)

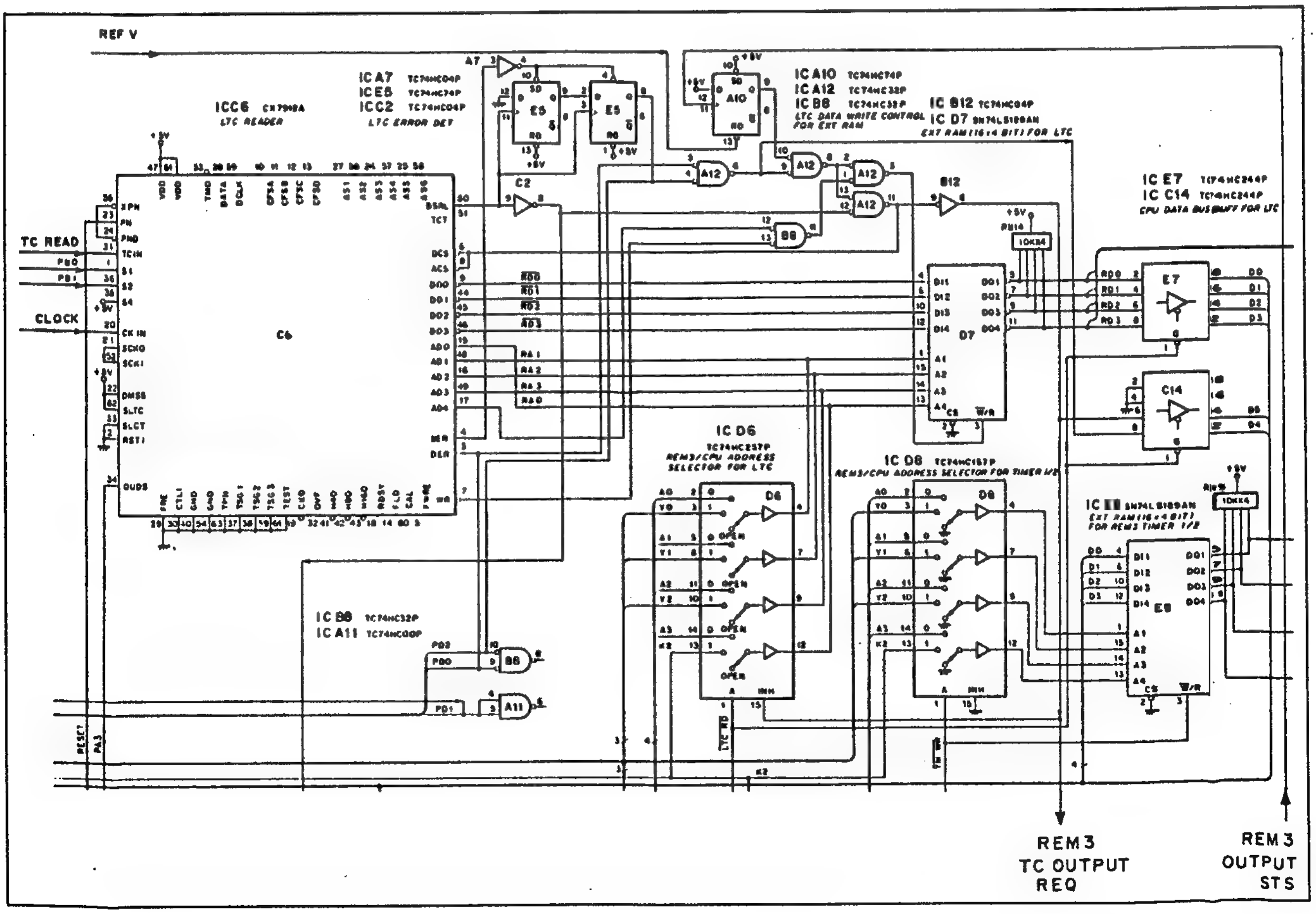


Fig. 4-7-15. LTC Reader (SY-103)

D-type flip-flop ICE5 is the circuit that detects the LTC BI-PHASE bit error. ICE5 latches the BER signal which is output from ICC5 and prevents the error data from being transferred to memory (RAM) ICD7. There is a reason for this : the BER signal, which indicates that the regularity of the BI-PHASE MARK modulation has been lost, is output but this signal is cleared immediately when the regularity is properly restored and the CPU cannot detect the bit errors. D-type flip-flop ICA10 generates the control signal for transferring the LTC data once per field to ICD7. The V pulse (REF V) is input to pin 13 of ICA10. Pin 9 of ICA10 is set low for that period from the timing of the V pulse fall edge until the completion of the data output to the REMOTE-3 connector, and the LTC data from ICC6 are transferred to memory ICD7. When the data output to the REMOTE-3 connector is completed, Pin 9 of ICA10 is set high to prohibit the transfer of data to the memory.
The system clock signal of LTC reader ICC6 is supplied from VITC reader ICC3 (CX7913A). It is produced by dividing down the system clock signal of the VITC reader to 1/3.

SYSTEM	VITC CLOCK	LTC CLOCK	LTC DYNAMIC RANGE
SMPTE	14.31818MHz	4.7723MHz	1/34 TO 107 TIMES
EBU	14.5MHz	4.8333MHz	1/26 TO 130 TIMES

The CPU on the SV-90 board is responsible for the LTC signal interpolation. When the error bit or BUSY bit is on once the LTC signal has been read, the CPU replaces the display with the LTC interpolation data created from the CTL signal and REEL FG signal. The LTC interpolation data are always provided even when there are no errors, and even immediately after the power has been switched on, it is possible to display precise interpolation data when the data are read out correctly.

(5) VITC reader (SY-103 board)

VITC reader ICC3 (CX7913A) contains most of the circuits required to read out the VITC signal. In the NTSC model (SMPTE), a system clock with a frequency of 14.31818 MHz is supplied to ICC3 ; in the PAL/SECAM model (EBU), it has a frequency of 14.5 MHz. The VITC signal is demodulated inside ICC3 based on the system clock signal, composite sync signal and playback VITC signal. ICA2 creates the composite sync signal. ICA2 gates the playback sync signal supplied from the VO-16 board using dropout information and outputs the sync signal only when it is played back normally from the tape. The playback VITC signal is directly input into ICC3 from the VO-16 board.

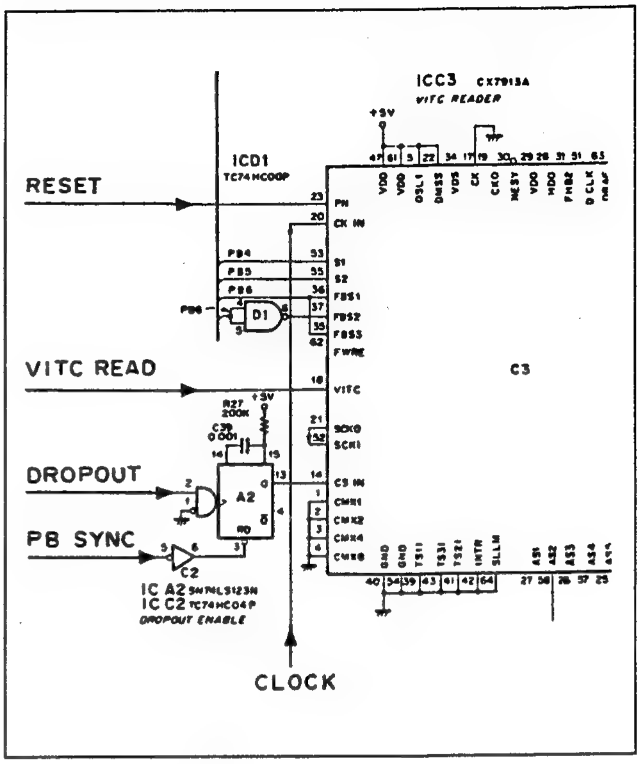


Fig. 4-7-17. VITC Reader Input Circuit (SY-103)

The VITC data provided from the playback signal are read out by ICC3 and immediately transferred to memory (RAM) ICD5. While ICC3 is outputting the VITC data, the BSRV signal (pin 50) is set high, the ICD4 output is prohibited, ICC3 controls the DO0−DO3, AD0−AD3 and WR signals, and the VITC data are written into memory ICD5. The timing at which the data are written is regulated as follows by the position of the VITC data.

SMPTE : V+0.636 ms−V+1.589 ms
(line 10−line 25)
EBU : V+0.448 ms−V+1.408 ms
(line 7−line 22)

Avoiding of the time during which the data are written, the CPU reads out the VITC data from memory ICD5 and it uses these data for the timer display and superimposition characters. "V+approx. 1.8 ms" represents the timing at which the CPU reads out the VITC data from memory ICD5. Memory ICD5 is constantly scanned by the system clock signal and the stored VITC data are output to the REMOTE-3 connector. However, VITC data output gate ICD4 is set on only once per field by the BSRV signal which is output from pin 51 of ICC3.

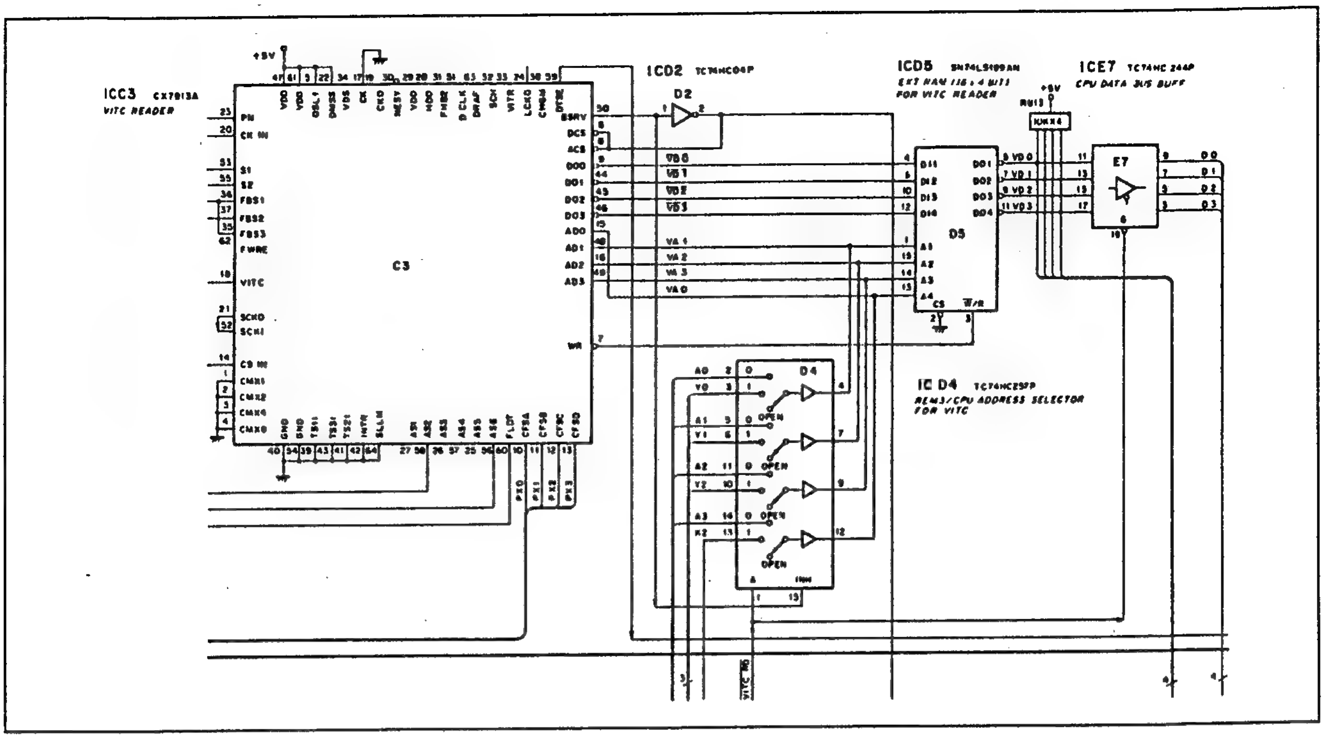


Fig. 4-7-18. VITC Reader Output Circuit (SY-103)

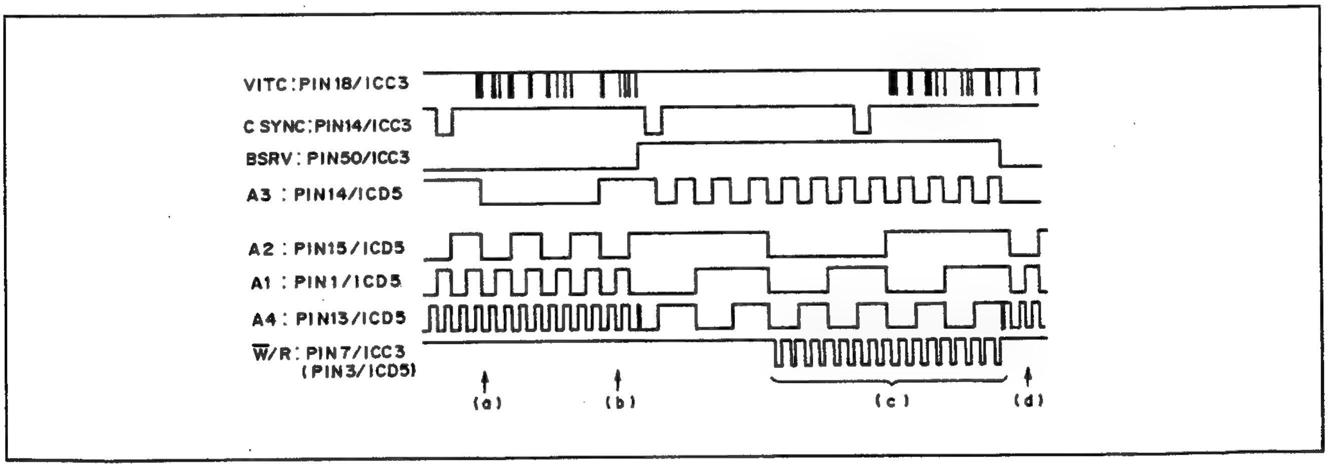


Fig. 4-7-19. VITC Write Timing (SY-103)

(a) The playback VITC signal is supplied to ICC3. The system clock signal is supplied to address pins A3, A2, A1 and A4 of ICD5 via ICD4.

(b) The BSRV signal is set high so that ICC3 will output the data.
The address output of ICC3 is supplied to the address pin of ICD5. The ICD4/system clock system is placed in the high-impedance state.

(c) The VITC data read out by ICC3 are transferred to memory ICD5.

(d) The ICC3 data output is completed.
The gate signal is output to the REMOTE-3 connector from the timing of the BSRV signal fall edge.

The error detector circuit is contained inside ICC3, and the detected error information is sent to the CPU from the DTSE pin (pin 59) via ICE3. ICC3 is also provided with output pins (DFSA–DFSD) for the color frame signal, and the CPU uses ICE3 to read in the color frame signal. The CPU infers the color field numbers in accordance with the NTSC or PAL/SECAM signal from the field mark bit of the VITC signal and this color field signal, and it inserts the number into the time code display.

(6) Timer memory circuit (SY-103 board)

The SY-103 board does not have a circuit which detects the timer data. The timer data are provided by the CPU on the SV-90 board from the CTL signal and REEL FG information through processing which accords with the software. In order for the TIMER-1 and TIMER-2 signals to be output to the REMOTE-3 connector, memory (RAM) ICE8 is provided on the SY-103 board.
Address selector ICD8 selects the address bus side only when the CPU writes the data into memory ICE8, and at all other times it selects the system clock side. The CPU writes the timer data into memory ICE8 once per field at the timing of "V+approx. 13.5 ms." Upon completion of the writing, the trigger (PA4) signal is output by the CPU from pin 60 of ICE3 in order to make REMOTE-3 connector gate circuit ICB6 active.

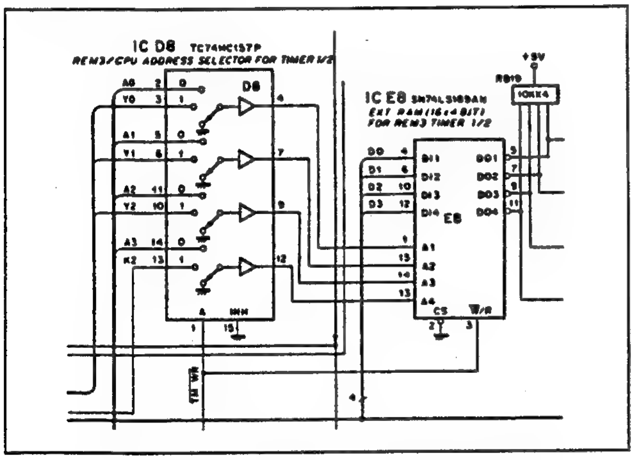


Fig. 4-7-20. Timer Memory Circuit (SY-103)

(7) Time data read/write timing (SY-103 board)

Following the description of the time data circuitry in sections (3) through (6), the following figure shows the read/write timings with respect to the various ICs as seen from the CPU.
The timing of all the time data except the LTC data is controlled by the software so that there will be no conflict due to any restrictions arising from the hardware configuration. It is possible to provide information as to whether even the LTC data have conflicted, and whether the data are to be retained or interpolated is controlled by the software.
When the tape speed is increased, the timing at which the LTC data are written into ICC6 becomes unstable, the data conflict with the read data in the first half of the field and it is no longer possible to write the data stably. The data are therefore read in the second half of the field to prevent conflict.

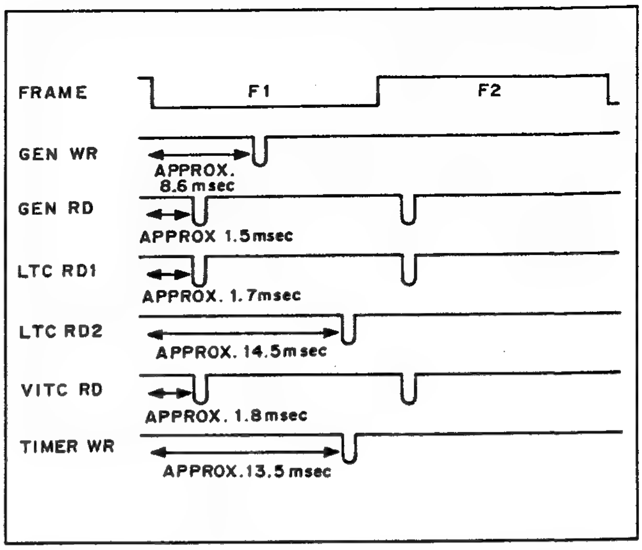


Fig. 4-7-21. Time Data Read/Write Timing (SY-103)

(8) Character generator (SY-103 board)

Character generator ICA4 (μPD6142C) is capable of displaying 64 characters in a maximum of 24 columns/12 lines using 5×7 dots. It can also control the display position and size of the characters as well as their background, and these can be selected using the menu.
The composite sync signals selected as follows are supplied by ICA3 to the H SYNC pin (pin 14) of ICA4.

- CHARA SYNC

This is the sync signal of the MONITOR output signal selected by the [S02. PICTURE MONITOR SELECT] menu.
The CHARA SYNC signal is selected by ICA3 when INPUT or DEMOD has been selected by menu S02.

- TBC SYNC

This is the sync signal of the TBC output video signal.
The TBC SYNC signal is selected by ICA3 when TBC OUT has been selected by the [S02. PICTURE MONITOR SELECT] menu or when VD2+TBC has been selected by the [S59. MIXED CHARA OUTPUT] menu.

- REF SYNC

This is the sync signal of the servo reference signal which is selected by the [S40. SERVO REF SELECT] menu.
The REF SYNC signal is selected by ICA3 when ENABLE has been selected by the [I60. CHARACTER RECORD] menu, in other words, when the characters are mixed with the video signal and recorded on tape.

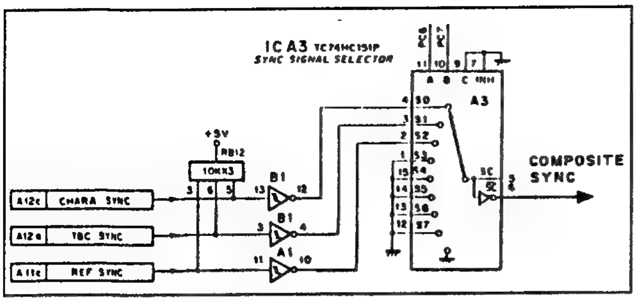


Fig. 4-7-22. Character Generator Sync Signal Selector (SY-103)

The V sync signal which has been separated from the composite signal by R39/C43 is supplied to the V SYNC pin (pin 13). The frequency (min. 4 MHz to max. 7 MHz) of the signal generated by the oscillator inside ICA4 is determined by L1, C184 and C185 which are connected to pins 6 and 7, and the character size in the horizontal direction is regulated. The 8-bit serial data which have been parallel/serial converted by ICE6 are supplied to ICA4 as the control command.

ICB9, A11 and B10 generate the 8 transfer clock signals required to transfer the data from ICE6 to ICA4. The $\overline{\text{CHR WR}}$ signal from the CPU which has been decoded by ICA13 is accepted into latch ICC8 and at the next stage latch ICC8 it is synchronized by the 0.6144 MHz reference clock signal. When pin 8 ($\overline{Q}$) of ICC8 is set low as a result, pin 8 (QD) of ICB9 is set low, NAND gate ICA11 and ICB10 are made active, and the transfer clock signals are sent to ICE6 and ICA4. When ICB9 reaches a count of 8 for the transfer clock signals, pin 8 (QD) is set high, feedback is then applied from ICC8, operation is suspended, and the output of the clock signal to ICE6 and ICA4 is stopped.

In order to set the transferred serial data in the register inside ICA4, the strobe pulse from the CPU is supplied through inverter ICA7 to pin 3 of ICA4.

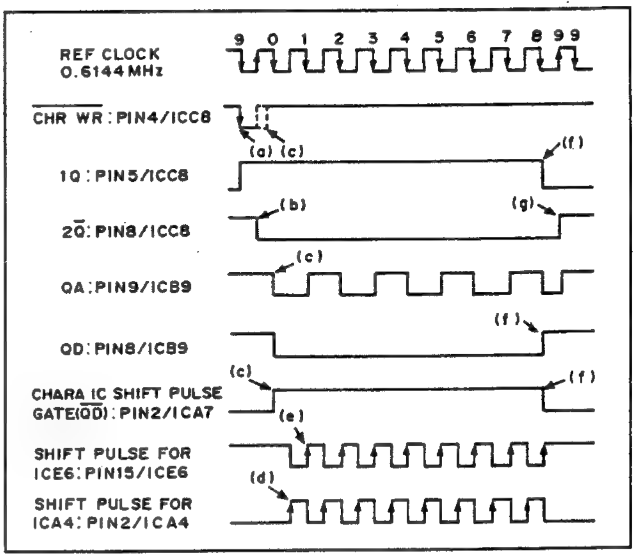


Fig. 4-7-24. Transfer Clock Signals (SY-103)

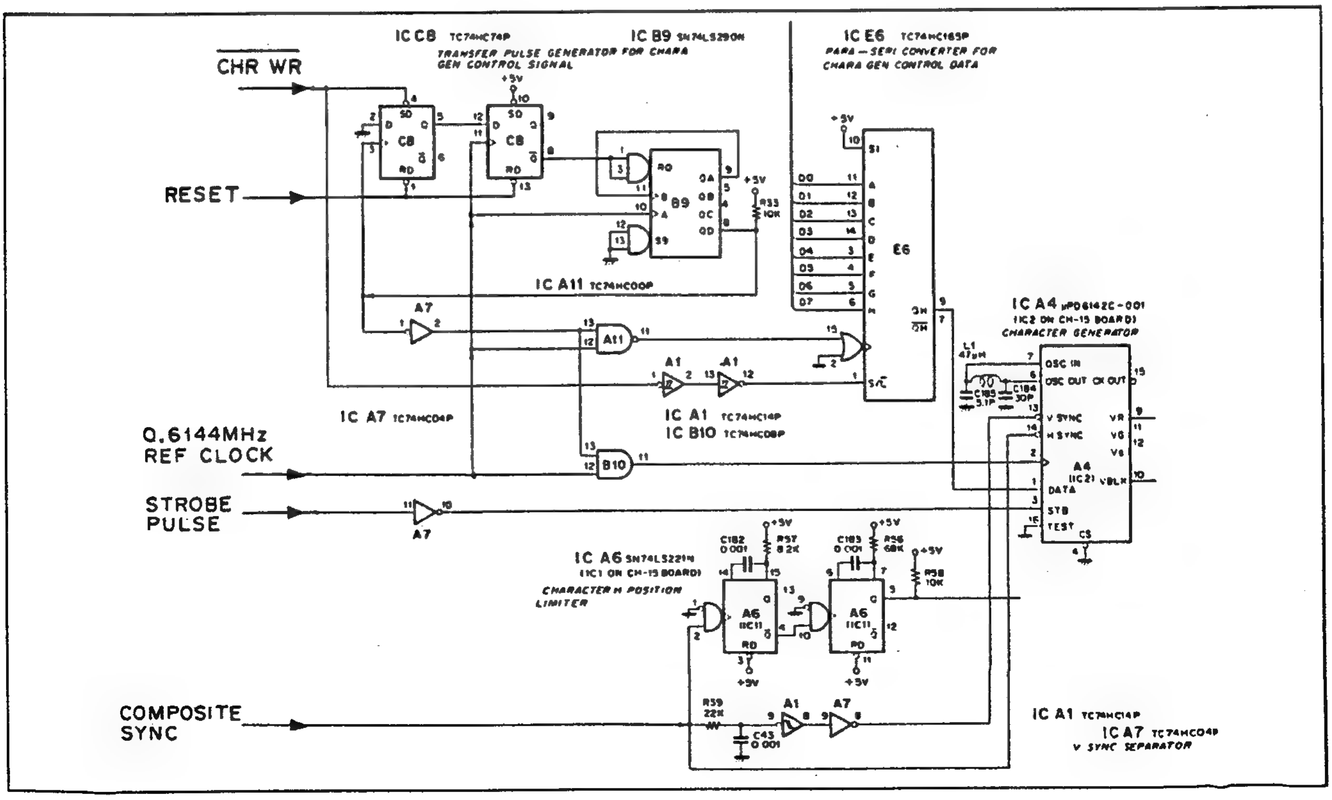


Fig. 4-7-23. Character Generator Input Circuit (SY-103)

(a) When the $\overline{\text{CHR WR}}$ signal is received from the CPU, pin 5 of ICC8 is set high.
(b) It is synchronized with the reference clock signal so that counter ICB9 is set to the enable status at the next rise edge of the reference clock signal.
(c) The counter advances by one count at the next fall edge of the reference clock signal, and the transfer clock signal gate is set to the enable status. When the $\overline{\text{CHR WR}}$ signal does not rise at the gate enable timing, the shift register ICE6 transfer is delayed and a malfunction results.
(d) One bit is transferred to ICA4.
(e) Shift register ICE6 is shifted by 1 bit.
(f) The gate pulse is disabled and pin 5 of ICC8 is reset.
(g) The counter is held after half a clock cycle and the clock signal transfer is suspended.

The characters generated by ICA4 and its gate signal are output to the other circuit boards through the various gates. Monostable multivibrator ICA6 generates the gate signals for adjusting the front porch and back porch width of the character output signal. The signal which is output from monostable multivibrator ICA6 is mixed with the character gate signal by AND gate ICG5, and the character signal is prevented from being mixed in with the front porch (9.4 μ sec) and back porch (1.5 μ sec) signals. Whether or not the character signal and character gate signal are to be valid is controlled by the PA7 signal from the CPU which is supplied to NAND gate ICB2. The PA7 signal from the CPU is the monitor character enable signal and the PA0 signal is the character recording enable signal. The character signal is also mixed with the VITC signal by AND gate ICC1 and, in accordance with the BVH-3000/3100 menu settings, the characters can be superimposed onto the VITC signal and recorded on tape.

(9) REMOTE-3 connector interface

The SY-103 board is provided with an interface circuit so that the time code data are output to the REMOTE-3 connector (parallel remote control, D-SUB 50 pins). The data which are output to this connector are synchronized by the system clock signal which is used exclusively for the REMOTE-3 connector. The system clock signals are created by dividing down the 14.31818 MHz (or 14.5 MHz for EBU) reference clock signal. While LTC reader ICC6 is outputting data, the system clock signal is stopped by the BSRL signal (pin 50 of ICC6) to be synchronized with the ICC6 output data. The BSRL signal is set high while ICC6 is outputting data. The following 8 types of data are output from the REMOTE-3 connector in the form of 4-bit×8-digit data strings. These data are output in a single period of the K3 pulse which is output from pin 9 of ICD11. The K3 pulse period is 143.03 μ sec (or 141.24 μ sec for EBU).

TM1	TM2
LTC TC	LTC UB
VITC TC	VITC UB
TCG	UBG

The system clock signals are defined as below.

TC clock signal:
This is the internal reference clock signal for transferring or updating the data.
SMPTE: 0.447 MHz (2.235 μ sec)
EBU: 0.453 MHz (2.207 μ sec)

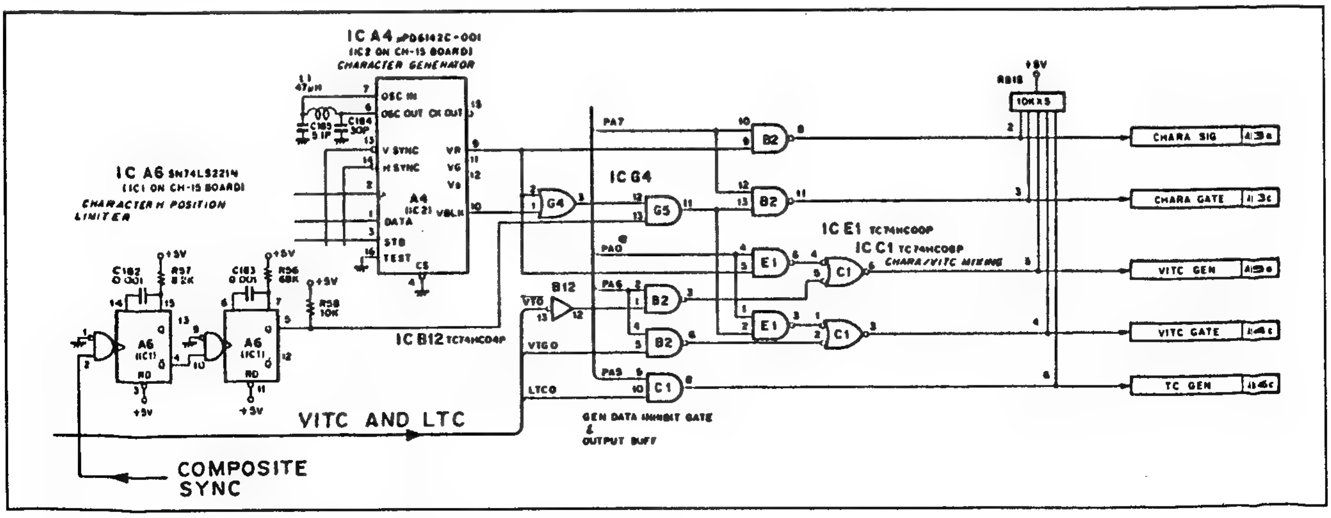


Fig. 4-7-25. Character Generator Output Circuit (SY-103)

Memory WR pulse :
This pulse has the same frequency as the TC clock signal. It is used when an external unit stores the time code data. The memory WR pulse is generated at the timing of the center of the Y0 pulse which is output from pin 4 of ICD9.

Y0–Y2 :
These are the timing pulses for scanning the time data configured by 4 bits×8 digits.

K1–K3 :
These are the timing pulses for scanning the 8 types of timing data.

K4 :
This is the pulse whose period is double that of the K3 pulse. It is used as the sync pulse when accepting the 8 types of data.

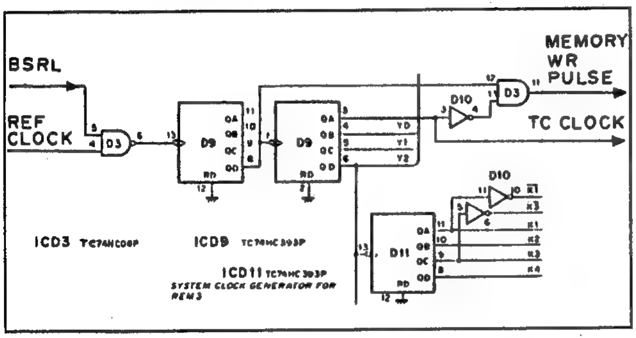


Fig. 4-7-26. System Clock Signal Generator (SY-103)

The digits of "1F–10H" are scanned by the Y0 pulse and the time data are scanned by the K1 pulse. The timing at which the time code reader/generators (ICC3, C6, C10) update the respective data is not synchronized with the system clock signals. ICB5 and B6 (SN74120N) are used in order to synchronize the timing with these signals and make the gates active. The timing is synchronized to the system clock signals by triggering ICB5 and B6 with the trailing edge of the signal indicating that ICC3, C6 and C10 are transferring the data to the memory. TIMER-1/-2 provides the trigger through the software. ICB5 and B6 output the first pulse of the input clock signal when pins S1 and S2 are set low. The time code ICs and REMOTE-3 connector interface are synchronized by using this output pulse as the gate pulse.

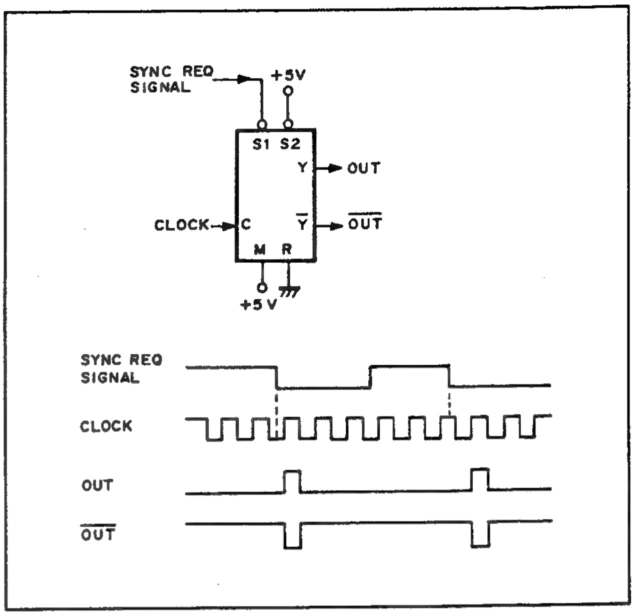


Fig. 4-7-27. SN74120N/ICB5, B6 Operation (SY-103)

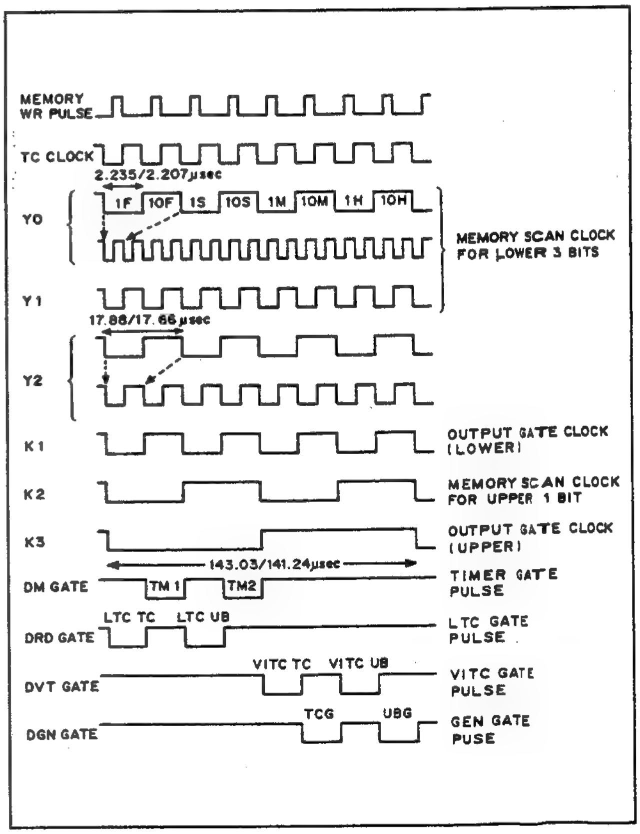


Fig. 4-7-28. REMOTE-3 Output Timing Chart (SY-103)

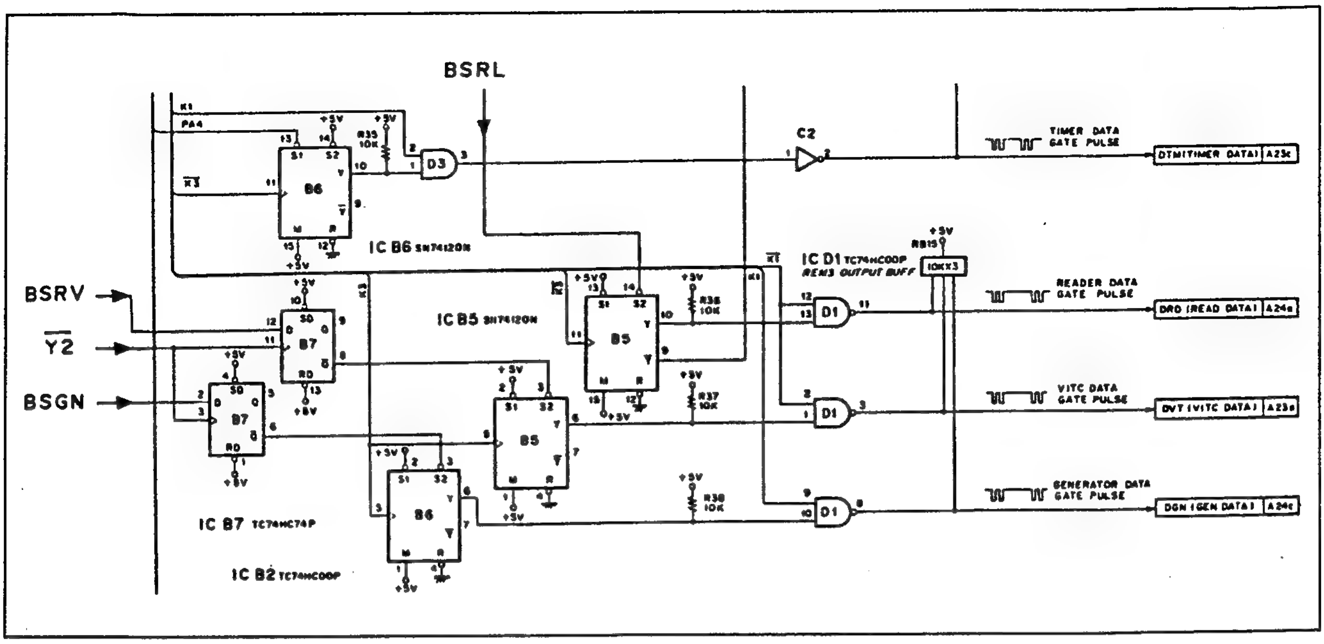


Fig. 4-7-29. REMOTE-3 Output Gate Circuit (SY-103)

ICB3 and B4 are the REMOTE-3 data selector which selects the time code data using the K1 and K3 pulses and which outputs the signals to the REMOTE-3 connector.

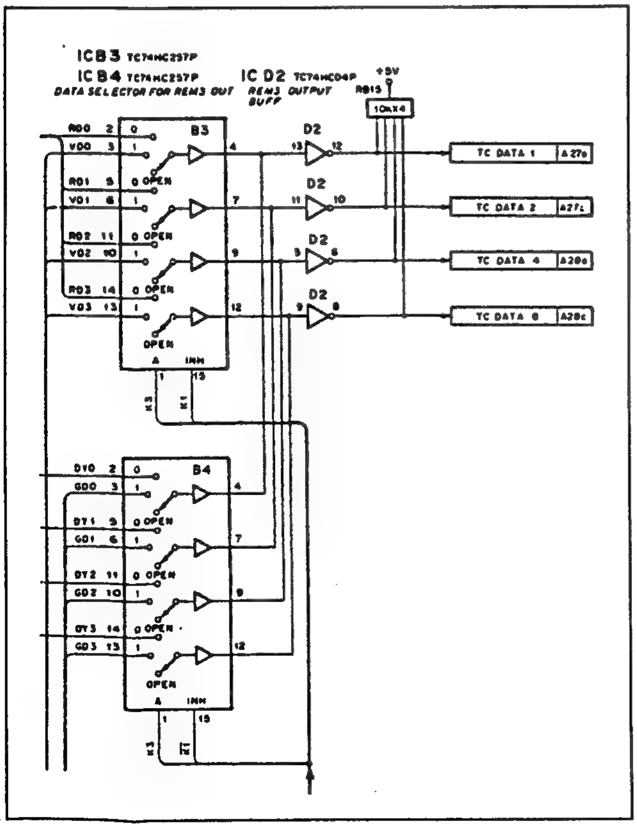


Fig. 4-7-30. REMOTE-3 Data Selector (SY-103)

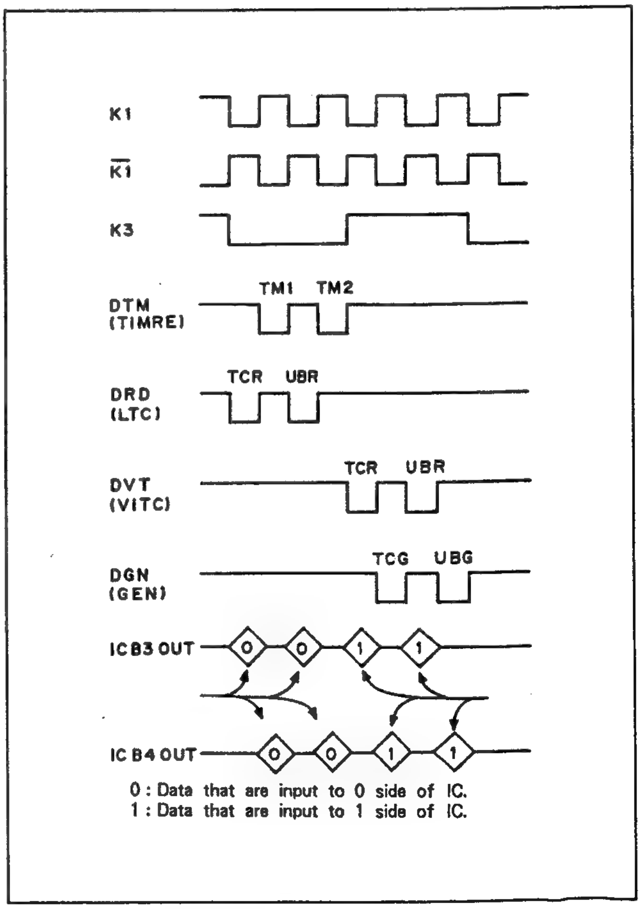


Fig. 4-7-31. REMOTE-3 Data Selector Timing Chart (SY-103)

4-7-3. Control Panel

(1) Outline

The function control panels of the BVH-3000/3100 and BKH-3090 are connected to their respective main units using a single multiple-pin cable (8-pin) in each case. In the case of the BVH-3000/3100, the function control panel can be detached from the main unit and used independently as a remote control unit.
This function control panel is configured with the circuit boards listed below.

- KC-14 board : CPU, power supply, fluorescent display tube driver
- EN-55 board : 21 key switches, LEDs
- DP-63 board : Tape transport control LEDs/switches
- DET-3 board : Search dial pulse detector circuit
- KY-103 board : LEDs, switches, LED decoder/driver, fluorescent display tube

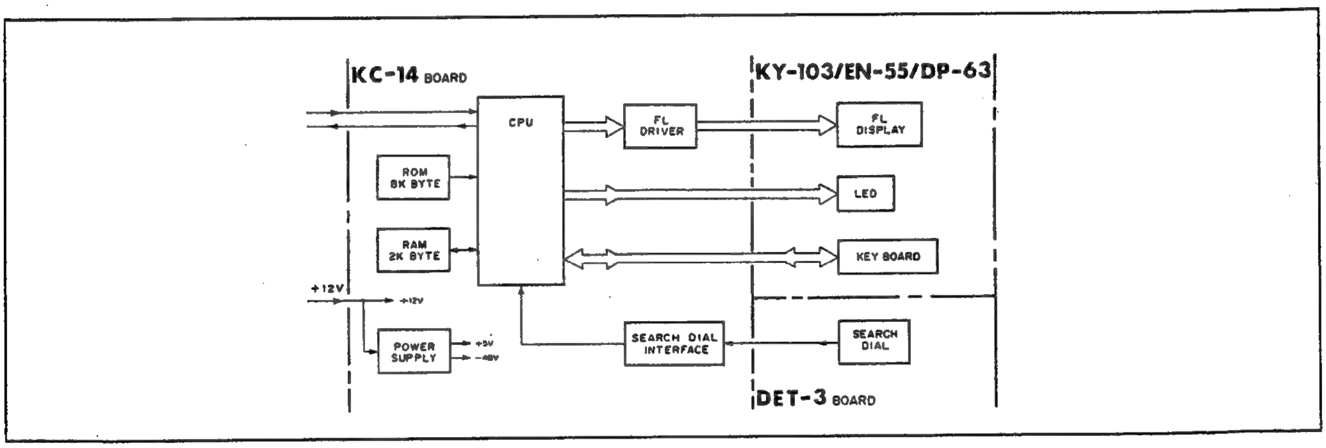


Fig. 4-7-32. Block Diagram of Control Panel

(2) Power supply (KC-14 board)

The +5V, −48V and filament voltage for the fluorescent display tube are generated on the KC-14 board.
The +5V voltage is generated by DC-DC converter ICB3 from the +12V voltage which is supplied to pins 5 and 7 of 8-pin connector CN701. ICB3 oscillates at a frequency of approximately 40 kHz.
ICA4 and Q103 generate the −48V voltage from the same +12V voltage. ICA4 also oscillates at a frequency of approximately 40 kHz. The −48V voltage serves as the power supply for the drive circuit of the fluorescent display tube.
The filament voltage of the fluorescent display tube is generated by Q101, 102 and T101. The 60 kHz square waves which are generated by multivibrator Q101 and 102 are taken out by T101 to provide a 9 Vp-p voltage.

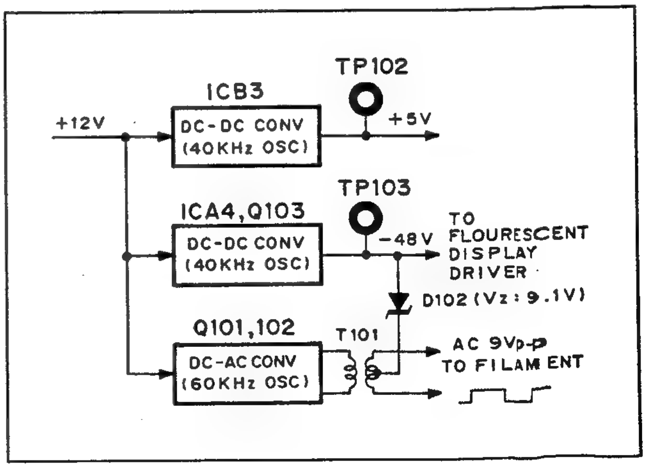


Fig. 4-7-33. Power Supply Circuit of Control Panel (KC-14)

(3) CPU and its peripheral circuits (KC-14 board)

The CPU ICG5 clock signal with its 14.7456 MHz frequency is generated by crystal oscillator X101. The frequency of this signal is further divided down to 1/24 by ICG7 and J7 to provide a clock signal with a frequency of 614.4 kHz and a duty ratio of 50%. This frequency is 16 times higher than the 38.4 kHz frequency of the clock signal which is used for communication.
Q104 serves to generate the low-level CPU reset pulse when the power is switched on and when RESET switch S101 has been pressed.
A non-maskable interrupt (NMI) function is not employed with CPU ICG5. The test mode is initiated by pressing TEST switch S102 which is connected to the INT1 pin (pin 26).
Communication between the BVH-3000 (or the RM-53 board of BKH-3090) is conducted via ICC7 in accordance with the RS-422 format.
The parallel I/O ports of CPU ICG5 are allocated as listed below.

PA7−PA0 : Input port for key data from KY-103/DP-63/EN-55 boards
PB7−PB0 : Output port for key matrix selection of KY-103/DP-63/EN-55 boards
PC7 : Test signal output port (TP109)
PC6 : Display enable port (active high) for fluorescent display tube
PC5 : Dial pulse input port
PC4 : Output port for square waves with a frequency of approx. 4 kHz for the buzzer
PC3 : Dial rotation direction input port
PC2 : 614.4 kHz (16 times the 38.4 kHz frequency used for communication) clock input port
PC1 : Serial data input port
PC0 : Serial data output port
PD7−PD0 : A7−A0 output port/D7−D0 input port
PF5−PF0 : A13−A8 output port
PF6 : Output port (active high) for data latch signals of fluorescent display tube
PF7 : Output port (active low) for scan decoder reset signal of fluorescent display tube.

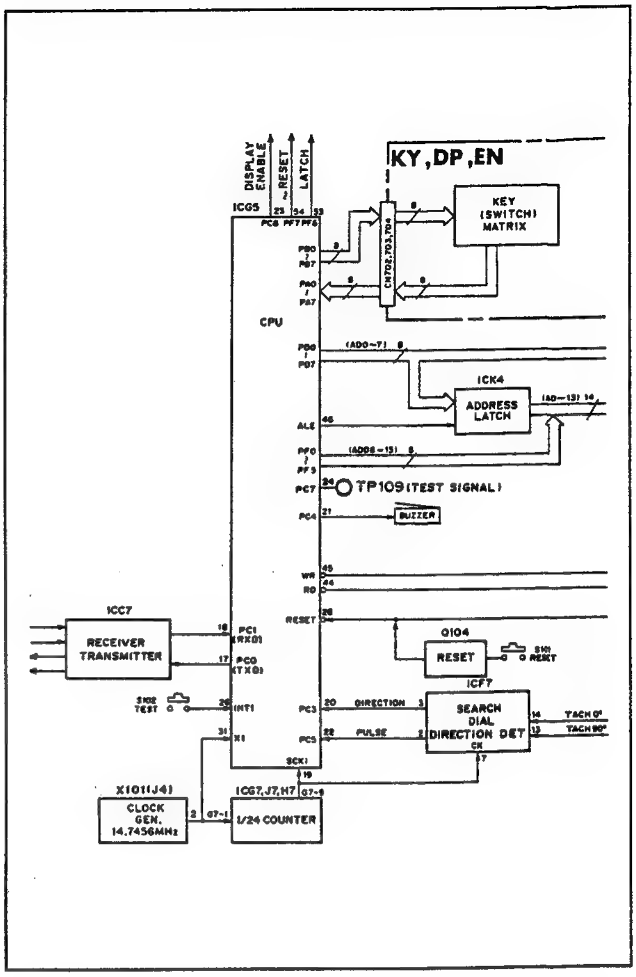


Fig. 4-7-34. CPU and Peripheral Circuits (KC-14)

The addresses of the CPU ICG5 peripheral devices are listed in the table below.

DEVICE	R/W	ADDRESS	SUPPLIED FROM
ROM ICJ5	R	0000−1FFFH	ICG5 PIN-52 (A13)
RAM ICJ6	R/W	2000−27FFH	ICKI7 PIN-3
ND1 (UPPER)	W	3000−3007H	CIF4 PIN-3
ND1 (LOWER)	W	3008−300FH	ICF4 PIN-6
LED LATCH	W	3800−3807H	ICF6 Y7-0

(4) Fluorescent display tube driver (KC-14 board)

CPU ICG5 on the KC-14 board is responsible for controlling fluorescent display tube ND1 and for generating the character patterns.
On its upper and lower lines, the fluorescent display tube displays 40 characters in each case. A character is composed of 5 columns by 7 lines.

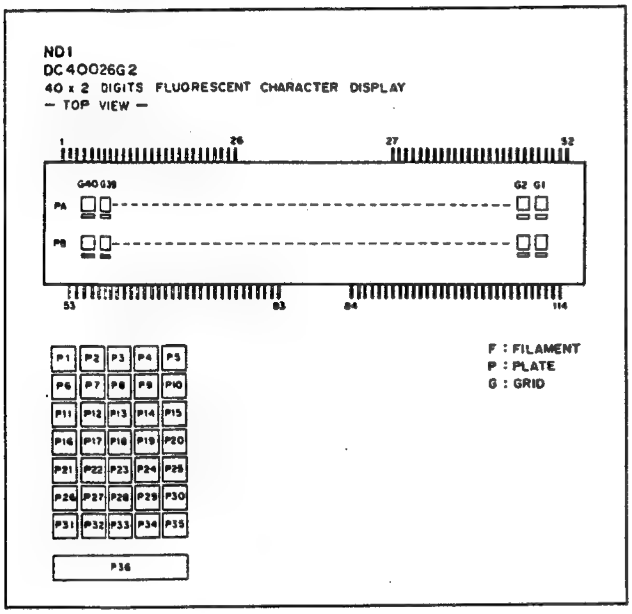


Fig. 4-7-35. Fluorescent Display Tube (ND1/KY-103)

(a) Display pattern latches

The 40 characters on the upper line of fluorescent display tube ND1 are latched to data latch ICM5, K3, J3, H3 and G3 while the 40 characters on the lower line are latched to data latch ICE3, F3, C5, D5 and E5. When the CPU is writing the character data into address 3000–3007H, the upper line 40-character latch signal is output from pin 3 of address decoder ICF4. When the CPU is writing the character data into address 3008–300FH, the lower line 40-character latch signal is output from pin 6 of ICF4.
The strobe pulse which is output from pin 53 (PF6 pin) of CPU ICG5 is supplied to the STRB pin of the data latches. As a result, the parallel data are supplied to the display driver (ICM4, K2, J2, H2, G2, E2, F2, C4, D4 and E4). The strobe pulse is further supplied to the clock input pin of D-type flip-flop ICE7 where the blanking signal is created for preventing the "blur" which arise when the character digits move. The blanking output signal from ICE7 is supplied to AND gate ICD6, it is gated with the display enable signal output from pin 23 (PC6 pin) of CPU ICG5, and it is supplied to the EN pin of the data latch.

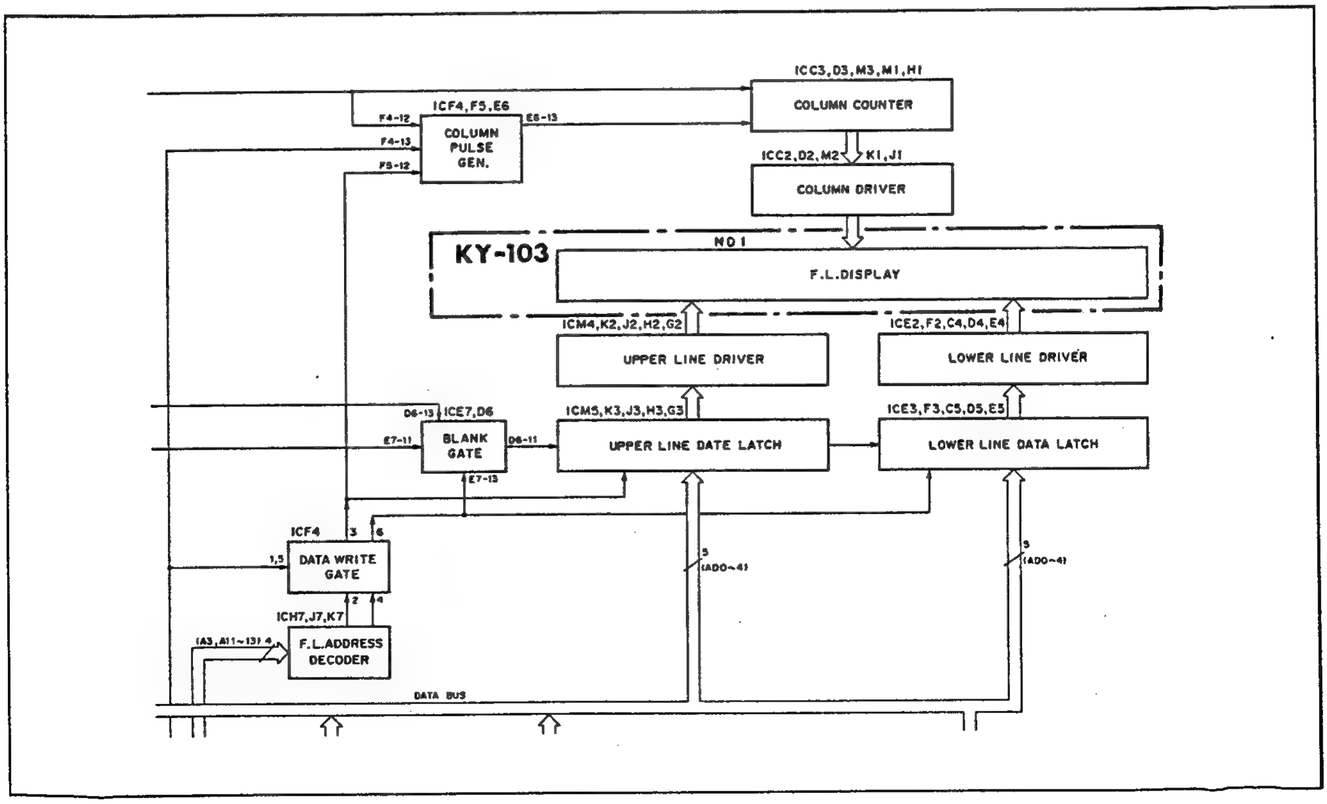


Fig. 4-7-36. Fluorescent Display Tube Driver (KC-14)

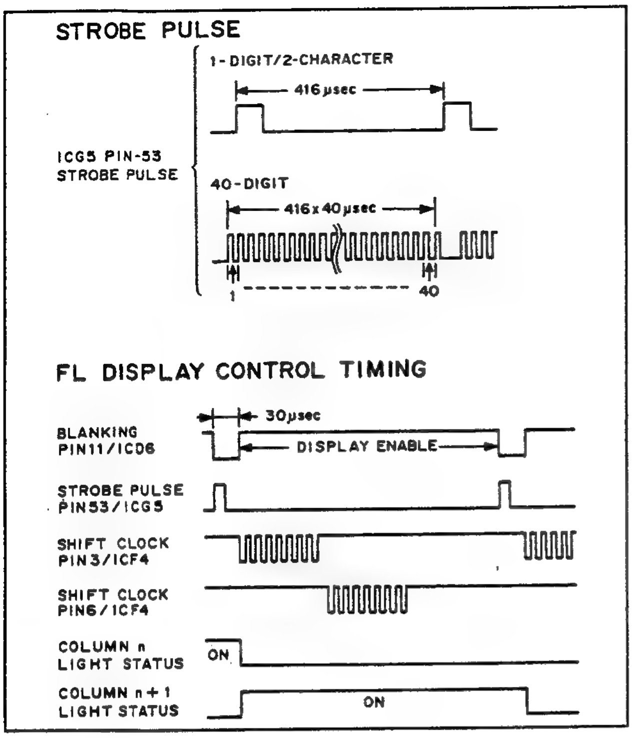


Fig. 4-7-37. Display Pattern Latch Timing (KC-14)

(b) Column decoder/driver

ICC3, D3, M3, M1 and H1 configure the column decoder which is composed of the 9-bit counter and 3-8 decoder. The middle 3 bits (2^3, 2^4 and 2^5) of the 9-bit counter are supplied to the 3-8 decoder. The most significant 3 bits (2^6, 2^7 and 2^8) of the 9-bit counter are compared with the preset value of CS1, CS2 and CS3. It is only when the two values coincide that the data corresponding to the middle 3 bits are sent to the 3-8 decoder and output from the "O1−O8" pins to the grid of the fluorescent display tube. This means that in order to latch the character pattern data of one character, the 3-8 decoder conducts writing 8 times and the output of this decoder is incremented by 1 each time (O1→O8). Only the IC which coincides with the preset value of CS1, CS2 and CS3 is driven.

ICF4, F5 and E6 configure the column clock circuit which is driven by the reset pulse output from pin 54 of CPU ICG5. ICE6 is a monostable multivibrator for setting the pulse width of the column clock pulse to a value equal to or exceeding the rating (1 μsec).

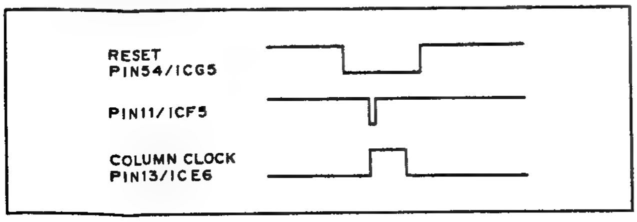


Fig. 4-7-38. Column Resetting, Column Clock Timing (KC-14)

(5) LEDs and clutch driver (KC-14, KY-103 boards)

CPU ICG5 controls the on/off operations of both the LEDs and the clutch on the control panel. Depending on the lamp address "LP7−LP0" from ICF6 on the KC-14 board, IC7, 8, 9, 10, 11 and 12 on the KY-103 board latch "AD7−AD0" and IC2, 3, 4, 5, 6 and 13 drive the LEDs.

The clutch on/off signal is output from pin 16 of latch IC7 and Q1 drives the clutch.

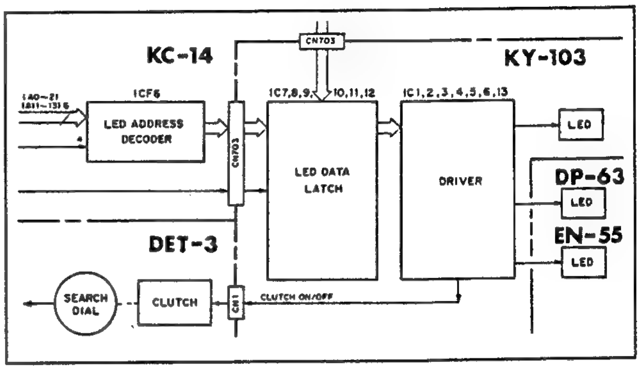


Fig. 4-7-39. LEDs and Clutch Driver (KC-14, KY-103)

(6) Dial pulse detector circuit (KC-14, DET-1 boards)

Mounted on the search dial is a multipolar magnet with an angle resolution of 2.5°. When this dial is rotated, dial pulses "TACH 0°" and "TACH 90°" with a phase difference of 90° are output from the divided magneto-sensing element (DME) on the DET-3 board, these are amplified by IC1 on the DET-1 board, and they are supplied to pins 13 and 14 of rotation direction detector ICF7 on the KC-14 board. The DIR1 signal which indicates the rotation direction of the search dial is output from pin 3 of ICF7 to CPU ICG5 while the dial pulse is output from pin 2 to ICG5. ICF7 is activated by the clock signal with the 614.4 kHz frequency.

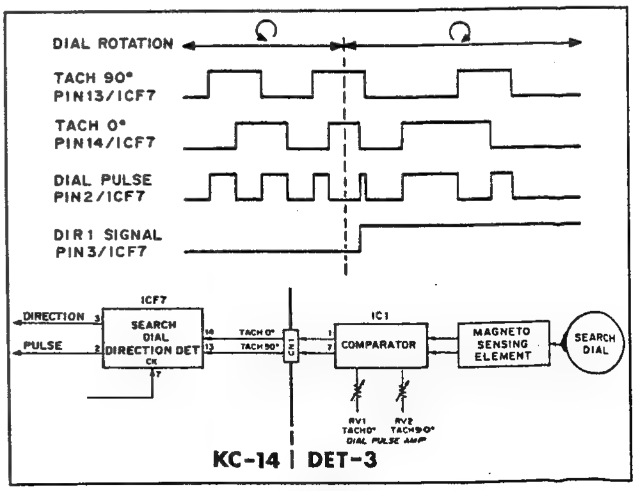


Fig. 4-7-40. Dial Pulse Detector Circuit (KC-14)

4-8. POWER SUPPLY SYSTEM

4-8-1. Outline of Power Supply System

The power supply block of BVH-3000/3100 is the combination of the switching type regulators and series regulators, forming a compact sized, high performance and high efficient power supply. This power supply block can accept AC power input in the range of 100V through 240V, having no need to care for local power supply voltage condition in use.
This power supply block consists of the three printed circuit boards of SP-01 board, SP-02 board and SP-03 board. The SP-01 and SP-03 boards provide the fixed output voltages from these power supply regulators while the SP-02 board provides the variable output voltage to be used in the various motors.

(1) SP-01 board
The SP-01 board consists of the circuits such as the primary rectifier circuit, the starter circuit, ±5V regulators, the regulator for reference +17V and the protection circuits which protect the whole system in case of shorting-circuit and excessive output voltage.

(2) SP-02 board
The SP-02 board consists of the 90V preliminary regulator circuit, and the variable voltage outputs power supply circuits which supply powers to the supply reel motor, the take-up reel motor, the drum motor and to the capstan motor. The variable output voltage power supplies are receiving the input control voltages from the respective motor driver circuits and provide the output voltages in proportion to the input control voltages. These circuits protect the driver circuits using the excess power protection circuits.

(3) SP-03 board
The SP-03 board includes the ±12V regulators, ±18V regulators, +13V regulator for the blower motor, +12V regulator for fan motor and the PA detecting circuit that is detecting the power active signal when the power input/output conditions are normal.

4-8-2. SP-01 Board

(1) Primary rectifier circuit (SP-01 board)

When the S1 power switch is turned on, the commercial AC power input is supplied to the power supply block through the CB1 circuit breaker on the rear panel. This AC input is bridge rectified by the D101 diode bridge through the L101 and L102 choke coils and the L103 power line filter. The rectified AC power is passed through the R101, R102 and RY-101 rush current protector, and is sent to the group of smoothing capacitors.
The other power line filter L104 is installed even after rectification for the purpose of suppressing the switching regulator noise in the vicinity of its generating area. The power line filters are installed in the SP-02 and SP-03 boards too.

(2) Starter (SP-01 board)

IC102 and T105 are the self-exciting type switching regulator circuit, functioning as the starter circuit. When power is turned on, the starter begins to work and supplies the power to the +5V switching regulator control circuit board (UR-20-C1 board). After the +5V power supply system has built-up its operation, the +5V switching regulator sends the control signal voltage that is generated inside, to D107 that stops the starter circuit operation. The D124 and D223 diodes work as the power switches for the control board.

(3) +5V power supply (SP-01 board)

The +5V power supply circuit consists of the half-bridge inverter circuit employing the PWM control method. It supplies not only +5V but also −5V and +17V control preliminary output. The +5V is fed back to IC171 on the UR-20-C1 board for voltage control.

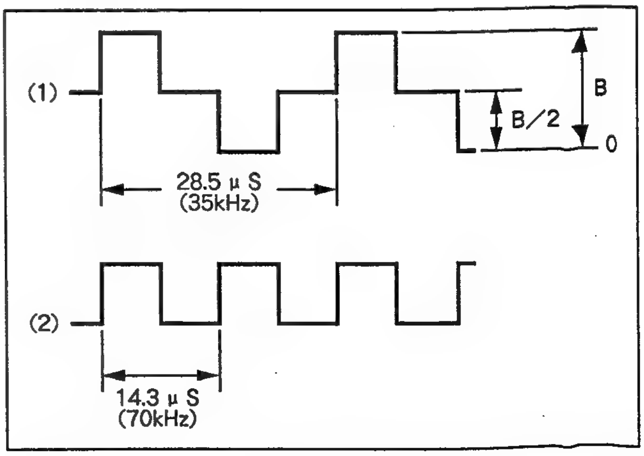


Fig. 4-8-1. Switching Waveform (SP-01)

The half-bridge inverter circuit is made of Q101, Q102, C128, C129 and T101. The primary side rectified voltage is converted to the alternating voltage as shown in Fig.(1), and is sent to the T101 converter transformer and the secondary voltage is obtained in proportion to the winding's turn ratio of the T101 transformer. The secondary output voltage is rectified by the D201 and D202 fullwave rectifier to generate the output shown in Fig.(2). It is smoothed out by the smoothing circuit of L201, C214 through C216 where alternating current is converted to DC current. The output voltage level is determined by the primary rectified voltage and the ON/OFF ratio of the repeating signal waveform. The DC output voltage is passed through the filter consisting of L202, L203, C217 and C218, and is sent to respective loads through connectors. The supplied voltage across the loads is fed back to IC201 on the UR-20-C1 board through the filter on the UR-20-F board, so that it is compared with reference voltage. The difference voltage between load's voltage and reference voltage is added to the IC171 error amplifier where this difference voltage regulates the output pulse width until the output load voltage is regulated.
The IC171 output pulse signal is sent to the Q101 and Q102 switching transistors through the Q171 and Q172 drivers and the T103 and T104 drive transformers. This power supply has the protection against overload that the primary current is detected by T102 and is fed back to IC171 in order to control the PWM pulse width. The characteristics of excessive-load protection circuit is determined by R179, R182 and R185. The output voltage is detected by D178 and D176. When an excessive voltages should be detected, it drives the D177 thyristor to stop output. The rush current caused by the charging current of the primary circuit's smoothing capacitors in the timing of power on, is limited by R101, R102 and RY101. When the switching regulator starts working, the rise-up of the output voltage is controlled to become slow rise-up by means of C178 and R195 of the UR-20-C1 board. The excessive current is thus prevented from flowing. Q174 is the detector circuit for the voltage to be supplied to the UR-20-C1 board. The IC171 is prohibited from functioning until the supply voltage reaches higher than 9V. During when the input voltage remains low, IC171's internal switching transistor has longer ON period, so that IC171's PWM modulation working range is limited by R189.

(4) −5V power supply (SP-01 board)

The −5V power supply is obtained from the +5V power supply circuit. The T101 +5V power's converter transformer has its secondary winding output that is smoothed out by D203, L204 and C219 and is then regulated by the series regulator consisting of Q209 and IC203 so that the −5V power is generated. The −5V power supply system also has the voltage detection across the load in the same manner as in the +5V power supply system. The −5V SENSE signal thus obtained, is fed back and is used for regulation. The excess current is detected for power supply protection by R242 through R245, R263, IC203 and Q216, and the excess voltage is detected by Q206 and D211 for the purpose of power supply protection.

(5) Control-use +17V power supply (SP-01 board)

The control-use +17V power supply is obtained from the +5V power supply circuit. The T101 +5V power's converter transformer has its secondary winding output that is smoothed out by D204, L205 and C221, and is regulated by the series regulator consisting of IC201, Q202 and Q203 so that the control-use +17V is generated. When the +17V output voltage becomes higher, the load for +5V power system is lightened by D208, Q205 and Q204 so that the output voltage should be corrected. The excess voltage is detected by D207 and the excess current is detected at the same time by PS202 and are used for their protection.
On the other hand, because the variable output voltage power supply systems are made to floating, the T101's secondary winding output is again separated by T201 and is then smoothed out by D205, L206 and C222 to generate the control-use +17V (F+17V) that is sent to the SP-02 board. The excess voltage is detected by Q201 and excess current is detected by PS203 and are used for system protection.

(6) Sync pulse generator (SP-01 board)

The one-shot multivibrator IC207 is the sync pulse generator. The generated sync pulse is supplied to the SP-02 and the SP-03 boards through the buffers Q214 and Q215 at the next stage, so that the switching regulators in the SP-02 and SP-03 boards are made synchronized. Because the SP-02 board's switching regulator that is supplying power to the various motors, has the floating output, the Q215 buffer output is supplied outside through the T202 pulse transformer.

(7) Low output and high output voltage protection (SP-01 board)

When the output voltage becomes too low, the positive voltage outputs of the fixed output type switching regulators and series regulators, are compared with the reference +5V by Q212 while their negative output voltages are compared with the reference −5V by Q213 for detection. In the variable output type power regulators, the pre-output voltage is used for detection. When the excessive low output is detected, the LVP signal is sent from the SP-02 and SP-03 boards to Q212. If the outputs are short-circuited, and the shorting condition remains longer than the pre-set time that is determined by the time constant of R261/C231 or R254/C179, the D177 is turned on to stop the +5V power supply and then stop the all regulator outputs. If all regulator outputs should be stopped, turn off the equipment POWER switch and wait until the primary circuit's rectifying voltage is discharged (approx. one minute). Q211 is the circuit that resets the C231 timer when the power is turned on. D207 is the excessive high output voltage detector that stops the regulator outputs when any trouble is detected.

4-8-3. SP-02 Board

(1) Control-use F17V power supply (SP-02 board)

This circuit consists of the Q209, Q210 and IC202 series regulator, using "F+17V" that is supplied from the SP-01 board.

(2) 90V pre-regulator (SP-02 board)

This circuit consists of Q101, Q103, T101, T102, T103, T104, UR-20-C4 board and peripheral circuits. It provides 90V output with maximum 150 Watts that are used for pre-power voltage supplies for the various motors. The circuit configuration is, same as +5V power supply circuit, the half-bridge inverter type switching regulator, using externally synchronized PWM control system. The bridge type rectifier circuit of D202 and D203 is used. Considering the case of non-load conditions, the R202 and R203 idling resistors are inserted. D228 and D477 are installed for the purpose of regulator protection.
IC201 and Q211 detect the overall power consumption of total motor systems so that the power supply regulator should be protected from the excessive heavy load. When the excessive load is detected, the "POWER SENSE" signal is generated to indicate this condition and is sent to the SV-90 board.

When the pre-regulator output voltage becomes too low due to its internal trouble, it is detected by Q214 and D219 and the LVP signal is sent to the SP-01 board through the IC205 photo-coupler so that all systems stop operation.

(3) S REEL VH power supply

This circuit is the variable output voltage power supply for the supply reel motor. This is the chopper type dc-dc converter circuit that operates with externally synchronized PWM system. The dc-dc converter circuit is made of Q201, Q202 and D203. Q201 and Q202 work as the switcher while D203 works as the fly-wheel diode. They are connected to the next circuit of L203 and C207 smoothing circuit. The "S-REEL VH CONT" voltage that is supplied from the motor driver RM-43 board is sent to the dc-dc converter through the UR-20-C6 board. The UR-20-C6 board controls the voltage amplification gain of this regulator so that the output voltage becomes ten times of the input voltage. Q672 of the UR-20-C6 board is the voltage detector of the "S-REEL VH CONT" voltage, stops output when the output voltage becomes too low.
T205 on the SP-02 board works as the input current detector. Because the input voltage and amplification efficiency maintain a constant relationship, the UR-20-C6 board regulates the output power to be maximum 80 Watts. When the output becomes higher voltage with lower current, internal diodes tend to generate the non-linear characteristics. The R257 resistor is providing offset to the T205 transformer that cancels the diodes' non-linearity and improves the power protection accuracy.
The peak value of the switching current is detected by IC203 and D232 that functions to protect the power supply circuit from the excess output current when the output becomes lower voltage. The detected signal is sent to the D477 gate through D230, D229, Q212 and Q213, that puts D477 on which stops the work of the 90V pre-regulator.

(4) T REEL VH power supply (SP-02 board)

This is the power supply for the take-up reel motor. The circuit configuration of this circuit is same as that of the S REEL VH power supply circuit.

(5) CAPSTAN VH power supply (SP-02 board)

This is the power supply for the capstan motor. The circuit configuration of this circuit is same as that of the S REEL VH power supply circuit, but this circuit has the amplification gain of five times for the input "CAP VH CONT" signal and the maximum output power is 20 watts. D238 and D239 are the high output voltage detection circuit. When the output voltage becomes high, the output is stopped in order to protect the driver circuit.

(6) DRUM VH power supply (SP-02 board)

This is the power supply for the drum motor. The circuit configuration of this circuit is same as that of the S REEL VH power supply circuit, but this circuit has the amplification gain of five times for the input "DRUM VH CONT" signal and the maximum output power is .45 Watts. The protection against the high voltage output works in the same manner as that of the CAPSTAN VH power supply.

4-8-4. SP-03 Board

(1) ±18V power supply (SP-03 board)

The ±18V power supply circuit has the same circuit configuration as that of the +5V power supply, of the half-bridge inverter type switching regulator, of the externally synchronized PWM control system. It is controlled by the UR-20-C5 board. Because the load of the ±18V power regulator has the wide range of variation, the idling resistor of R269 is used.

(2) +13V blower solenoid power supply (SP-03 board)

The +13V power supply circuit has the same circuit configuration as that of the +5V power supply, of the half-bridge inverter type switching regulator, of the externally synchronized PWM control system. It is controlled by the UR-20-C2 board. In order to use the air-threading blower in the floating circuit, the L210 filter is inserted.

(3) ±12V power supply (SP-03 board)

This ±12V power supply is consisting of series regulator, and is connected to the afore-mentioned +13V power supply circuit and is output. The ±18V is used for controlling power source of this power supply circuit. The output voltage across load is detected in the same manner as ±5V power supply circuit. The detected voltage across the load is called as ±12V SENSE that is fed back for power supply regulation.

(4) +12V fan motor power supply (SP-03 board)

The power source for the +12V fan motor is obtained by connecting the series regulator IC206 in the output of the +13V blower solenoid power supply circuit.

(5) Power active detection circuit (SP-03 board)

This circuit consists of Q213, IC205, and Q207 through Q210.
The circuit consisting of Q213 and IC205 functions to detect whether the power supplies are working normally or not. If the output voltage is detected to be too low, the detected output is sent to respective power supplies through the driver circuits of Q207 through Q210.
The pin 5 of IC205 is receiving the secondary winding's output voltage of T101 of the +13V switching regulator through D201. The voltage level of the primary circuit rectifying circuit is detected in this way. When the voltage of the primary circuit rectifying voltage is too low, Q210 is turned off. Q211 and Q212 are the detection circuit for excessive high output voltage of −13V power supply. If the excessive high output voltage is detected, the "STOP" signal is sent to the SP-01 board.

SECTION 5
PERIODIC CHECK AND MAINTENANCE

5-1. PERIODIC INSPECTION SCHEDULE

The table on the right presents the time periods for cleaning, adjusting or replacing major parts. The replacement period depends upon usage conditions, so use the period indicated as a reference when making maintenance inspection schedules. The times indicated here are according to a head hours meter. If the part in question cannot be clearly determined, refer to the relevant page (Page of Section D column in table).

Note 1 : Part No. of Entrance Slant Guide Assy
A-6046-062-A is equivalent to A-6046-056-A or B

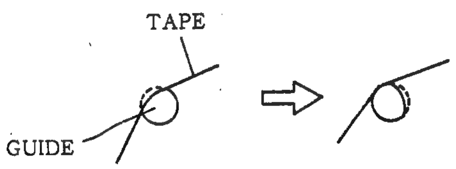
Note 2 : Part No. of Exit Slant Guide Assy
A-6046-061-A is equivalent to A-6046-055-A or B

Note 3 : Type No. and Part No. of Upper Drum Assy
DMR-33-R A-6052-096-A : for BVH-3000
DMR-34-R A-6052-099-A : for BVH-3000PS
DMR-35-R A-6052-095-A : for BVH-3100
DMR-36-R A-6052-100-A : for BVH-3100PS

Note 4 : Type No. and Part No. of Head Drum Assy
DMH-33A-R A-6050-477-A : for BVH-3000
DMH-34A-R A-6050-484-A : for BVH-3000PS
DMH-35A-R A-6050-476-A : for BVH-3100
DMH-36A-R A-6050-485-A : for BVH-3100PS

Note 5 : "↑"
The symbol "↑" in the table means that when the part indicated in the upper column is replaced, it is done so automatically.

Note 6 : "ROT"
The symbol "ROT" in the table means that the guide is to be rotated so that the worn away portion of the guide does not contact the tape.



Note 7 : "CLN", "ADJ", "RPL"
CLN : Cleaning
ADJ : Adjustment
RPL : Replacement

BLOCK NAME OR PART NAME	PART NUMBER	PAGE OF SECTION D	DAILY	2500 HOURS	5000 HOURS	7500 HOURS	10000 HOURS	12500 HOURS	15000 HOURS	REMARKS
TAPE PATH			CLN	ADJ	ADJ	ADJ	ADJ	ADJ	ADJ	Refer to section 5-2 for cleaning and section 9-2 for adjustment.
BEARINGS OF GUIDE ROLLER 1,2	3-656-948-00	D-8,9,10		RPL	RPL	RPL	RPL	RPL	RPL	After replacement, refer to section 9-2 for the tape running adjustment.
MOVABLE GUIDE ASSY	A-6046-059-A	D-17,18,19	CLN				RPL			Refer to section 6-2 for replacement and to section 6-2-2 for adjustment.
ENTRANCE SLANT GUIDE ASSY	NOTE 1. A-6046-062-A	D-17,18,19	CLN		RPL		↑		RPL	Replace in accordance with section 6-4-1.
EXIT SLANT GUIDE ASSY	NOTE 2. A-6046-061-A	D-17,18,19	CLN		RPL		↑		RPL	Replace in accordance with section 6-4-2.
TAPERED GUIDE	3-714-588-01	D-17,18,19	CLN	ROT	RPL	ROT	↑	ROT	RPL	After replacement, check the RF waveform in accordance with section 6-12.
IP ROLLER SHAFT ASSY	A-6046-027-E	D-20,21,22	CLN		RPL		RPL		RPL	
IP DRIVING ASSY	A-6037-022-A	D-39,40,41				RPL			RPL	
DEMAGNETIZING OF HEADS				When required, demagnetize the heads referring to section 5-5.						
TRACKING CHECK				Every 250 hours, check the RF waveform refferring to section 5-3. If necessary, perform the adjustment in accordance with section 9-5-2.						
UPPER DRUM ASSY	NOTE 3	D-14,15,16	CLN	Check the head projection every 500 hours. If necessary, replace the upper drum.						Check the head projection referring to section 5-4. When the upper drum has been replaced, perform the adjustment in accordance with the flowchart shown in section 6-1-2.
HEAD DRUM ASSY	NOTE 4	D-14,15,16	CLN		RPL		RPL		RPL	Replace in accordance with section 6-2. After replacement, perform the adjustment in accordance with the flowchart shown in section 6-2-2.
BRUSH SLIP RING ASSY	A-6053-043-A	D-14,15,16		RPL	↑	RPL	↑	RPL	↑	Replace in accordance with section 6-3.
REEL BRAKE				ADJ	ADJ	ADJ	ADJ	ADJ	ADJ	Refer to section 6-2 for the brake torque adjustment.
REEL STOPPER PIN	3-673-680-11	D-5,6,7				RPL			RPL	After replacement, verify the height of the reel table in accordance with section 9-2.
REEL CLAW ASSY	X-3651-315-0	D-5,6,7				RPL			RPL	If reel table has been removed when the reel claw assy is replaced, verify the height of the reel table in accordance with section 9-2.
BRAKE BAND	X-3673-601-0	D-5,6,7				RPL			RPL	Replace in accordance with section 6-6.
BRAKE SOLENOID	1-454-304-00	D-5,6,7				RPL			RPL	Replace in accordance with section 6-7.
S-REEL MOTOR	8-835-231-01	D-5,6,7				RPL			RPL	Replace in accordance with section 6-5-1.
T-REEL MOTOR	8-835-231-01	D-5,6,7				RPL			RPL	Replace in accordance with section 6-5-2.
S-TENSION ARM ASSY	A-6042-025-A	D-8,9,10	CLN	ROT	ROT	RPL	ROT	ROT	RPL	Replace in accordance with section 6-8.
PINCH ROLLER ASSY	A-6035-036-A	D-23,24,25	CLN	RPL	RPL	RPL	RPL	RPL	RPL	Replace in accordance with section 6-10.
SOLENOID OF PINCH ROLLER	1-454-432-11	D-23,24,25			ADJ	RPL		ADJ	RPL	Replace in accordance with section 6-11.
JOINT PIN OF PLUNGER	3-714-535-01	D-23,24,25			RPL		RPL		RPL	Replace referring to section 6-11.
CAPSTAN MOTOR	8-835-232-01	D-23,24,25	CLN		RPL		RPL		RPL	Replace in accordance with section 6-9.
AUDIO/CTL R/P HEAD for NTSC,PS for PS-A4	8-825-771-01 8-825-737-61	D-20,21,22	CLN	RPL	RPL	RPL	RPL	RPL	RPL	Replace in accordance with section 6-13.
AUDIO MONITOR HEAD for NTSC,PS for PS-A4	8-825-770-91 8-825-737-71	D-20,21,22	CLN	RPL	RPL	RPL	RPL	RPL	RPL	Replace in accordance with section 6-14.
HD-07 BOARD	1-606-680-00	D-20,21,22		RPL	RPL	RPL	RPL	RPL	RPL	Replace it when replacing the audio/CTL R/P head or audio monitor head.
AUDIO/CTL ERASE HEAD for NTSC,PS for PS-A4	8-825-725-50 8-825-725-70	D-20,21,22	CLN	When required, replace in accordance with section 6-15.						
FULL ERASE HEAD for NTSC	8-828-957-01	D-17,18,19	CLN	When required, replace in accordance with section 6-16.						
V/S ERASE HEAD for PS,PS-A4	8-825-725-10	D-17,18,19	CLN	When required, replace in accordance with section 6-16.						
BLOWER	1-541-424-11	D-39,40,41			RPL		RPL		RPL	
FAN MOTOR (CONNECTOR PANEL)	1-541-327-11	D-36,37,38			RPL		RPL		RPL	
FAN MOTOR (POWER BLOCK)	1-541-337-21	D-33,34,35				RPL			RPL	
POWER SWITCH	1-570-936-11	D-11,12,13				RPL			RPL	

5-2. CLEANING

1. Clean the parts shown by the arrows in Fig.5-1 with a cleaning piece or a cotton swab soaked in cleaning liquid.

   Note : If tape magnetic material or back coating material adheres to the guide pins of the entrance or exit slant guides, the tape may be severed. Open the movable guide and clean the guide posts and guide flanges sufficiently.

2. Clean the rotary heads by lightly pressing a cleaning piece soaked in cleaning liquid up against them, then slowly rotating the upper drum by hand.

   Note 1 : NEVER do cleaning while rotating the drum if the power is on !

   Note 2 : Always clean the heads in a circular motion. Cleaning the heads in a vertical direction can produce damages. Also, do not use a cotton swab to clean the heads.

3. If dirt is difficult to remove, use alcohol. After cleaning always wipe with a dry cloth.
4. The front shield plate of the audio head which has opened automatically can be opened further by pressing it by hand. If left in this condition, however, air threading cannot be done and the shield is no longer adequate. After opening the plate by hand, always be sure to return it to its original position.

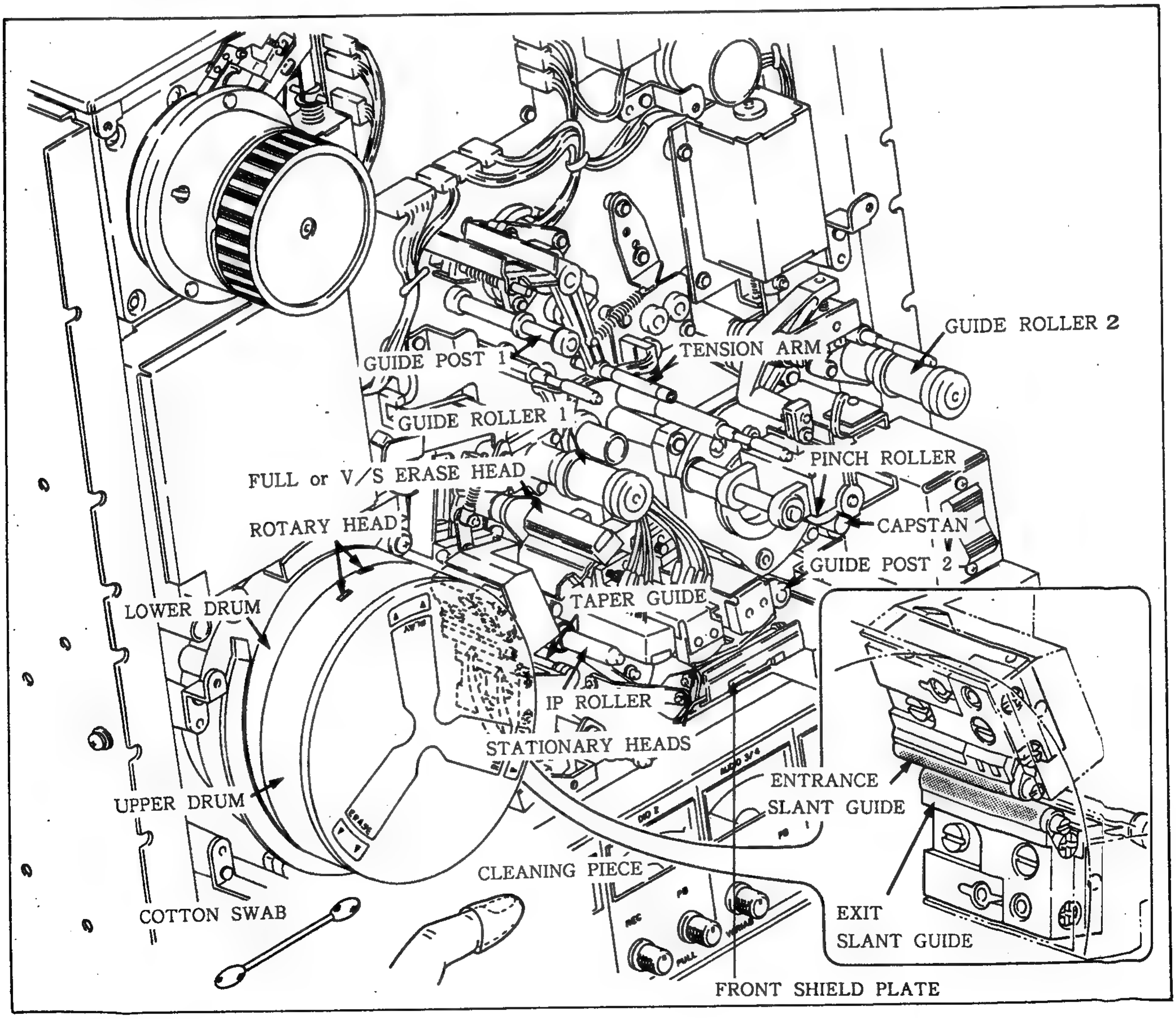


Fig. 5-1. Cleaning of Guide Surfaces and Heads Along Tape Path

5-3. TRACKING CHECK

1. While depressing switch S2 on the SY-103 board, press the [0] key of 21-key section.(Or, select test menu T17. See Section 3-2.) The TTP ADJ mode is assumed and the control panel display is as shown below.

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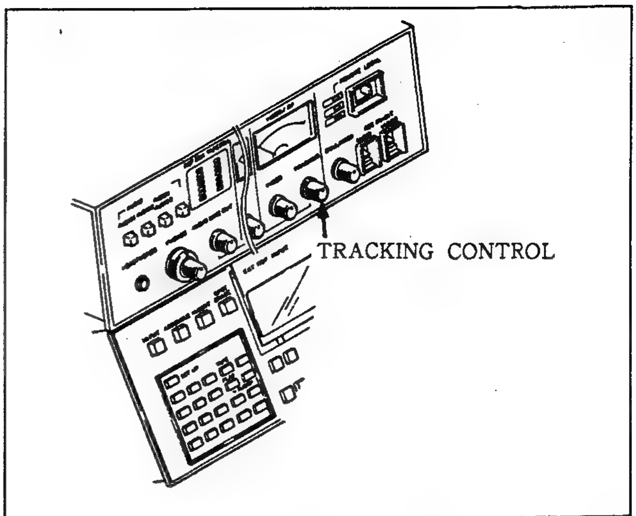
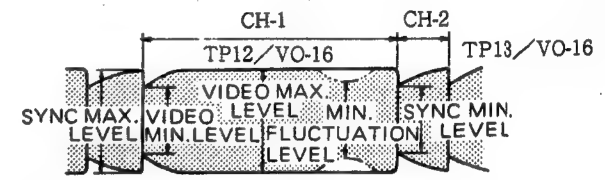
                    >_
```

   Next, key in [C], [8], [0], [SET]. The control panel display becomes as shown below. If a different display appears, key in [C], [8], [0], [SET] once again.

```
>C80_                    > TRACKING ADJ  _
   XXXX XXXX XXXX        >_
```

2. Connect CH-1 of oscilloscope to TP12 of the VO-16 board and CH-2 to TP13.
3. Thread the alignment tape.
4. When the WHITE portion of alignment tape is played back, confirm that the waveform of the RF envelope satisfies the specifications of Fig.5-2. Tracking adjustment is required if the specifications are not met.
5. Pull out the tracking knob and confirm that RF envelope waveform increases and decreases are all at about the same level while the knob is being turned right and left. If there is a great change in waveform, tracking adjustment is required.
6. Turn the tracking knob so that the RF amplitude reaches its maximum. Confirm that there is no change in the RF amplitude even when the tracking knob is pressed inward at the maximum value. If there is such a change, the CTL head position must be adjusted.
7. Key in [C], [0] of 21-key section and press [SET] key.
8. Press the RESET switch S3 on the SV-90 board. Normal operating mode is restored.





$$\text{CH-1 VIDEO RF}: \frac{\text{VIDEO MIN. LEVEL}}{\text{VIDEO MAX. LEVEL}} \times 100 \geqq 80(\%)$$

$$\text{CH-2 SYNC RF}: \frac{\text{SYNC MIN. LEVEL}}{\text{SYNC MAX. LEVEL}} \times 100 \geqq 70(\%)$$

Fig. 5-2. Tracking Check

5-4. HEAD PROJECTION CHECK

Preliminary Information

A. Each head mounted on the upper drum is guaranteed to operate for 500 hours under normal operating conditions.

B. If the projection of the video head (not sync head) is 40 μm or less, replacement of the upper drum is recommended.

C. Use the drum eccentricity adjustment gauge to measure the magnitude of head projection. This gauge comes in two types : an old and a new version which are distinguished by the color (black or white) of the pin inserted in the measurement arm.
New gauge : part no. J-6250-800-A (black pin)
Old gauge : part no. J-6040-750-B/A (white pin)
When the black (or white) pin of this gauge is used repeatedly, it wears so replace it with a new pin as necessary. If the white pin of an old gauge is replaced with the black pin for a new gauge, the old gauge can be used just like a new one.
Black pin : part no. J-6250-810-A

D. Before measuring the head projection or adjusting the eccentricity of the upper drum, always clean the cylindrical surface of the upper drum and the tip of the pin inserted in the measurement arm of the gauge so that the heads will not be damaged.

Check

1. Remove the drum panel.
2. Confirm that the dial gauge probe is mounted at the center of the pin inserted into the measurement arm of the adjustment gauge. If it is not at the center, adjust its position as shown in Fig.5-3.
3. Turn the zero adjustment screw full counterclockwise.
4. While setting the stopper of upper drum adjustment gauge so that it touches the bottom side of the lower drum, turn the fixing knob so that the position is fixed as shown in the figure.
5. To measure the video head projection, turn the dial gauge in the direction of the arrow A as shown in Fig.5-4, then move it in the direction of arrow B and arrow C until the circular mark engraved on the shaft of the fixing knob is half hidden, then return dial gauge towards the drum. (Reference) In measuring the projection of the sync head, turn the dial gauge in the A direction of Fig.5-4, then after pressing it until it reaches direction B, return it toward the drum, and conduct measurement the same as in steps 6 and 7. Correct the sync head projection value as indicated below according to the pin inserted in the measurement arm.
Sync head projection in case of black pin
=measured value−5 μm

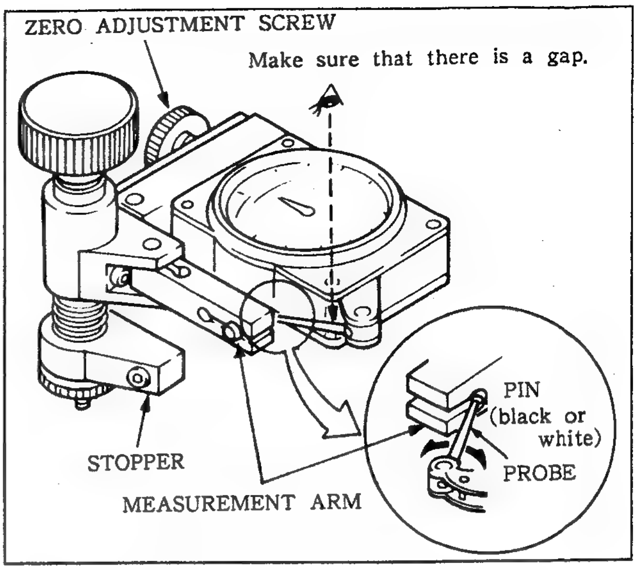


Fig. 5-3. Upper Drum Eccentricity Adj. Gauge

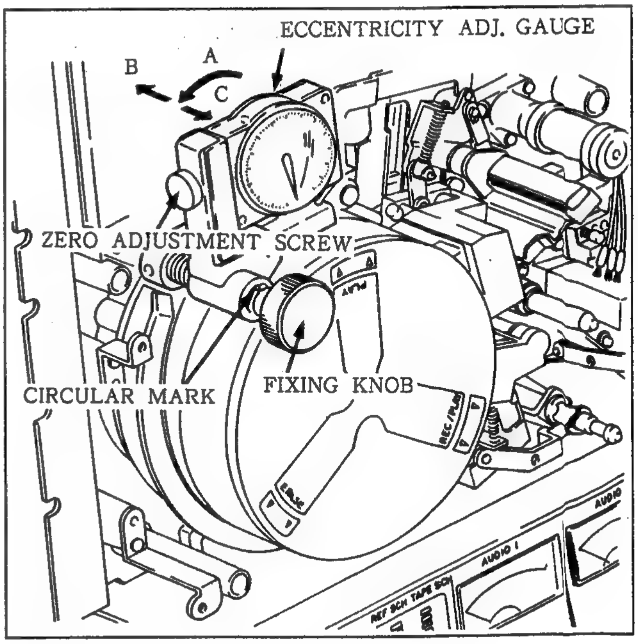


Fig. 5-4. Head Projection Measurement

Sync head projection in case of white pin
=measured value−10 μm

6. Turn the upper drum by hand so as to bring the video head close to the white pin of the gauge. Never touch the head with the pin.
7. Turn the zero adjustment knob so that the gauge indicates zero.
8. Confirm that the projection of the video R/P head and the video PLAY head are both over 40 μm. If the projection of either head is below 40 μm, we recommend that the upper drum be replaced.
9. Turn the zero adjustment screw of the upper drum eccentricity adjustment gauge fully counterclockwise, then remove the gauge.
10. Install the drum panel.

5-5. DEMAGNETIZING THE HEADS

1. Prepare the demagnetizer.
2. Bring the demagnetizer as close to the heads as possible.(Never allow demagnetizer to touch a head!) Then slowly pull the demagnetizer away from the head: when the until is about one meter away from the head, turn off the power to the demagnetizer.

Note : The front shield plate of the audio head which has opened automatically can be opened further by pressing it by hand. If left in this condition, however, air threading cannot be done and the shield is no longer adequate. After opening the plate by hand, always be sure to return it to its original position.

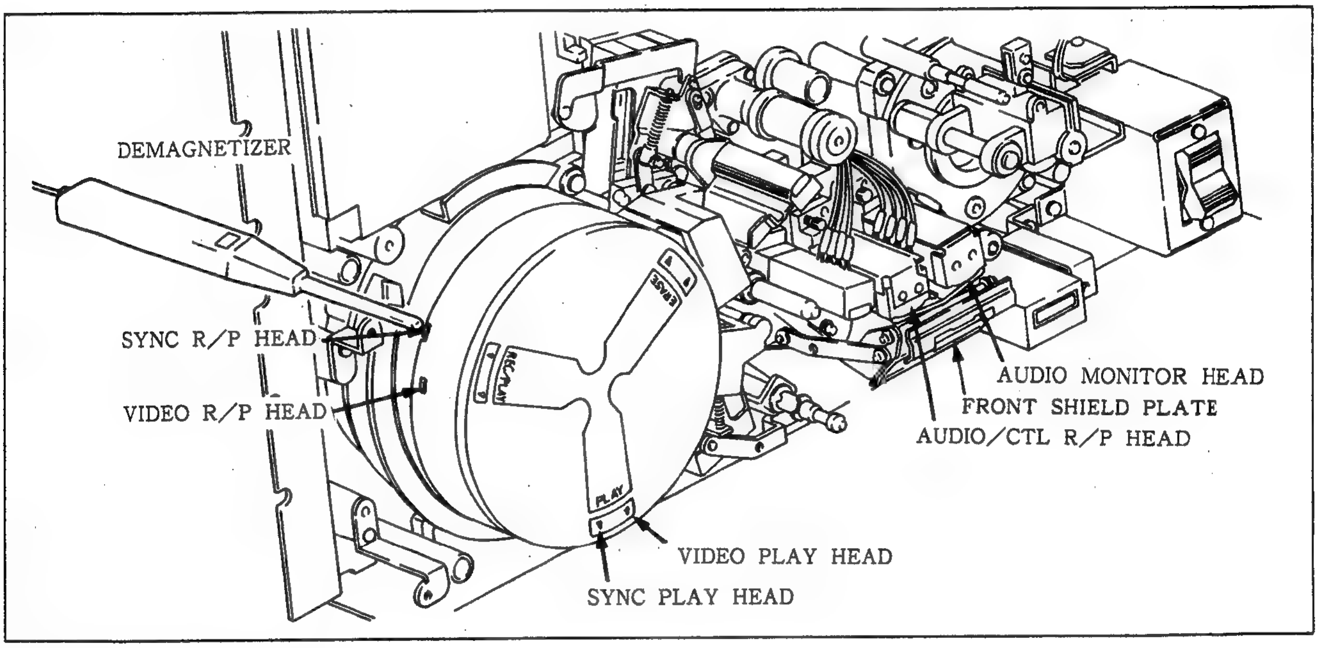


Fig. 5-5. Head Demagnetization

SECTION 6
PARTS REPLACEMENT

6-1. UPPER DRUM REPLACEMENT

Preliminary Information

A. Each head mounted on the upper drum is guaranteed to operate for about 500 hours under normal operating conditions.

B. If the video head projection (distance from drum surface to head tip) is 40 μm or less, we recommend to replace the upper drum.

C. Prepare the following tools for replacement.
Upper drum eccentricity adjustment gauge:
Part no. J-6040-750-A/B (white pin) or
J-6250-800-A (black pin)
Taper screws:
Part no. J-6040-460-A

D. Measure the head projection with the upper drum eccentricity adjustment gauge. In measuring the projection of the sync head with the adjustment gauge, make corrections as follows according to the pin inserted in the head projection measurement arm.
- Sync head projection with black pin
=measured value−5 μm
- Sync head projection with white pin
=measured value−10 μm

E. Before measuring the head projection or adjusting the eccentricity of the upper drum, always clean the cylindrical surface of the drum and the tip of the pin inserted in the measurement arm of the gauge so the heads will not be damaged.

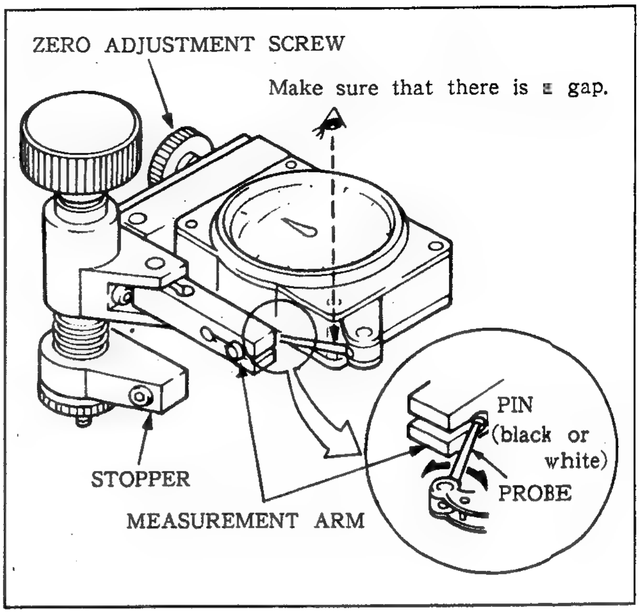


Fig. 6-1. Upper Drum Eccentricity Adjustment Gauge

6-1-1. Replacement

1. While being especially careful not to damage the cylindrical surface of the upper drum, insert a flat-blade screwdriver under the drum lid as shown in Fig.6-2-1, then remove the lid.
2. Remove the three screws securing the DR-13 board.
3. Remove the two screws securing the upper drum.
4. Clean the following parts with a cloth soaking in cleaning liquid. See Fig.6-2-2.
   a. Lower drum flange
   b. Entire perimeter of lower drum lead surface
   c. Guide posts and guide flanges of entrance and exit slant guides
   d. Upper drum install surface
5. Position the upper drum so that the white line on the DR-15 board of the lower drum forms a straight line with the white line on the DR-14 board of the upper drum, then fix in position by alternately tightening two taper screws.
6. Remove the taper screw at the video head and fix the upper drum with a flat washer, spring washer and screws (C4×14). Remove the taper screw on the opposite side and fix in the same manner with screws.

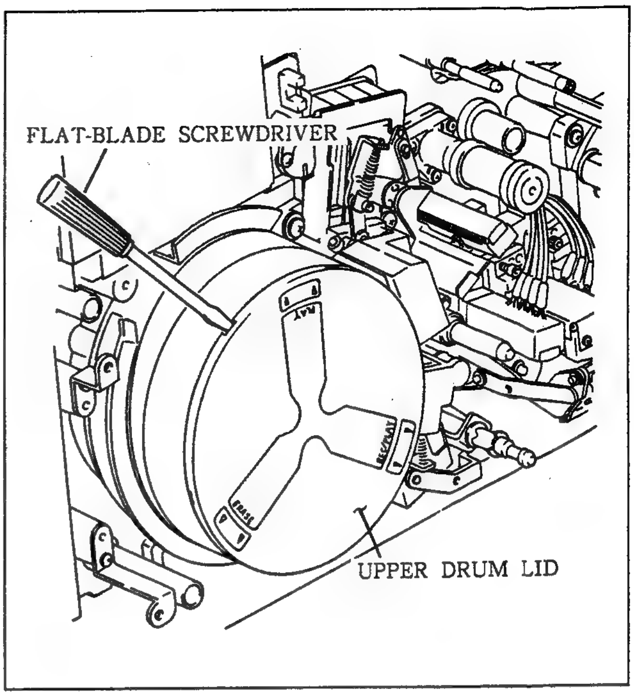


Fig. 6-2-1. How to Remove Upper Drum Lid

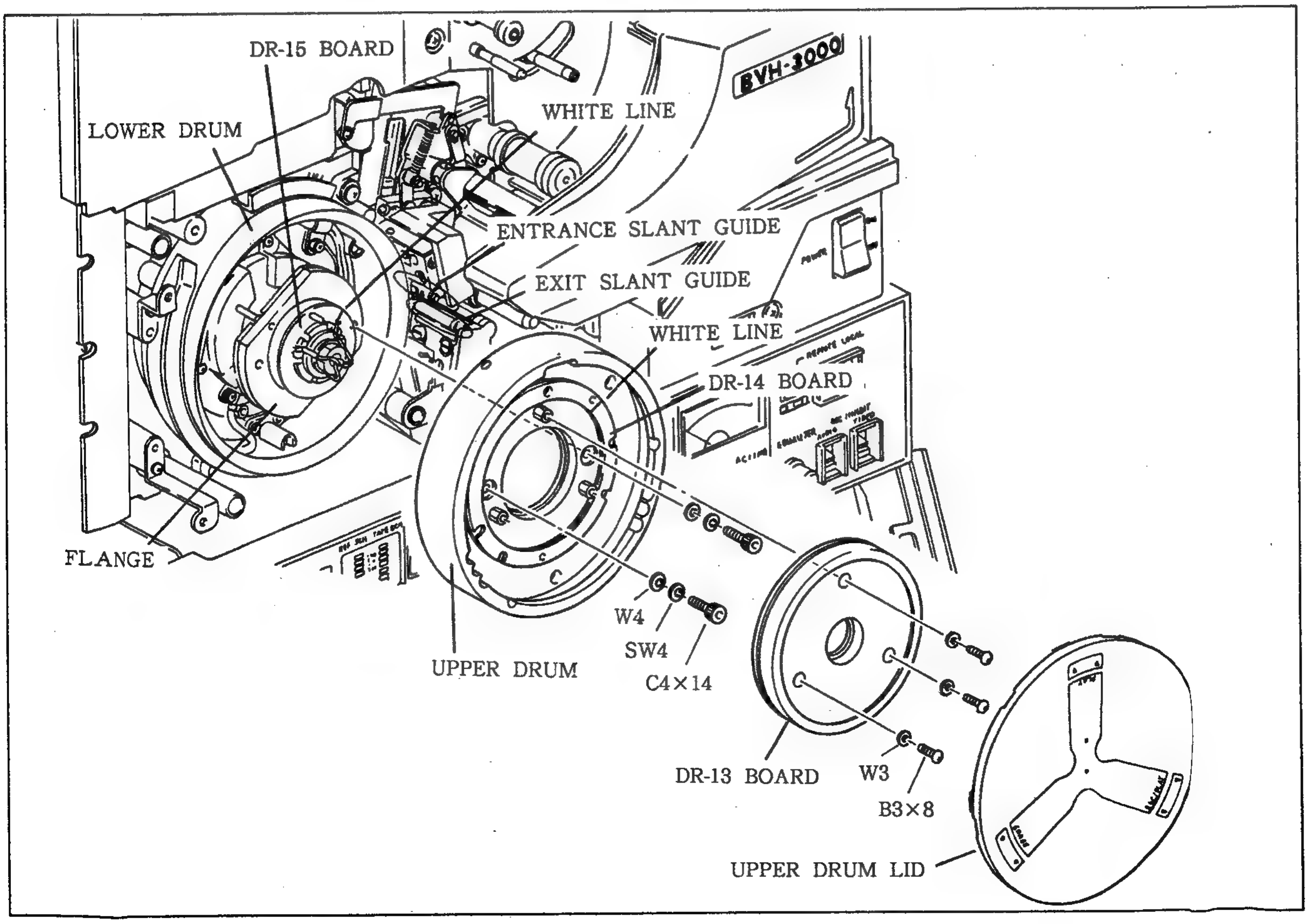


Fig. 6-2-2. Replacement of Upper Drum Assembly

Eccentricity Adjustment

7. Loosen the two screws tighten in step 6 by turning each 1/2 to 1 rotation.
8. Confirm that the dial gauge probe is at the center of the pin inserted in the measurement arm of the upper drum eccentricity adjustment gauge as shown in Fig.6-1. If it is not at the center, readjust the probe position.
9. Turn the zero adjustment screw of the gauge fully counter clockwise.
10. While positioning the gauge stopper shown in Fig. 6-1 so as to contact the bottom side of the lower drum, secure in place by turning the fixing knob at the position shown in Fig.6-3.
11. Turn the dial gauge in the A direction as shown in Fig.6-3, next pull it until it stops in the B direction, then slowly return it toward the drum once again.
12. Turn the zero adjustment screw so that the dial needle indicates zero.
13. After the upper drum has been slowly rotated once counterclockwise, confirm that the swing of the dial needle is within 3 μm. If it exceeds 3 μm, adjust as follows.
   a. Turn the upper drum slowly by hand and stop it at the point where the needle swing is greatest.
   b. With a screwdrive handle or nylon hammer, tap the inside of the upper drum opposite the gauge until the needle swing is about 1/3 of the maximum value as shown in Fig.6-3.
   Note : Always tap the inside of the upper drum.
   c. Slowly turn the upper drum by hand once again and confirm that the needle swing is within 3 μm. If it exceeds 3 μm, stop the upper drum once again at the point where the needle swing is at its maximum position and repeat step b.
   Repeat steps a, b and c until the needle swing is within 3 μm.
14. Alternately tighten the two screws that secure the upper drum so that the drum is firmly positioned. Turn the upper drum slowly by hand and confirm that the dial gauge needle swing is within 3 μm.
15. Turn the gauge zero adjustment screw fully counterclockwise, then remove the gauge.
16. Carefully wipe the contacts of boards DR-13, 14 and 15 with a clean dry cloth.
17. Install the DR-13 board with washer (M3) and three screws (B3×8) so that head name written on the shield cover corresponds to the name of the head on board DR-14.
18. After confirming that the brassy ring of DR-13 board is put in the lower drum flange steadily, tighten the three screws to secure the DR-13 board.

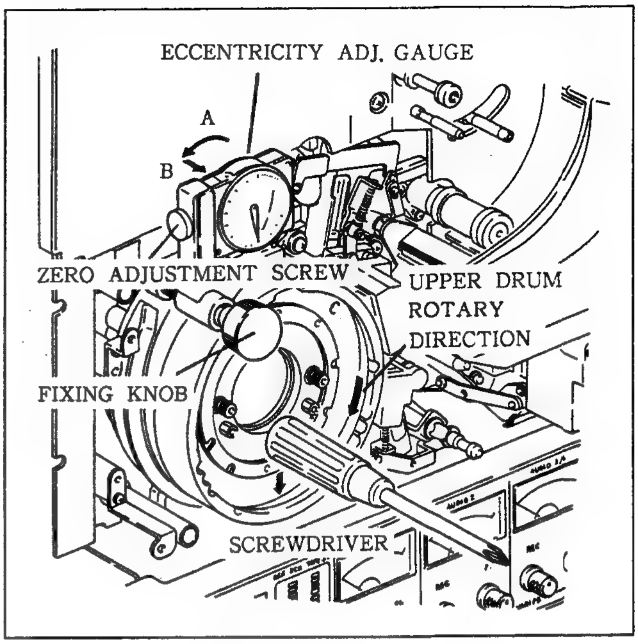


Fig. 6-3. Upper Drum Eccentricity Adjustment

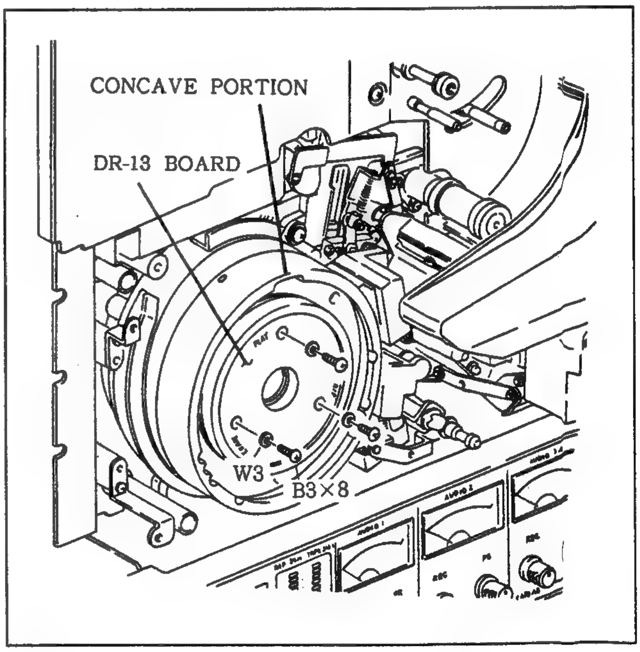
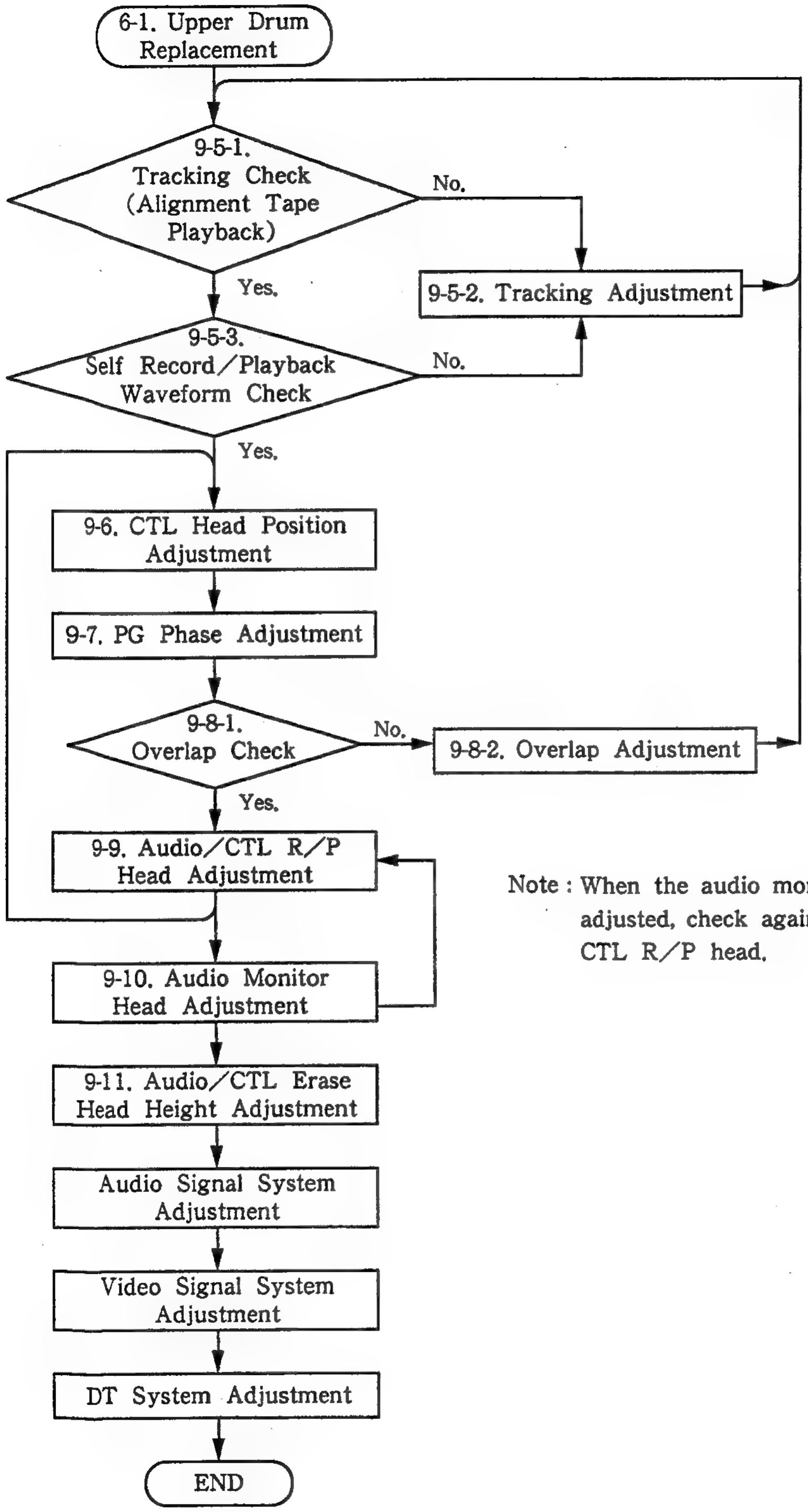


Fig. 6-4. Board Installation

19. Place the lid of the upper drum in correspondence with the head name on board DR-13 : align the convex portion of the upper drum lid with the concave portion of the upper drum (Fig.6-4) and push the lid into the upper drum.
   Note : Make sure that the upper drum lid has been mounted securely.
20. Install the drum panel.

6-1-2. Adjustment After Upper Drum Replacement



Note : When the audio monitor head is adjusted, check again the audio/CTL R/P head.

6-2. HEAD DRUM ASSEMBLY REPLACEMENT

Preliminary Information

A. The head drum assembly must be replaced in the following cases.
   a. Correct RF waveform cannot be obtained regardless of how often the tracking is adjusted because of wear on or damage to the tape guide.
   b. Deterioration of video or audio signal caused by wear on the rotor component bearing cannot be tolerated.

B. After replacing the head assembly, close the movable guide and confirm that the gap between the upper drum and the movable guide is at least 50 μ m before engaging electric current and rotating the upper drum.

C. After B above has been confirmed, the rotary speed when the drum is rotated by the analog speed loop of the drum servo network must be adjusted.

D. Always make sure that the power is turned off when replacing the assembly.

6-2-1. Replacement

Parts removal

1. Remove the stationary head cover, the drum panel and the reel panel.
2. Move to the rear of the machine, remove the two connectors from the CD-36 board, then remove another two connectors from the drum motor.
3. Go to the front of the machine, remove the shield cover from board RP-32 and remove four connectors (two connectors with BVH-3100).
4. Pull out two connectors from the head drum assembly (one connector with BVH-3100).
5. When the slant guides are closed, turn the movable guide drive motor with a flatblade screwdriver (for M4) to open the slant guides.
   Note : Be very careful when turning the motor not to damage the photo interrupter on board MC-29.
6. Loosen slightly the four screws securing the movable guide assembly, push the assembly in the direction opposite to the head drum assembly, and remove the movable guide assembly pin, which has been attached directly to the drum ass'y without any gap.
7. Remove the upper drum lid as shown in Fig.6-2-1 with flatblade screwdriver.
8. Turn the upper drum so that the three holes for screwdriver fit directly over the install screws of the head drum assembly as shown in figure below. While supporting the head assembly steadily, loosen the three install screws with a 3mm hexagonal screwdriver. Finally, pull the assembly directly towards to remove it so it does not hit against guides, etc.

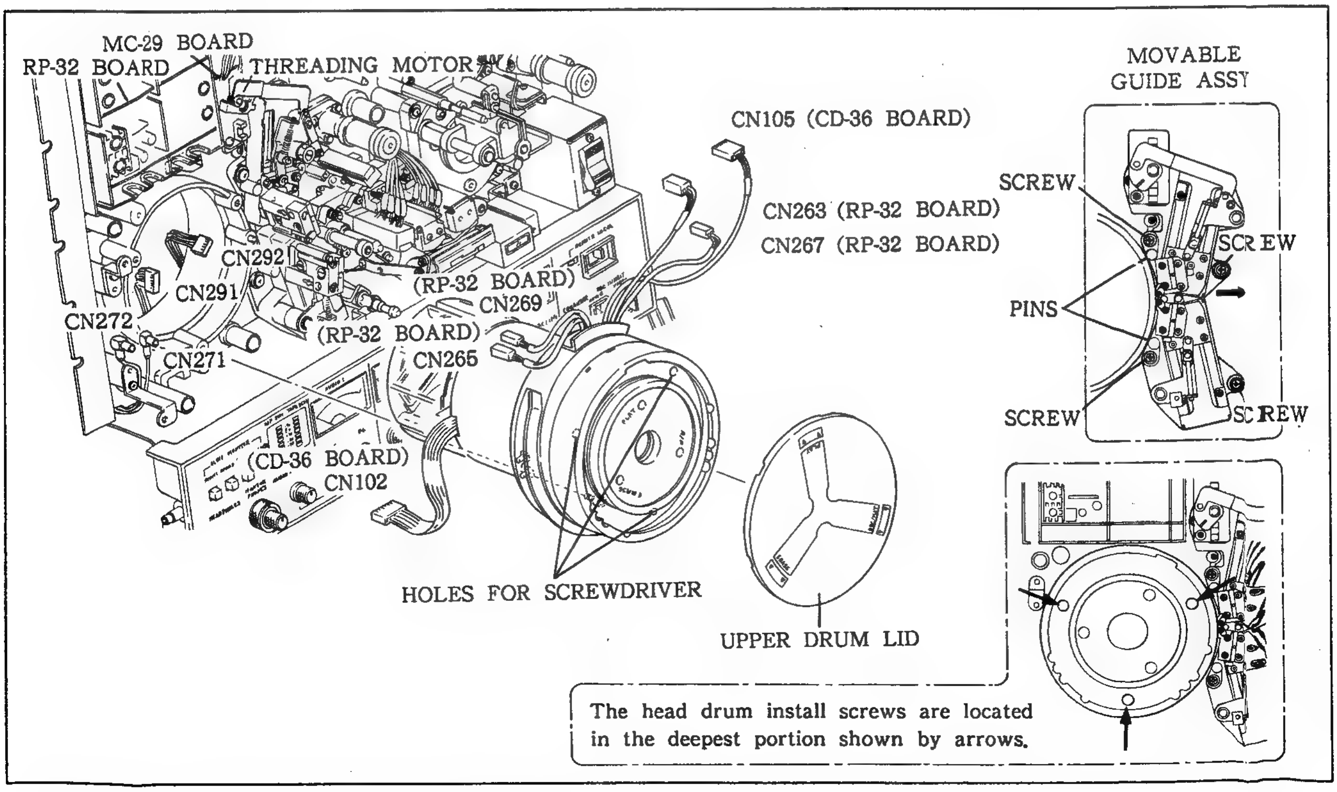


Fig. 6-5. Head Drum Assembly Removal

Cleaning

9. Wipe the following components with a clean cloth soaked in cleaning liquid.
   a. The parts of the entrance and exit slant guides facing the drum.
   b. The upper surface of the boss on which the head drum assembly was installed.
   c. The surface of the new head drum coming in contact with the tape.

   Note : If alcohol was used in the cleaning fluid, wipe the parts with a soft, dry cloth again after cleaning.

Installation

10. Pass the connector CN102 through the hole of the base plate to the rear. Hold the head drum assembly securely as shown in Fig.6-6 so that the hole through which the CN269 harness passes is facing upwards and set the assembly so that the guide hole of the lower drum goes over pin A. Confirm that there is no slack between the lower drum and the upper surface of the base plate installation boss, then align the screwdriver holes of the upper drum to fit over the head drum installation screws. Pass a hexagonal screwdriver through these holes and firmly tighten the screws.

    Note : Be especially careful that the head drum assembly does not hit against the slant guide assembly.
11. Plug in connectors CN263, CN265, CN267 and CN269 in the prescribed locations of the RP-32 board.
12. Plug in connectors CN271 and CN272 to the positions shown in Fig.6-6 : CN272 is not included with BVH-3100.
13. Pass connector CN105 through the hole shown in Fig.6-6 to the rear of the base plate.
14. Go to the rear of the machine and plug in connectors CN102 and CN105 at their specified positions on the CD-36 board.
15. Plug in connectors CN291 and CN292 at their prescribed positions at the rear of the drum.
16. Place the drum lid so that the head name written on the drum lid is directly over the same head name on the board cover inside the upper drum. Arrange so that the concave portion of the upper drum fits the convex portion of the upper drum lid, then push the lid into the upper drum.

    Note : Make sure that the upper drum lid is installed securely.
17. While pushing the movable guide assembly in the direction of both the head drum assembly and the eccentric stopper shown in Fig.6-6, tighten the four screws securely.
18. Confirm that a 30 μm thickness gauge cannot be inserted in the sealed components at the three locations shown in the figure below.

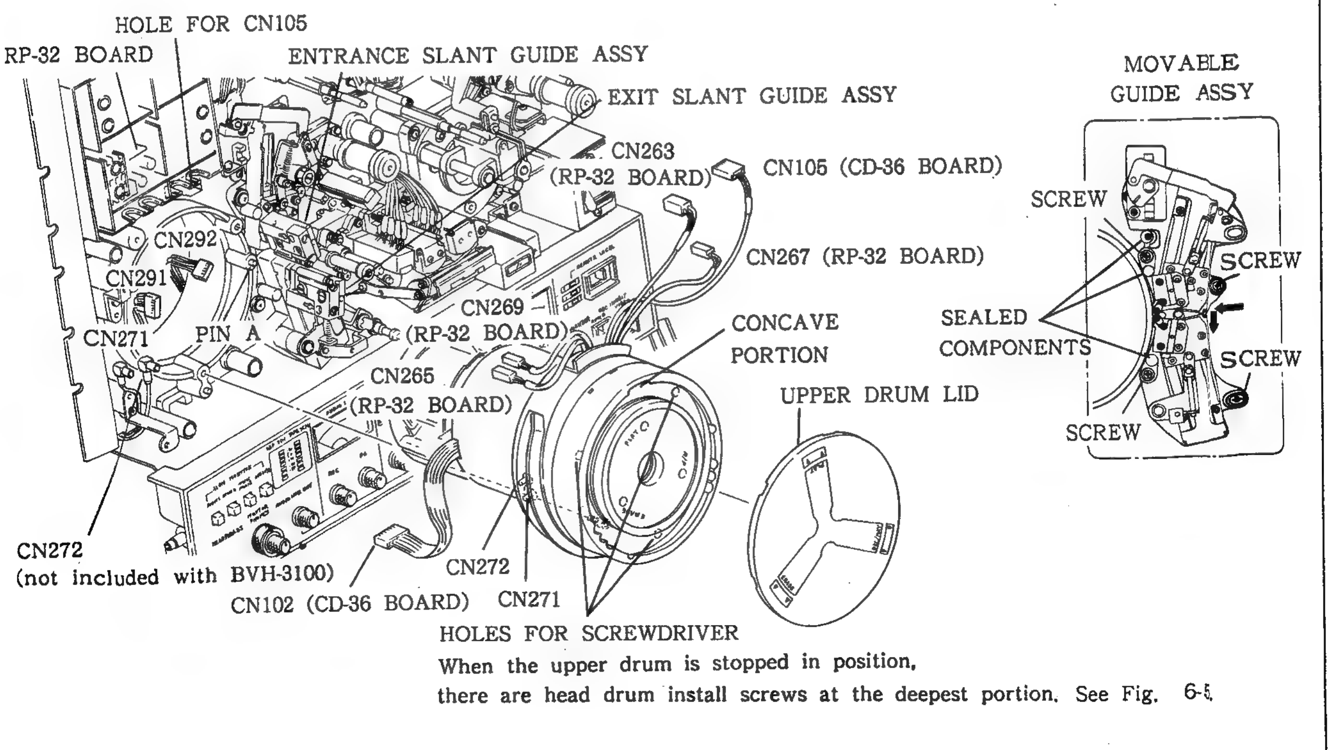


Fig. 6-6. Installation of Head Drum Assembly

Gap Confirmation

19. Insert 50 μ m-thick paper (or video tape folded in two) between the upper drum and movable guide including the guide flanges.
20. Turn the movable guide drive motor with a flat-blade screw driver to close the movable guide.
21. Confirm smooth movement of the paper.

Drum Speed Adjustment

22. While pressing the switch S2 of the SY-103 board, also press key [0] of 21-key section to set the TTP ADJ Mode.
23. Set the machine in STANDBY mode.
24. Key in to [C], [D] of 21-key section (To key in [D], [3] key while pressing blue-colored [OUT] key) and press the [SET] key.
25. While pressing the blue-colored [OUT] key, press the blue-colored [IN] key until the four-digit display with arrow attached in Fig.6-8 becomes 0000±50 (FFB0 to 0050).
26. Confirm that the DR LED on board SV-90 glows.
27. Set the machine in STANDBY OFF mode.
28. While pressing the blue-colored [OUT] of 21-key section, key in [C], [T], [F] and press the [SET] key.
29. Press the [+] key until the display shows "PUSH NVWR SW".
30. Press the NVWR button of SV-90 board.
31. Key in [C], [0] of 21-key section and press [SET] key.

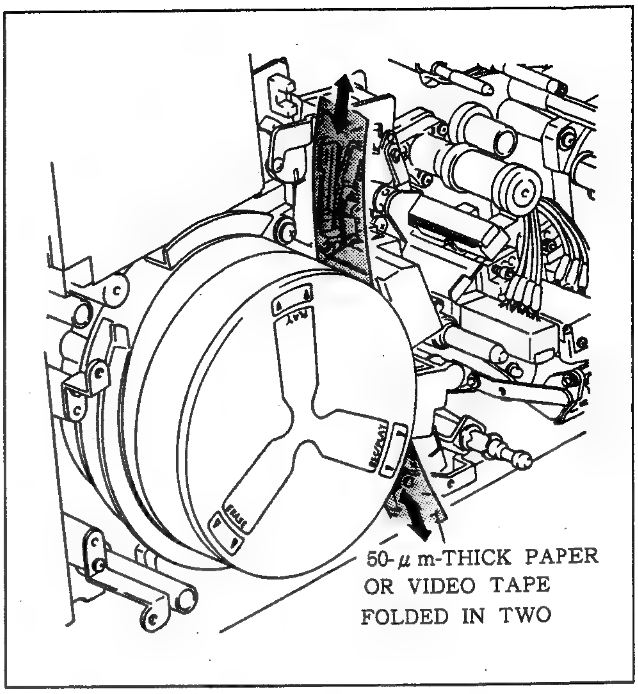
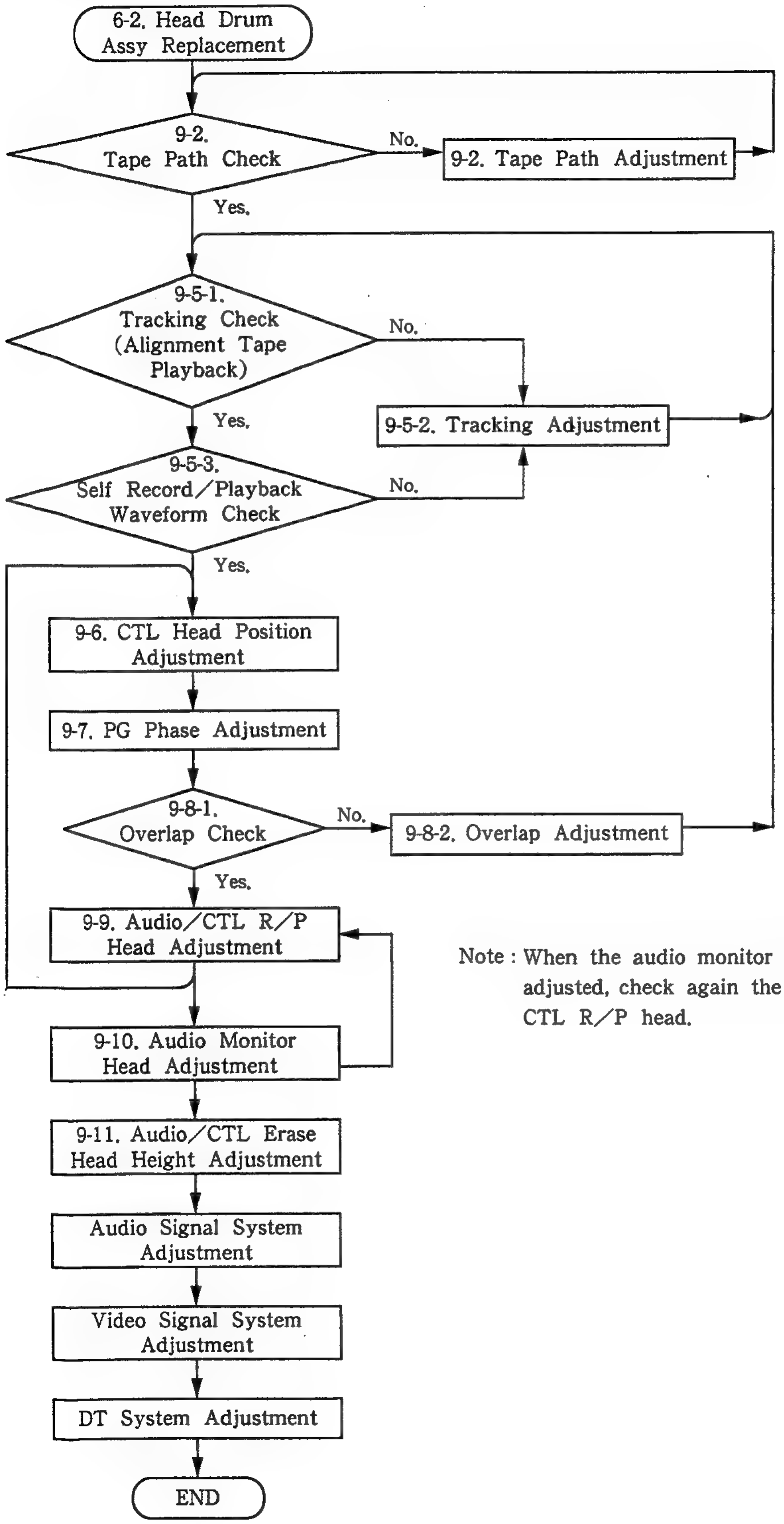


Fig. 6-7. Gap Confirmation

Step	Display Reading	
22		>_
24	>CD_ XXXX 0000 XXXX	>DRM SPEED ADJ_ >_
28	>DRUM SPPED ADJ XXXX 0000 XXXX	>NVW >XXXX XX-XX
29	> XXXX XX-XX XXXX 0000 XXXX	>XXXX XX-XX >PUSH NVWR SW
30	>PUSH NVWR SW_ XXXX 0000 XXXX	>READY_ >_
31	>CO	>TEST MODE OFF >_

Fig. 6-8. Display Readings During Drum Speed Adjustment

6-2-2. Adjustment After Head Drum Replacement



Note : When the audio monitor head is adjusted, check again the audio／CTL R／P head.

6-3. SLIP RING ASSEMBLY REPLACEMENT

Preliminary Information

A. Electrically conductive grease must not be applied to the area where the slip ring and flange make contact.

B. There is no particular need for adjustments after the slip ring assembly has been replaced. However, check that the brushes are placed in the grooves of the slip ring properly.

Parts Removal

1. Disconnect connector CN291 which is connected to the head drum assembly.
2. Loosen sufficiently the three screws which secure the rear cover to the head drum assembly and remove the rear cover.
3. Loosen the screw securing the brush stopper by rotating it through two turns and remove the brush stopper from the pin.
4. Release the lock of the connector on the SR-36 board, and disconnect the SR-35 board.
5. Loosen sufficiently the screws securing the slip ring assembly and remove the assembly while drawing it to the front and taking care that it does not come into contact with the brush stopper.

Parts Mounting

6. Fit the positioning pin on the SL-08 board into the hole on the SL-07 board and then remount the new slip ring assembly using the three screws (PS3×12).

   Note : Take sufficient care to avoid bringing the brush into contact with the brush stopper or screwdriver.
7. Insert the SR-35 board into the connector on the SR-36 board. Then lock the connector.
8. Align the brush stopper with the pin and tighten up the screw securing the brush stopper.
9. Check that the brush has not worked free from the groove in the slip ring.
10. Replace the rear cover and insert connector CN291 into its prescribed positiotn.

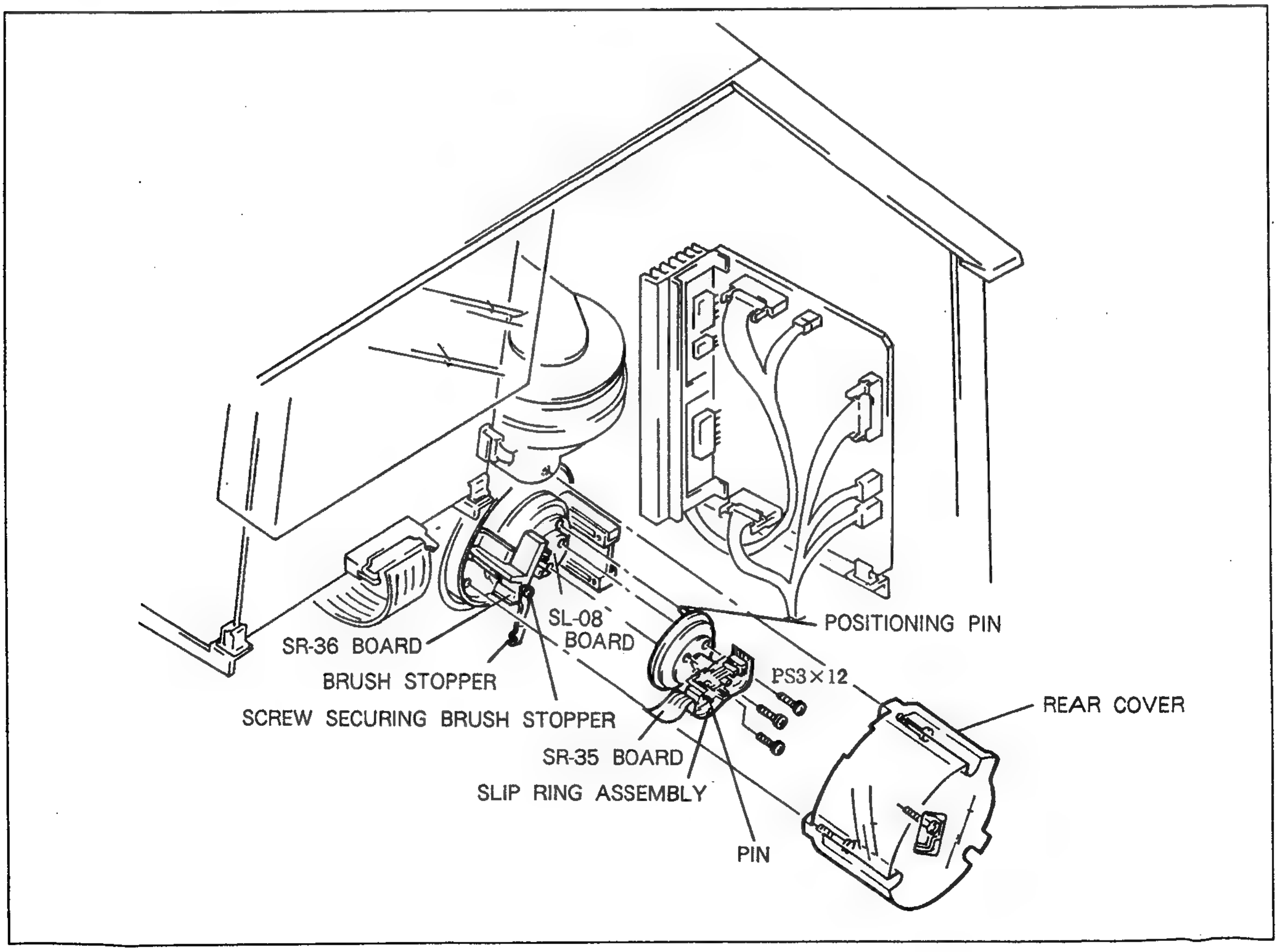


Fig.6-8. Slip Ring Assembly

6-4. SLANT GUIDE ASSEMBLY REPLACEMENT

Preliminary Information

A. If the guide pin of the entrance or exit slant guide has worn, it can be replaced without having to replace the entire assembly.

B. In order to prevent the rotary heads of the upper drum from being damaged and to provide roughly the RF waveform overlap during mounting, the parts should be mounted so that the prescribed clearance will be left between the upper drum and the entrance (or exit) slant guide assembly.

6-4-1. Entrance Slant Guide Assembly Replacement

Parts Removal

1. Switch off the power. When the slant guide is closed, rotate the moving guide drive motor using a flat-blade screwdriver to open the slant guide.
2. Check that the tips of the setscrews ① and ② are come in contact with the entrance slant guide.
3. Remove the two screws used to mount the entrance slant guide assembly and remove the fence from the same assembly.
4. Clean the parts which were hidden by the slant assembly both on the contact surfaces of the lower drum and the mounting surface on the slide base on which the slant guide assembly is mounted.

Parts Mounting

5. Loosen the setscrew ① which is screwed into the boss for adjusting the clearance between the pin and drum by rotating it through one turn.(See Fig.6-10.)
   Note : Do not loosen setscrew ② .
6. Push the entrance slant guide in the both directions of the setscrews ① and ② simultaneously, and yet keep it as far away from the upper drum as possible and secure it loosely using the two screws (C3×10) along with the washers (W3) and spring washers (SW3).
7. Rotate the rotary head of the upper drum and secure it so that it is distanced from the slant guide. Next, rotate the moving guide drive motor using a flat-blade screwdriver to close the slant guide.
   Note : Close the slant guide properly while taking sufficient care so that the guide bracket does not touch the head of the upper drum.
8. First check that there is a clearance between the guide bracket and the upper drum and then tighten up screw A.
   Note : Leave screw B secured loosely.(Thighten the screw B, then loosen it 1/2 to 1 turn.)

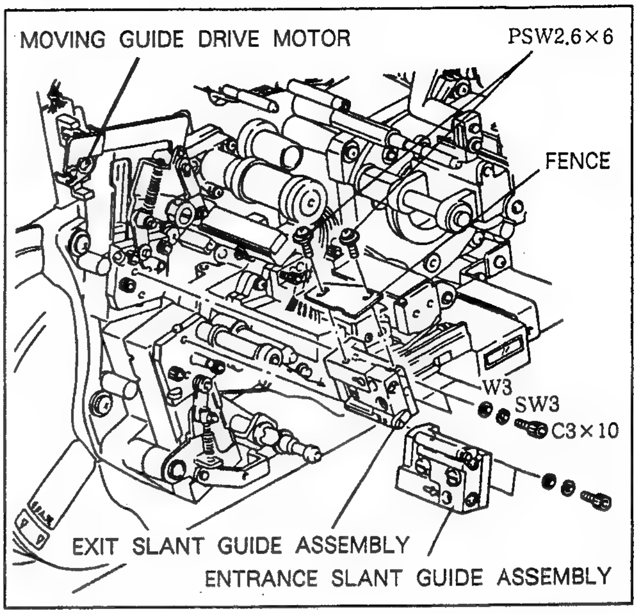


Fig.6-9. Slant Guide Assembly Replacement

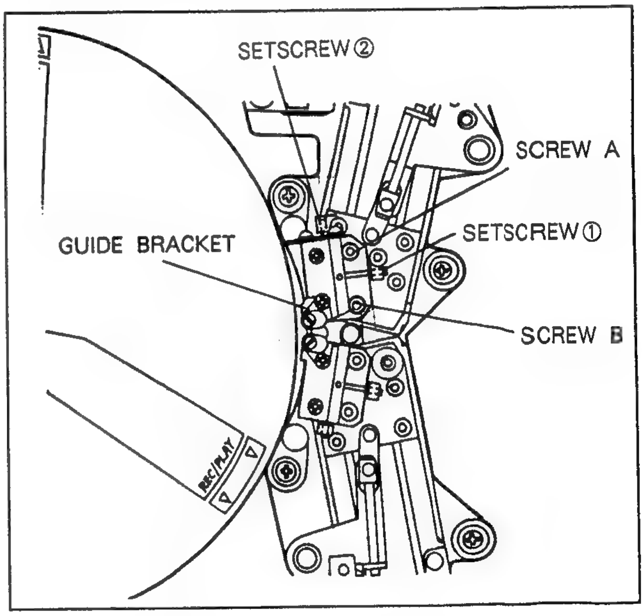


Fig.6-10. Entrance Slant Guide Replacement

9. Now adjust setscrews ① and ② as instructed below so that the clearance between the top of the guide bracket and upper drum is made 0. 1mm. The clearance is measured using a thickness gauge.
   When the clearance is too wide: Adjust the clearance by loosening setscrew ② and by rotating setscrew ① in the clockwise direction.
   When the clearance is too narrow: Adjust the clearance by loosening setscrew ① and by rotating setscrew ② in the clockwise direction.
10. Tighten up screws A and B properly. Check the clearance between the top of the guide bracket and upper drum again. Loosen setscrews ① and ②, force them against the guide block and then apply retaining compound.
11. Replace the fence as instructed below and adjust its position.
   a. As shown by the arrow in Fig.6-11, proceed to push the bottom part of the fence lightly against the cylindrical surface at the bottom part of the lower drum while pushing the fence downward, and secure it loosely using the two screws (PSW2.6×6).
   b. Adjust the clearance between the upper drum and top of the fence to 0.15±0.05mm. Tighten up the two screws which were secured loosely in the above step. And check the clearance between the upper drum and the top of the fence again.
   c. Apply retaining compound to the screws which were tightened up in step b.
12. Open the slant guide, place a 1-inch video tape which has been folded in two between the slant guide (including the guide flange) and the upper drum and close the slant guide. Then check that the tape moves smoothly. Refer to Fig.6-7.

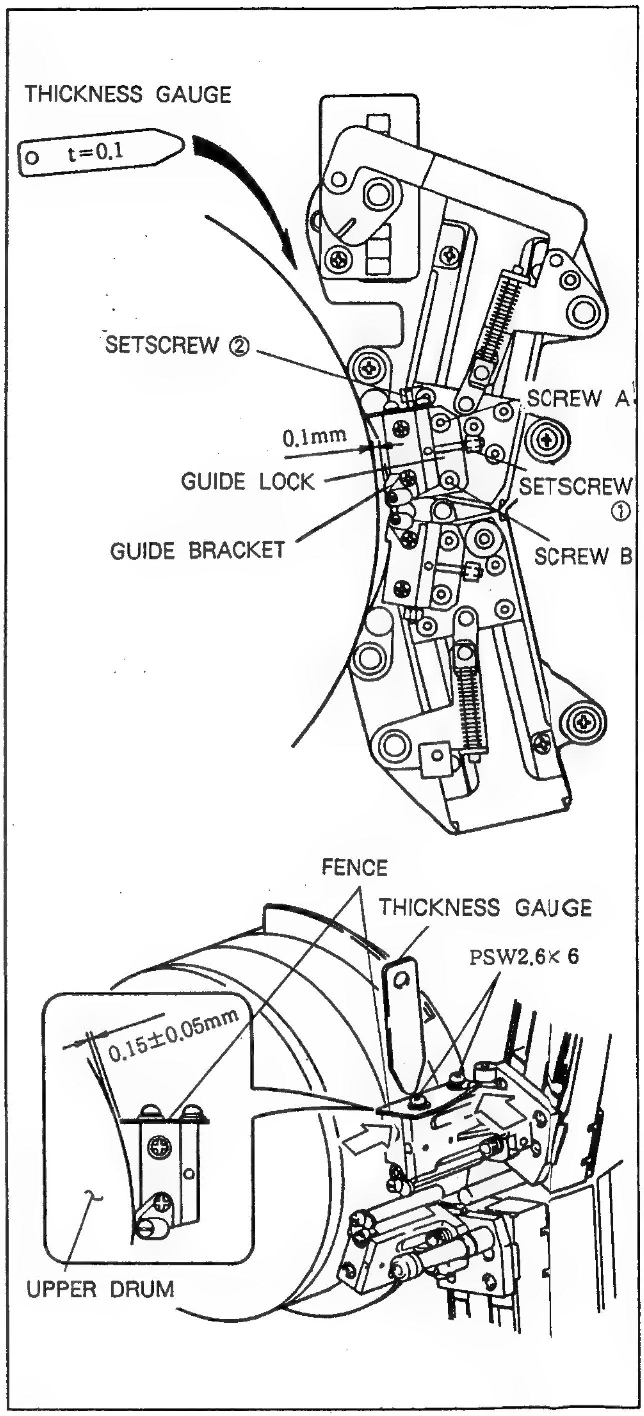


Fig.6-11. Adjustment of Mounting Position of Entrance Slant Guide Assembly

6-4-2. Exit Slant Guide Assembly Replacement

Parts Removal

1. Switch off the power. When the slant guide is closed, rotate the moving guide drive motor using a flat-blade screwdriver to open the slant guide.
2. Check that the tips of the setscrews ③ and ④ are come in contact with the exit slant guide.
3. Remove the two screws used to mount the exit slant guide assembly.
4. Clean the parts which were hidden by the same assembly both on the contact surfaces of the lower drum and the mounting surface on the slide base on which the slant guide assembly is mounted.

Parts Mounting

5. Loosen the setscrew ③ which is screwed into the boss for adjusting the clearance between the pin and drum by rotating it through one turn.
   Note : Do not loosen setscrew ④.
6. Push the exit slant guide in the both directions of the setscrews ③ and ④ simultaneously, and yet keep it as far away from the upper drum as possible and secure it loosely using the two screws (C3×10) along with the washers (W3) and spring washers (SW3).
7. Rotate the rotary head of the upper drum and secure it so that it is distanced from the slant guide. Next, rotate the moving guide drive motor using a flat-blade screwdriver to close the slant guide.
   Note : Close the slant guide properly while taking sufficient care that the guide post does not touch the upper drum.
8. First check that there is a clearance between the guide post and the upper drum and then tighten up screw C.
   Note : Leave screw D secured loosely.(Tighten the screw D, and then loosen it 1/2 to 1 turn.)
9. Now adjust setscrews ③ and ④ as instructed below so that the clearance between the top of the guide post and upper drum is made 0.09mm. The clearance is measured using a thickness gauge.
   When the clearance is too wide : Adjust the clearance by loosening setscrew ④ and by rotating setscrew ③ in the clockwise direction.
   When the clearance is too narrow : Adjust the clearance by loosening setscrew ③ and by rotating setscrew ④ in the clockwise direction.
   Check the clearance again
10. After having adjusted the clearance, tighten up screws C and D properly. Loosen setscrews ③ and ④, force them against the guide block and then apply retaining compound to them.

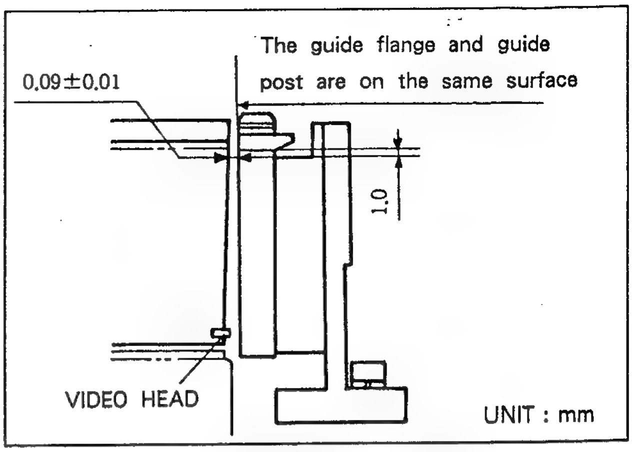
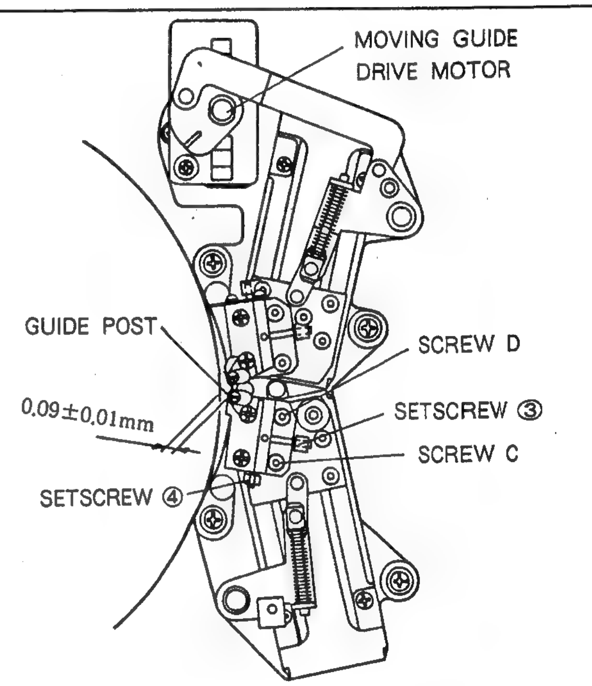


Fig.6-12-1. Position Relationship in Vicinity of Exit Slant Guide Assembly



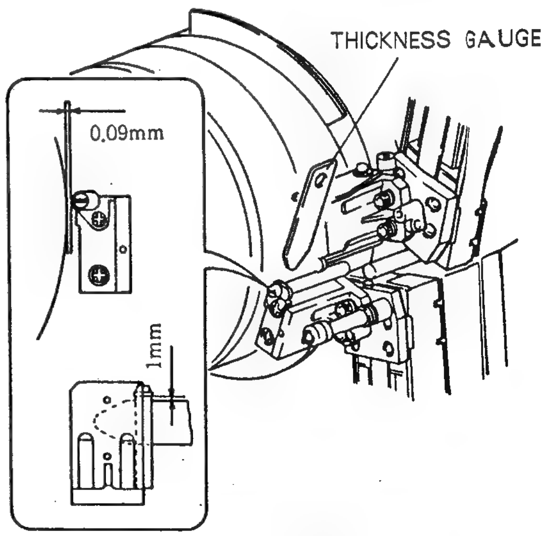
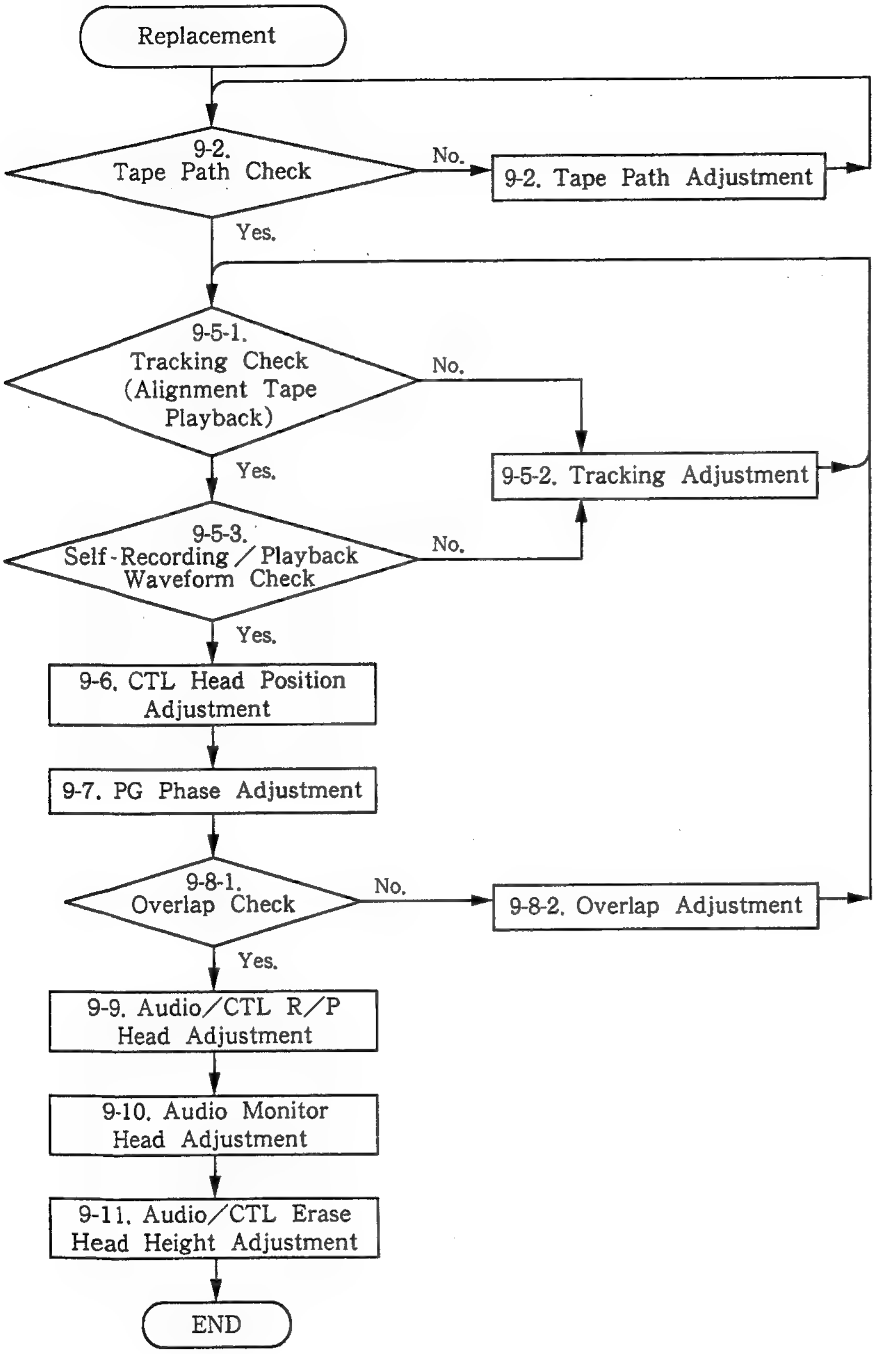


Fig.6-12-2. Adjustment of Mounting Position of Exit Slant Guide Assembly

6-4-3. Adjustments After Slant Guide Assembly Replacement



6-5. REEL MOTOR REPLACEMENT

Preliminary Information

A. The replacement and the adjustments after the replacement are conducted in accordance with the rough summary below.

Parts Removal	The other parts which are removed together with the motor will be used after the motor has been replaced and so these should be cleaned.
↓ Parts Mounting	The positions of the brake band guide and brake solenoid must be adjusted after the motor has been replaced.
↓ Reel Height Adjustment	
↓ Electrical Adjustments	The FG duty cycle and output torque of the reel motor are adjusted.
↓ Brake Torque Adjustment	The mechanical brake torque is adjusted both in the forward and reverse directions.
↓ END	

B. The mechanical brake is activated together with the electromagnetic brake when the power goes off while the tape is still running or when the tape sensor senses that there is no tape. In the test mode, the drive torque of the motor that applies when the motor is operated at a constant speed with the mechanical brake applied is indicated as the mechanical brake torque. This means that the amount of the braking force is in direct proportion to the size of the value displayed.

C. The following equipment should be provided for the adjustments.
- Brake adjustment tool
  Sony Part No. J-6043-720-A
  Application : For adjusting the positions of the brake band guide, flexible solenoid and link stopper.
- Thickness gauge
  Sony Part No. J-6041-670-A
  Application : For adjusting the link stopper position

D. After the reel motor has been replaced, proceed to check the tape transport in accordance with the instructions in Section 9-2-2. When the tape path height has been changed at this time, it is necessary to perform the adjustments subsequent to the tracking check indicated in the flow chart in Section 9-2-1.

6-5-1. Supply Reel Motor Replacement

Parts Removal

1. Switch off the power, remove the front panels and draw out connector CN001 from the DS-19 board.
2. Move to the rear of the machine and open the power supply section. Then disconnect connectors CN203, CN205 and CN207 from the RM-43 board.
3. Loosen the two setscrews ① shown in Fig.6-13, and draw out the reel table while by hand causing the solenoid plunger to be adsorbed.
4. Remove the two E-rings ② and then the brake band.
5. Remove screw ③ and then the brake solenoid assembly.
6. Disengage one end of the two springs mounted between the link stopper and brake link. Then remove the E-ring ④ and the brake link.
7. Remove the three screws ⑤ and then the brake band guide.
8. Remove the three brake band supports ⑥.
9. Remove screw ⑦ which secures the link stopper and then remove the brake support ⑧.
10. Remove the four screws ⑨ and then the supply reel motor.
11. Clean the top surface of the boss on which the motor is mounted and also the parts which have just been removed.

    Note : Take sufficient care not to bend the brake band.

Parts Mounting

12. Pass the three harnesses of the new reel motor to the rear from the holes in the base plate and secure the reel motor using the four screws ⑨ (PSW4×16). Now move to the rear of the machine and connect connectors CN207, CN205 and CN203 to their prescribed positions on the RM-43 board.
13. Secure the link stopper with the brake support ⑧ and then tighten up screw ⑦ (PSW3×6).
14. Mount the three brake band supports ⑥.

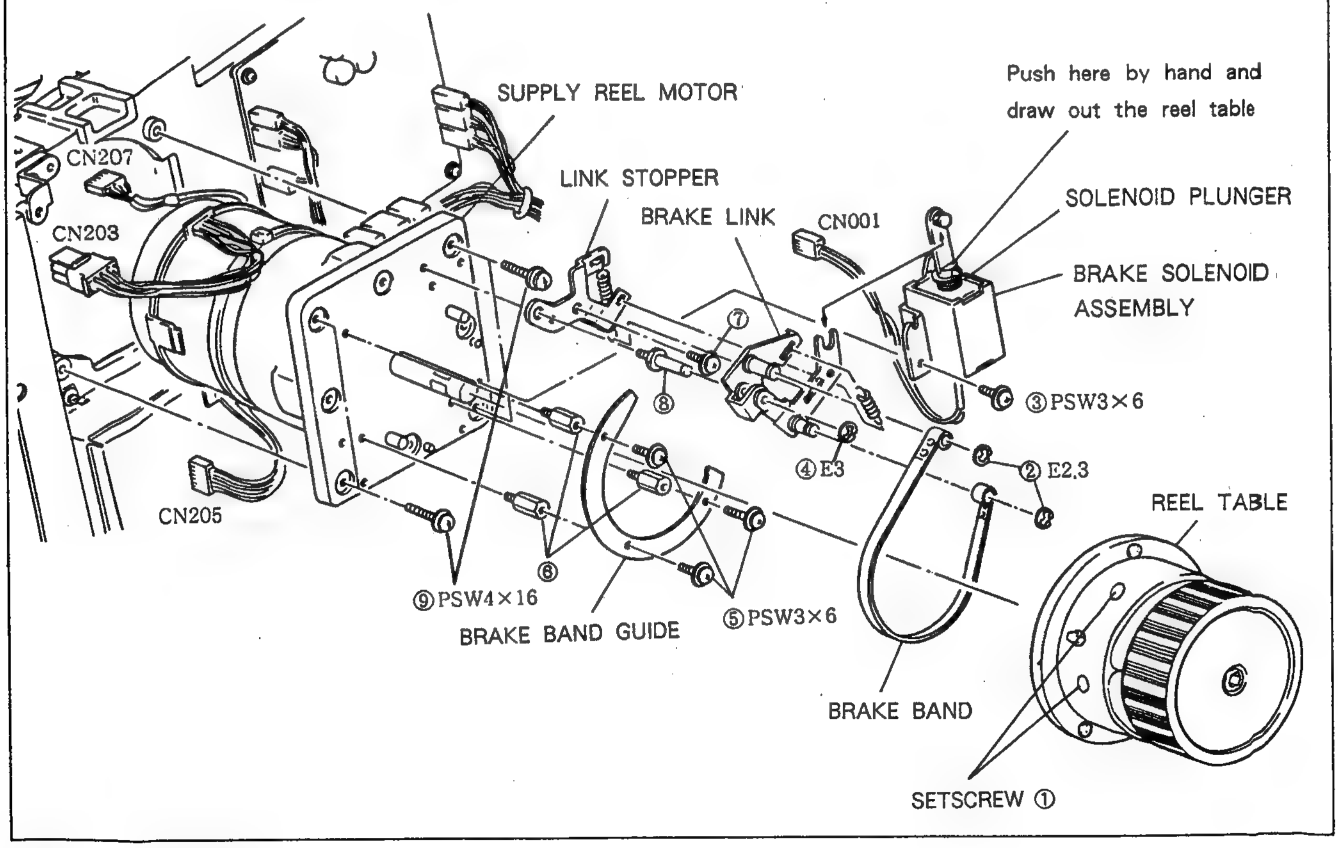


Fig.6-13. Supply Reel Motor Replacement

Brake Band Guide Position Adjustment

15. Turn the side of the brake adjustment tool, which has been provided, that is marked A/JB-372 to the front and, as shown in Fig.6-14, mount the tool onto the reel motor shaft.
16. Secure the brake band guide properly using the three screws (PSW3×6) while pressing the brake band guide lightly against the brake adjustment tool.
17. Remove the brake adjustment tool.

Link Stopper Position Adjustment

18. Arrange the brake links as shown in Fig.6-13, insert them into the brake support and secure it using the E-ring ④ (E3).
19. Attach the spring between the link stopper and brake link.
20. Secure the brake solenoid assembly loosely using screw ③.
21. While causing the solenoid plunger to be adsorbed by hand, turn the side of the brake adjustment tool marked B to the front and attach the tool onto the reel motor shaft.
22. Adjust the position of the link stopper so that the clearance between the link stopper and brake link (top) is set to the value shown in Fig.6-15 without the solenoid plunger being adsorbed.

Brake Solenoid Position Adjustment

23. Cause the solenoid plunger to be adsorbed by hand. Adjust the position of the brake solenoid so that the clearance between the brake adjustment tool and brake band is not less than 0.2mm in the entire Z area range without the brake-bands becoming deformed in the vicinity shown by X and Y in the figure. After the adjustment, tighten up the mounting screws properly and secure the solenoid.
24. Remove the brake adjustment tool while causing the solenoid plunger to be adsorbed by hand.
25. After having cleaned the bottom cylinder area of the reel table (the area with which the brake band comes into contact), cause the solenoid plunger to be adsorbed by hand and mount the reel table onto the motor shaft.
26. While pressing the reel table lightly in the motor direction, tighten up the two setscrews and secure.

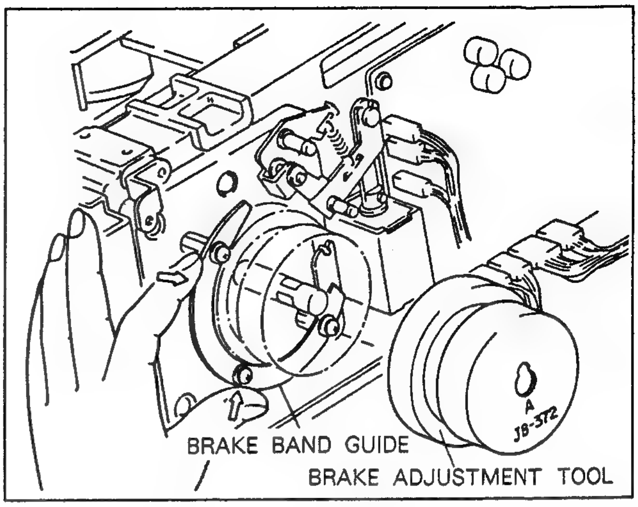


Fig.6-14. Brake Band Guide Position Adjustment

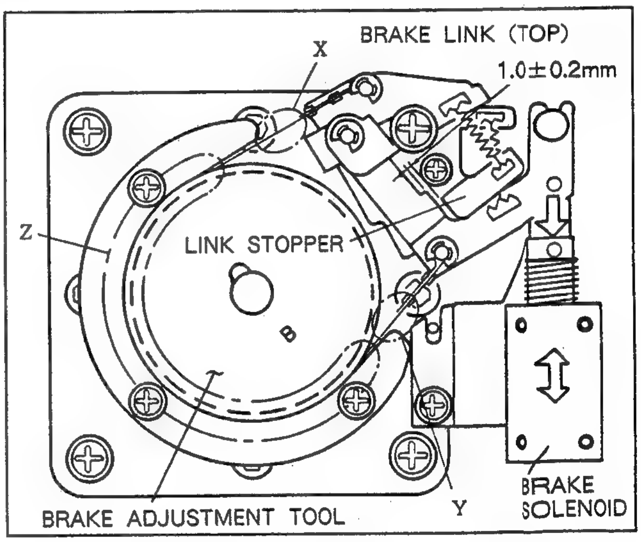


Fig.6-15. Link Stopper/Brake Solenoid Position Adjustment

Reel Table Height Adjustment

27. Load a prerecorded tape which does not have any wrinkles or other such damage. Set the machine to the F.FWD mode and check that the tape does not come into close contact with the reel flange. Conduct the same check for the REW mode. If it does make close contact, adjust it as outlined in the next step. If the tape curls at any location except the reel flange, make the adjustmsent in accordance with the section which details the tape transport adjustments.
28. Proceed to adjust the height in the following sequence.
    a. Remove the tape and then remove the cover while referring to Fig.6-16.
    b. Loosen the two setscrews which secure the reel table and rotate the height adjustment screw.
    Note 1: The height will change by 0.7mm with every turn of the height adjustment screw.
    Note 2: Rotate the height adjustment screw as follows in accordance with the symptom.
    - **Rotate it clockwise when the tape makes contact with the top reel flange.**
    - **Rotate it counterclockwise when the tape makes contact with the bottom reel flange.**

    c. Tighten up the two setscrews while pushing the reel table gently in the motor direction. After having checked again the height of the reel table as in Step 27, reinstall the reel washer and cover.

Adjustment of Supply Reel Motor FG Duty Cycle

29. Adjust the FG duty cycle of the motor by the following procedure.
    a. Press the [0] key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
    b. Press the [F], [9] and [SET] keys in the 21-key section in sequence.
    c. While keeping the blue [OUT] key in the 21-key section depressed, press the blue [IN] key untill the first and last 2 digits (part shown by the arrow in Fig.6-17) of the 4-digit indication at the bottom left of the display enter in D0-DA (hexadecimal notation).
    This operation causes the FG duty cycle to be adjusted to 50%.
    d. Press the [F], [3] and [SET] keys in the 21-key section in sequence so that the reel motor stops.
    e. Press the [C], [T] and [F] keys in sequence while keeping the blue [OUT] key in the 21-key section depressed.
    f. Press the [SET] key and then press the [+] key until "PUSH NVWR SW" appears on the display.
    g. Press the NVWR button on the SV-90 board.
    h. Press the RESET switch S3 on the SV-90 board.

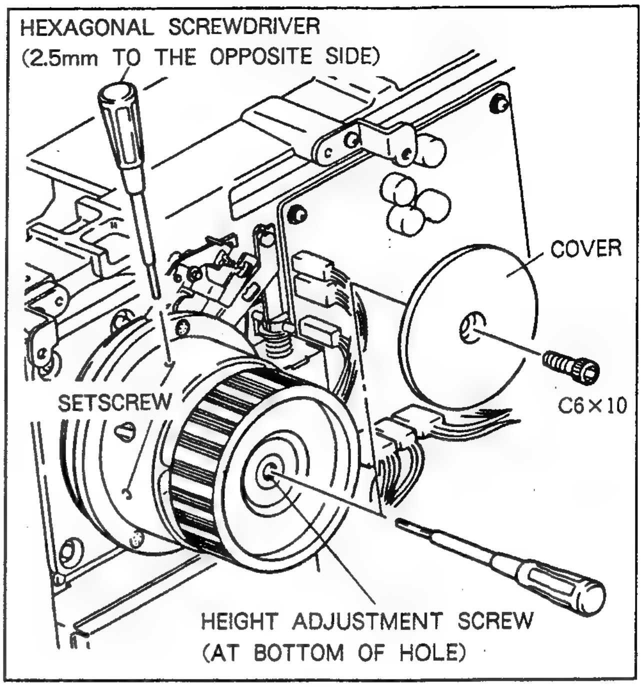


Fig.6-16. Supply Reel Table Height Adjustment

Step	Display Reading
29-a	>_
29-b	>F9 SFG ADJ_ abcd XXXX XXXX>_
29-e	>NVW
29-f	>PUSH NVWR SW
29-g	>PUSH NVWR SW_>READY_ >_

Fig.6-17. Adjustment of Supply Reel Motor FG Duty Cycle

(Operation will now be returned to the ordinary operation mode.)

Supply Reel Motor Torque Adjustment

30. Adjust the drive torque of the reel motor according to the following sequence.
    a. Press the $\boxed{0}$ key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
    b. Press the $\boxed{T}$, $\boxed{0}$ and $\boxed{SET}$ keys in the 21-key section in sequence.
    c. Check that the supply reel automatically turns in the forward and reverse directions and stops.
    d. After the motor has stopped running, check that the 2 digits (area indicated by the black arrow in Fig.6-18) are within 63-65 (hexadecimal notation). If they are not, proceed to adjust as follows.
    e. Press the $\boxed{T}$, $\boxed{1}$ and $\boxed{SET}$ keys in the 21-key section in sequence.
    f. Check that the supply reel automatically turns in the forward and reverse directions and stops.
    g. After the motor has stopped running, check that the 2 digits (area indicated by the white arrow in Fig.6-18) are within 63-65 (hexadecimal notation). If they are not, repeat the adjustment starting with step e.
    h. Press the $\boxed{C}$, $\boxed{T}$ and $\boxed{F}$ keys while keeping the blue $\boxed{OUT}$ key in the 21-key section depressed.
    i. Press the $\boxed{SET}$ key and then press the $\boxed{+}$ key until "PUSH NVWR SW" appears on the display.
    j. Press the NVWR button on the SV-90 board.
    k. Press the RESET switch S3 on the SV-90 board. (Operation will now be returned to the ordinary operation mode.)

Step	Display Reading
30-a	>_
30-b	>TO 0 START >XX XX XX XX ab >XX XX XX XX
30-d	>XX XX XX XX ab >XX >_
30-e	>T1 ADJ & START>XX XX XX XX ab >XX XX XX XX
30-g	>XX XX XX XX ab >XX >_
30-h	>NVW
30-i	>PUSH NVWR SW
30-j	>PUSH NVWR SW_>READY_ >_

Fig.6-18. Supply Reel Motor Torque Adjustment

Mechanical Brake Torque Adjustment

31. Adjust the mechanical brake torque as follows.
  a. Press the $\boxed{0}$ key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
  b. Press the $\boxed{T}$, $\boxed{3}$ and $\boxed{SET}$ keys in the 21-key section in sequence.
  c. After the reel has automatically stopped, check that the "ab" indication on the display (first 2 digits of area indicated by the black arrow in Fig.6-19) is within 1E-2D and that the "ef" indication on the display (first 2 digits of area indicated by the white arrow in Fig.6-19) is 05. If the ratings are not satisfied, conduct the following check ; if they are satisfied, proceed to step f.
  d. **If the "ab" indication does not satisfy the rating:** Change the position at which the adjustment spring (FWD/CCW) shown in Fig.6-20 is attached.
  If the "ef" indication does not satisfy the rating: Change the position at which the adjustment spring (REV/CW) shown in Fig.6-20 is attached.
  e. Repeat steps b through d until the ratings are satisfied.
  f. Press the RESET switch S3 on the SV-90 board. (Operation will now be returned to the ordinary operation mode.)

Step	Display Reading
31-a	>_
31-b	>T3 BRK CHECK> abcd efgh >XX XX XX XX

Fig.6-19. Brake Torque Adjustment

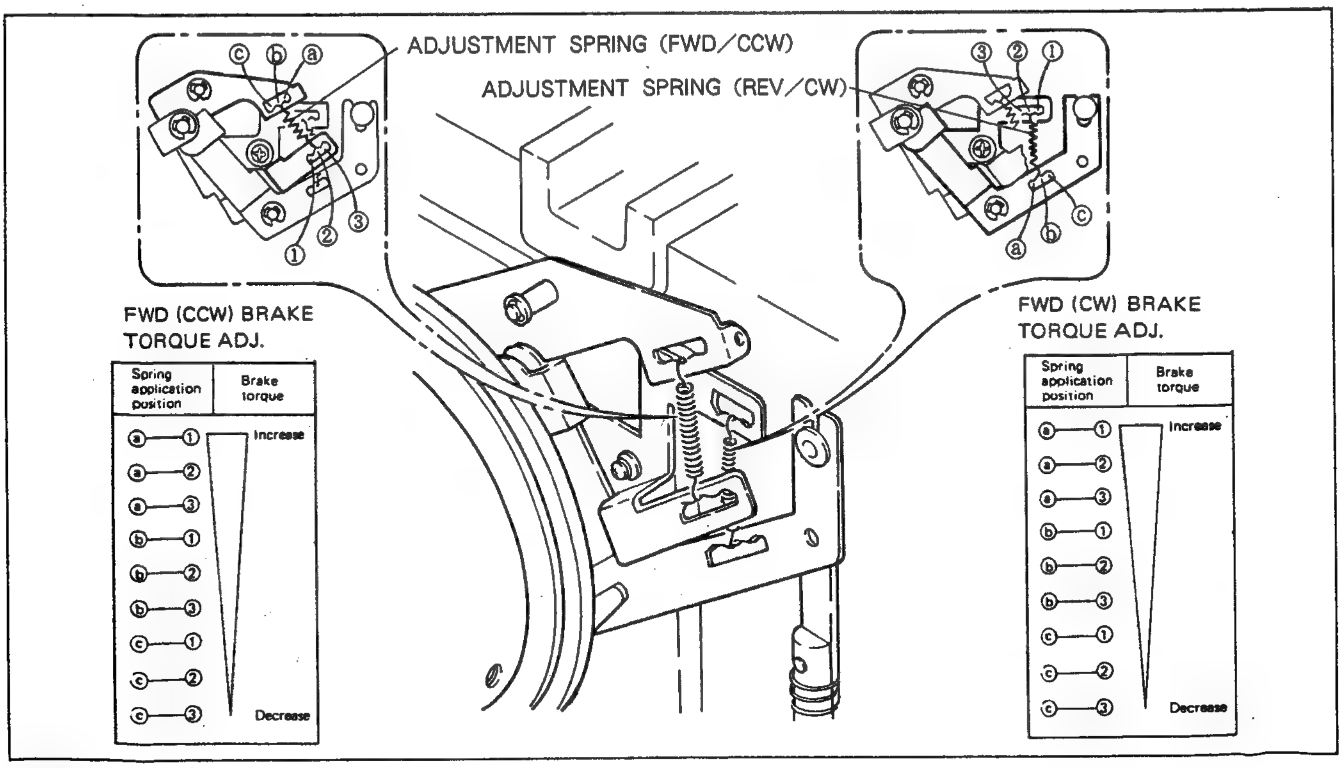


Fig.6-20. Supply Reel Brake Torque Adjustment

6-5-2. Take-up Reel Motor Replacement

Parts Removal

1. Switch off the power, remove the front panels. Next, draw out connector CN009 from the DS-19 board.
2. Move to the rear of the machine and open the power supply section. Then disconnect connectors CN201, CN204 and CN206 from the RM-43 board.
3. Loosen the two setscrews ① shown in Fig.6-21, and draw out the reel table while causing the solenoid plunger to be adsorbed by hand.
4. Remove the two E-rings ② and then the brake band.
5. Remove screw ③ and then the brake solenoid assembly.
6. Remove one end of the two springs mounted between the link stopper and brake link. Then remove the E-ring ④ and the brake link.
7. Remove the three screws ⑤ and then the brake band guide.
8. Remove the three brake band supports ⑥.
9. Remove screw ⑦ which secures the link stopper and then the brake support ⑧.
10. Remove the four screws ⑨ and then remove the take-up reel motor.
11. Clean the top surface of the boss on which the motor is mounted and also the parts which have just been removed.

    Note : Take sufficient care not to bend the brake band.

Parts Mounting

12. Pass the three harnesses of the new reel motor to the rear from the holes in the base plate and secure the reel motor using the four screws ⑨ (PSW4×16). Now move to the rear of the machine and connect connectors CN206, CN204 and CN201 to their prescribed positions on the RM-43 board.
13. Secure the link stopper with the brake support ⑧ and then tighten up screw ⑦ (PSW3×6).
14. Mount the three brake band supports ⑥.

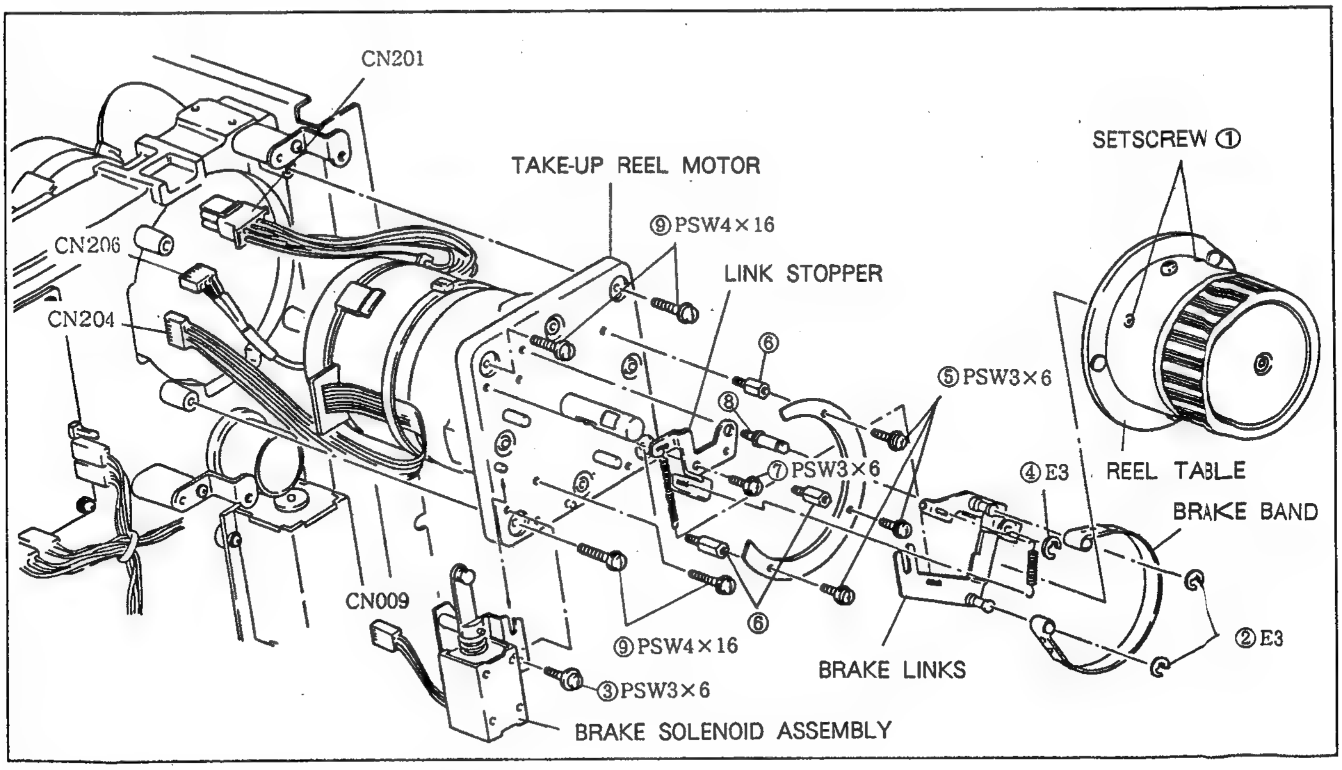


Fig.6-21. Take-up Reel Motor Replacement

Brake Band Guide Position Adjustment

15. Turn the side of the brake adjustment tool, which has been provided, that is marked A/JB-372 to the front and, as shown in Fig.6-22, mount the tool onto the reel motor shaft.
16. Secure the brake band guide properly using the three screws (PSW3×6) while pressing the brake band guide lightly against the brake adjustment tool.
17. Remove the brake adjustment tool.

Link Stopper Position Adjustment

18. Arrange the brake links as shown in Fig.6-21, insert them into the brake support and secure them using the E-ring (E3).
19. Attach the spring between the link stopper and brake link.
20. Secure the brake solenoid assembly loosely using the screw ③.
21. While causing the solenoid plunger to be adsorbed by hand, turn the side of the brake adjustment tool marked B to the front and attach the tool onto the reel motor shaft.
22. Adjust the position of the link stopper so that the clearance between the link stopper and brake link (top) is set to the value shown in Fig.6-23 without the solenoid plunger being adsorbed.

Brake Solenoid Position Adjustment

23. Adsorb the solenoid plunger by hand. Adjust the position of the brake solenoid so that the clearance between the brake adjustment tool and brake band is not less than 0.2mm in the entire Z area range without the brake bands becoming deformed in the vicinity shown by X and Y in Fig.6-23. After the adjustment tighten up the screws which secure the solenoid properly.
24. Remove the brake adjustment tool while causing the solenoid plunger to be adsorbed by hand.
25. After having cleaned the bottom cylinder area of the reel table (the area with which the brake band comes into contact), cause the solenoid plunger to be adsorbed by hand and mount the reel table onto the motor shaft.
26. While pressing the reel table lightly in the motor direction, tighten up the two setscrews and secure.

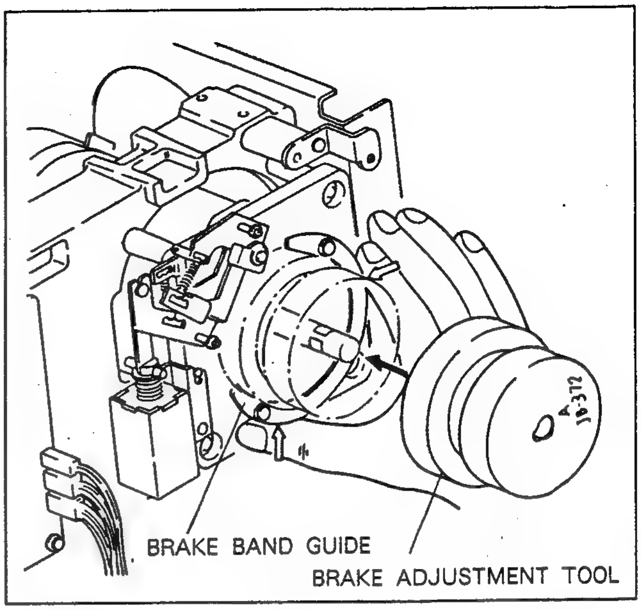


Fig.6-22. Brake Band Guide Position Adjustment

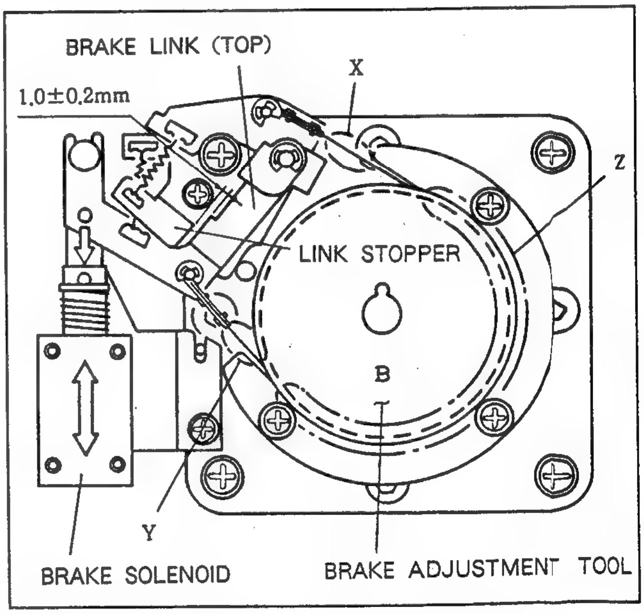


Fig.6-23. Link Stopper/Brake Solenoid Position Adjustment

Reel Table Height Adjustment

27. Thread a recorded tape which does not have any wrinkles or other such damage. Set the machine to the F.FWD mode and check that the tape does not come into close contact with the reel flange. Conduct the same check for the REW mode. If it does make close contact, adjust it as outlined in the next step. If the tape curls at any location except the reel flange, make the adjustment in accordance with the section which details the tape transport adjustments.
28. Proceed to adjust the height in the following sequence.
  a. Remove the tape and then remove the cover while referring to Fig.6-24.
  b. Loosen the two setscrews which secure the reel table and rotate the height adjustment screw shown in Fig.6-24.
  Note 1 : The height will change by 0.7mm with every turn of the adjustment screw.
  Note 2 : Rotate the adjustment screw as follows in accordance with the symptom.
  - **Rotate it clockwise when the tape makes contact with the top reel flange.**
  - **Rotate it counterclockwise when the tape makes contact with the bottom reel flange.**

  c. Tighten up the two setscrews while pushing the reel table gently in the motor direction. After having checked again the height of the reel table as in Step 27, reinstall the cover.

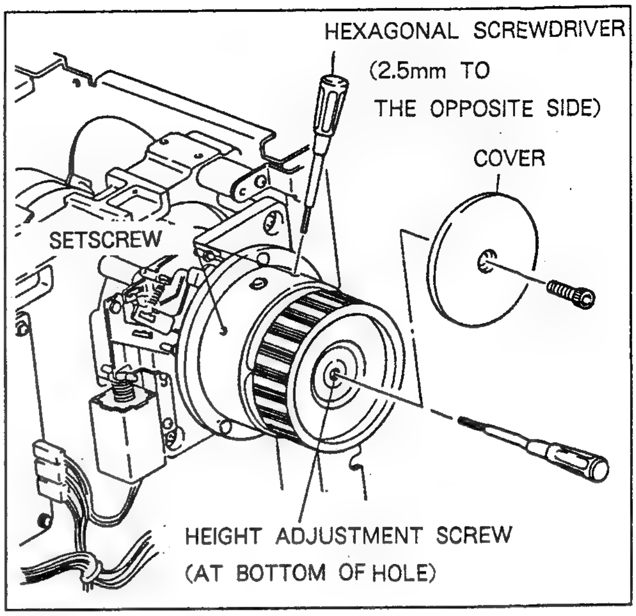


Fig.6-24. Take-up Reel Table Height Adjustment

Adjustment of Supply Reel Motor FG Duty Cycle

29. Adjust the FG duty cycle of the motor by the following procedure.
  a. Press the [0] key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
  b. Press the [F], [A](press the [0] key while keeping the blue [OUT] key depressed for [A] key) and [SET] keys in the 21-key section in sequence.
  c. While keeping the blue [OUT] key in the 21-key section depressed, press the blue [IN] key untill the first and last 2 digits (part shown by the arrow in Fig.6-25) of the 4-digit indication at the bottom left of the display have entered in D0-DA (hexadecimal notation).
  This operation causes the FG duty cycle to be adjusted to 50%.
  d. Press the [F], [3] and [SET] keys in the 21-key section in sequence so that the reel motor stops.
  e. Press the [C], [T] and [F] keys in sequence while keeping the blue [OUT] key in the 21-key section depressed.
  f. Press the [SET] key and then press the [+] key until "PUSH NVWR SW" appears on the display.
  g. Press the NVWR button on the SV-90 board.
  h. Press the RESET switch S3 on the SV-90 board.

Step	Display Reading
29-a	>_
29-b	>FA TFG ADJ_ $\underbrace{\text{abcd}}$ XXXX XXXX>_
29-e	>NVW
29-f	>PUSH NVWR SW
29-g	>PUSH NVWR SW_>READY_ >_

Fig.6-25. Adjustment of Take-up Reel Motor FG Duty Cycle

(Operation will now be returned to the ordinary operation mode.)

Take-up Reel Motor Torque Adjustment

30. Adjust the drive torque of the reel motor according to the following sequence.
    - a. Press the $\boxed{0}$ key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
    - b. Press the $\boxed{T}$, $\boxed{8}$ and $\boxed{SET}$ keys in the 21-key section in sequence.
    - c. Check that the take-up reel automatically turns in the forward and reverse directions and stops.
    - d. After the motor has stopped running, check that the 2 digits (area indicated by the black arrow in Fig.6-26) are within 63-65 (hexadecimal notation). If they are not, perform steps e to g.
    - e. Press the $\boxed{T}$, $\boxed{9}$ and $\boxed{SET}$ keys in the 21-key section in sequence.
    - f. Check that the take-up reel automatically turns in the forward and reverse directions and stops.
    - g. After the motor has stopped running, check that the 2 digits (area indicated by the white arrow in Fig.6-26) are within 63 to 65 (hexadecimal notation). If they are not, repeat the adjustment starting with step e.
    - h. Press the $\boxed{C}$, $\boxed{T}$ and $\boxed{F}$ keys while keeping the blue $\boxed{OUT}$ key in the 21-key section depressed.
    - i. Press the $\boxed{SET}$ key and then press the $\boxed{+}$ key until "PUSH NVWR SW" appears on the display.
    - j. Press the NVWR button on the SV-90 board.
    - k. Press the RESET switch S3 on the SV-90 board. (Operation will now be returned to the ordinary operation mode.)

Step	Display Reading
30-a	>_
30-b	>T8 0 START >XX XX XX XX ab >XX XX XX XX
30-d	>XX XX XX XX ab >XX >_
30-e	>T9 ADJ & START>XX XX XX XX ab >XX XX XX XX
30-g	>XX XX XX XX ab >XX >_
30-h	>NVW
30-i	>PUSH NVWR SW
30-j	>PUSH NVWR SW_>READY_ >_

Fig.6-26. Take-up Reel Motor Torque Adjustment

Mechanical Brake Torque Adjustment

31. Adjust the mechanical brake torque as follows.
    a. Press the [0] key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
    b. Press the [T], [B](press the [1] key while keeping the blue [OUT] key depressed for [B] key) and [SET] keys in the 21-key section in sequence.
    c. After the reel has automatically stopped, check that the "ab" indication on the display (first 2 digits of area indicated by the black arrow in Fig.6-27) is within 05 and that the "ef" indication on the display (first 2 digits of area indicated by the white arrow in Fig.6-19) is 1E-2D. If the ratings are not satisfied, conduct the following check ; if they are satisfied, proceed to step f.
    d. **If the "ab" indication does not satisfy the rating:** Change the position at which the adjustment spring (FWD/CCW) shown in Fig.6-28 is attached.
    If the "ef" indication does not satisfy the rating: Change the position at which the adjustment spring (REV/CW) shown in Fig.6-28 is attached.
    e. Repeat steps b through d until the ratings are satisfied.
    f. Press the RESET switch S3 on the SV-90 board. (Operation will now be returned to the ordinary operation mode.)

Step	Display Reading
31-a	>_
31-b	>TB BRK CHECK>abcd efgh >XX XX XX

Fig.6-27. Brake Torque Adjustment

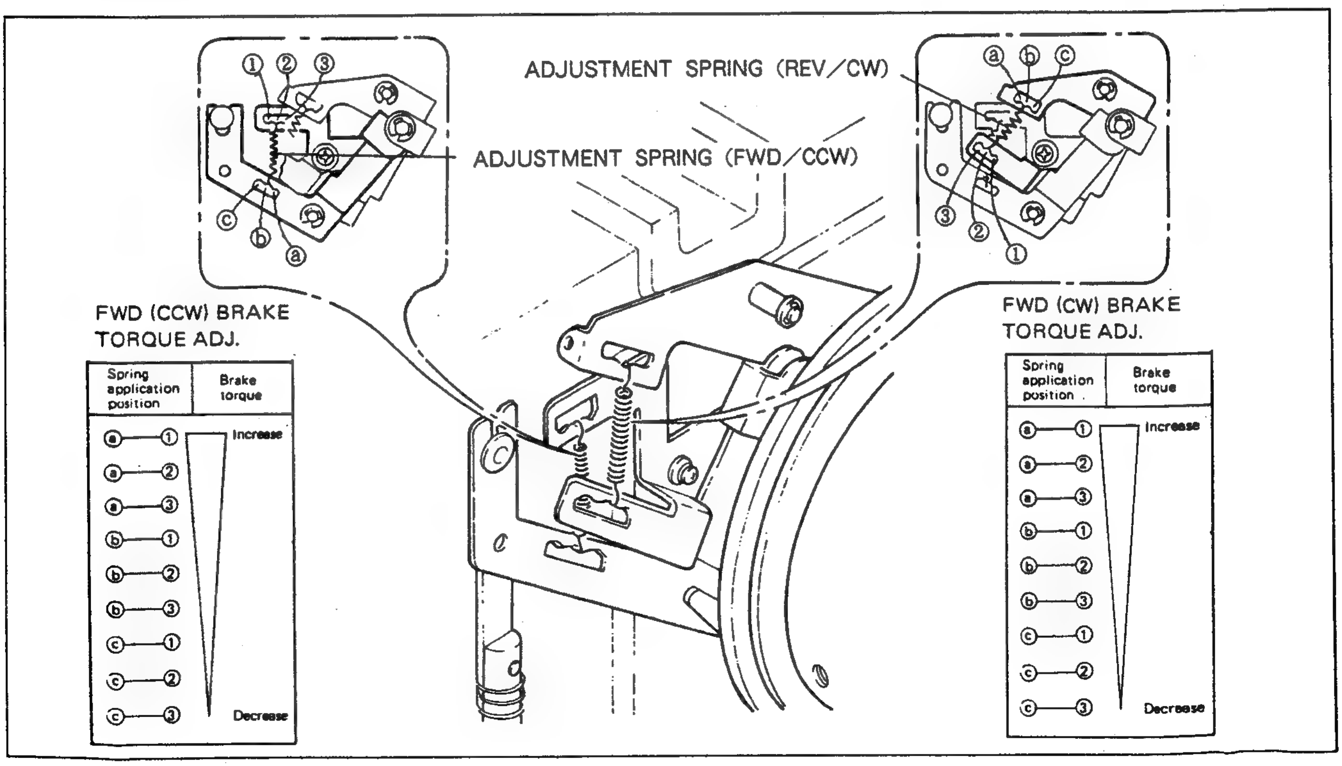


Fig.6-28. Take-up Reel Brake Torque Adjustment

6-6. BRAKE BAND REPLACEMENT

Preliminary Information

A. The mechanical brake functions when the power is OFF and when no tape has been threaded. It therefore follows that if this brake is properly adjusted, the reels can be stopped without any tape damage even if the power is turned off by accident while the tape is running.

B. The mechanical brake needs to be replaced when its torque cannot be adjusted no matter how the position where the adjustment spring is attached is changed.

C. The brake band replacement and the adjustments after the replacement are outlined briefly below.

Parts Removal
↓
Parts Mounting
↓
Mechanical Brake Torque Adjustment
↓
Reel Table Height Check
↓
END

Parts Removal

1. Loosen the two setscrews shown in the figure. Remove the reel table while causing the solenoid plunger to be adsorbed. Clean the area where contact was made with the brake band at the bottom cylindrical area of the reel table.
2. Remove the two E-rings and remove the brake band.

Parts Mounting

3. Mount the new brake band in the position shown in the figure and secure it using the two E-rings (E2.3).
4. Turn the surface marked B on the brake adjustment tool in front, as shown in the figure, while causing the solenoid plunger to be adsorbed and insert the tool onto the reel motor shaft.
5. Check that the clearance between the link stopper and brake link (top) is 1.0mm±0.2mm without causing the solenoid plunger to be adsorbed. If the clearance does not satisfy this value, adjust the position of the link stopper.
6. Remove the brake adjustment tool while causing the solenoid plunger to be adsorbed and mount the reel table instead. Secure the reel table by tightening up the two setscrews while pushing it lightly in the motor direction.

This illustration shows the supply side as the example but replacement is conducted in exactly the same way for the take-up side.

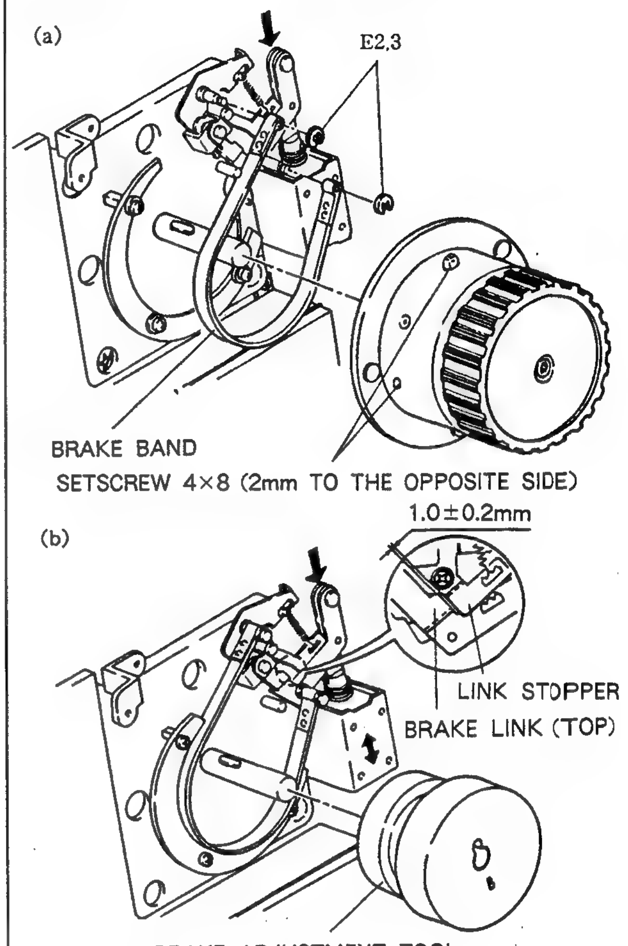


Fig.6-29. Brake Band Replacement

Mechanical Brake Torque Adjustment

7. Adjust the brake torque following step 31 in Section 6-4-1 for the supply side and step 31 in Section 6-4-2 for the take-up side.

Reel Table Height Check

8. Thread a recorded tape which does not have any wrinkles or any other such damage. Set the machine to the F.FWD mode and check that the tape does not come into close contact with the reel flange. Conduct the same check for the REW mode. If it does make close contact, adjust it in accordance with the instructions in the tape transport adjustment section.

6-7. BRAKE SOLENOID REPLACEMENT

Preliminary Information

The brake solenoid is replaced as follows.

Parts Removal
↓
Parts Mounting
↓
Solenoid Assembly Position Adjustment
↓
Mechanical Brake Torque Adjustment — S side : Section 6-5-1 step 31; T side : Section 6-5-2 step 31
↓
Reel Table Height Check — S side : Section 6-5-1 step 27,28; T side : Section 6-5-2 step 27,28
↓
END

Parts Removal

1. Loosen the two setscrews which secure the reel table. Draw out the reel table while causing the solenoid plunger to be adsorbed.
2. As in Fig.6-30, remove the screw (PSW3×6) and remove the brake solenoid assembly.
3. Disassemble the brake solenoid assembly while referring to the diagram.

Parts Mounting

4. Replace the new solenoid and re-assemble. Mount it so that the bracket can be moved lightly.
5. As shown in Fig.6-31, first adjust so that the clearance between one end of the bracket's long hole and the solenoid pin is 5.0mm±0.5mm. Then secure the bracket firmly.
6. Secure the solenoid assembly to the position shown in Fig.6-30 using a screw (PSW3×6).

Solenoid Assembly Position Adjustment

7. Turn the surface marked B on the brake adjustment tool in front while causing the solenoid plunger to be adsorbed by hand and insert the tool onto the reel motor shaft.

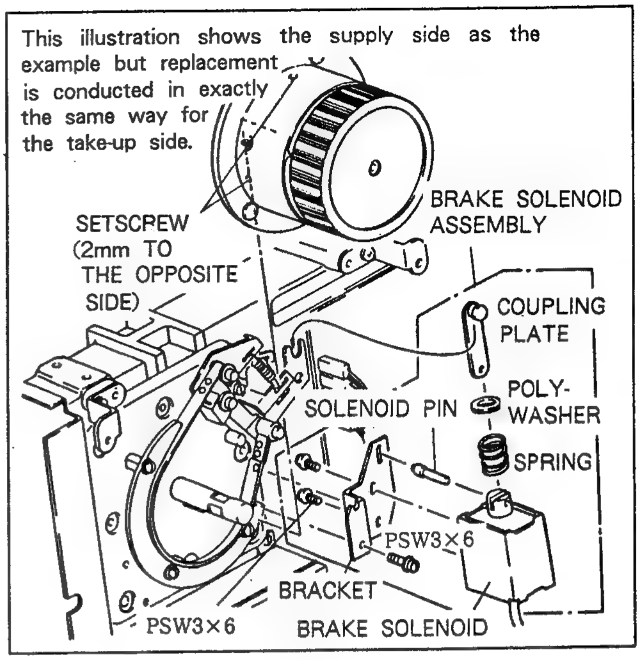


Fig.6-30. Brake Solenoid Replacement

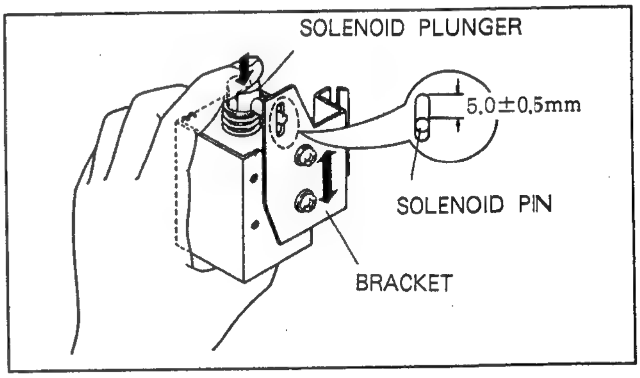


Fig.6-31. Bracket Mounting Position Adjustment

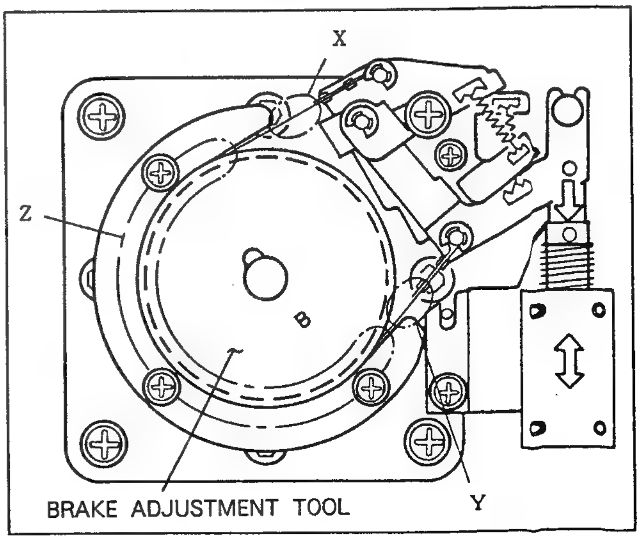


Fig.6-32. Solenoid Assembly Position Adjustment

8. While causing the solenoid plunger to be adsorbed by hand, adjust the position of the brake solenoid so that the clearance between the brake adjustment tool and brake band is not less than 0.2mm in the entire Z area range without the brake band becoming deformed in the vicinity shown by X and Y in Fig.6-32. After the adjustment tighten up the mounting screw properly and secure the solenoid.
9. Remove the brake adjustment tool while causing the solenoid plunger to be adsorbed by hand and mount the reel table instead.
10. Secure the reel table by tightening the two setscrews while pushing it in the motor direction.
11. Adjust the mechanical brake and reel table height in accordance with the instructions in the preliminary Information.

6-8. TENSION ARM ASSEMBLY REPLACEMENT

Preliminary Information

A. The tension arm assembly needs to be replaced when the tape tension cannot be adjusted properly. When a worn guide shaft is to blame, however, either replace the shaft only or rotate the worn area to a position where it will not make contact with the tape and re-use it.

B. The tension spring used with the tension arm assembly has a great effect on the tape tension. The hook area should not be bent and the spring should be replaced only with the specified part.

C. Take care not to apply any force to the board, which is mounted on the tension arm assembly, that it is not designed to withstand.

D. Provide the following equipment for the tape tension adjustment.
- Tension adjustment tool
  Sony Part No. J-6251-960-A
- Digital voltmeter

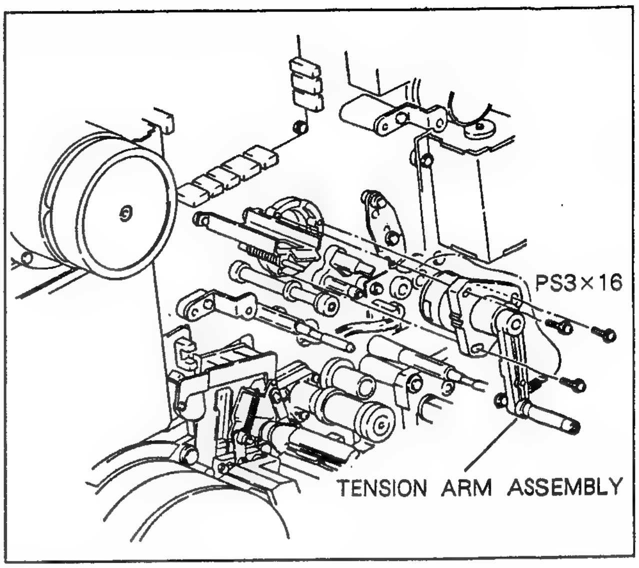


Fig.6-33. Tension Arm Assembly Replacement

Replacement

1. Disconnect connector CN003 from the DS-19 board.
2. Remove the spring from the spring holder.
3. Remove the three screws (PS3×16) shown in the figure and then remove the tension arm assembly. Next mount the new tension arm assembly in its place, and apply the spring to the spring holder.

Adjustment

4. Adjust the tape tension as in Section 9-2.

6-9. CAPSTAN MOTOR REPLACEMENT

Preliminary Information

A. The capstan motor is replaced as follows.

Parts Removal
↓
Parts Mounting
↓
Pinch Roller Pressure Adjustment
↓
Motor FG Duty Cycle Adjustment
↓
Motor Speed Adjustment
↓
Tape Path Adjustment
↓
END

B. Provide the following equipment in order to adjust the pressure of the pinch roller.
- Tension scale with a full scale of 5kg Sony Part No. J-6041-640-A
- Provide a piece of string with a length of 20cm.

C. Depending on the stretching direction, the value indicated on the tension scale will differ slightly. Before proceeding with the measurement, therefore, point the tension scale in the stretching direction beforehand and adjust the zero point on the scale.

Parts Removal

1. Move to the rear of the machine and open the power supply section. Then disconnect connectors CN107 and CN108 from the capstan motor.
2. Remove the two screws, PS4×10 and PS3×8, which secure the ES mount.
3. Remove the E-ring and then remove the pinch roller assembly and poly-washer.
4. Remove the pinch roller support.
5. Remove the four screws PSW4×16 and remove the capstan motor.

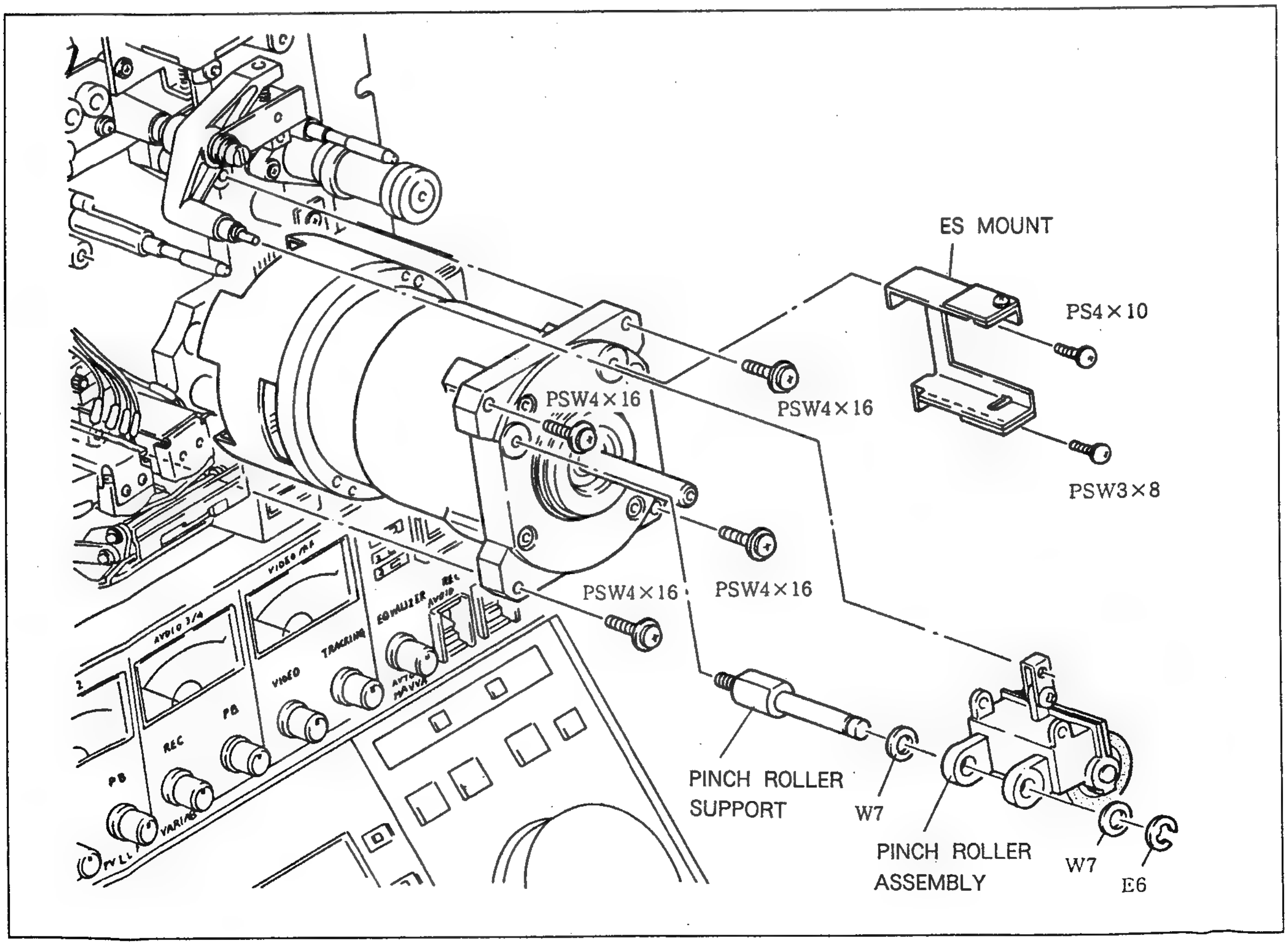


Fig.6-34. Capstan Motor Replacement

Parts Mounting

6. Secure the new capstan motor using the four screws (PSW4×16).
7. Re-assemble the parts by proceeding in reverse from step 6 through 1.

Pinch Roller Pressure Adjustment

8. Press the [0] key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
9. Press the [F], [0] and [SET] keys in the 21-key section in sequence.
   This causes the following to appear on the display;

>FO	>PINCH

10. Press the [7] key while pressing the blue [OUT] key in the 21-key section.
    (This causes the pinch roller to be pressed onto the capstan.)
11. Attach the 5kg tension scale to the pinch roller arm, as shown in Fig.6-35. Stretch the tension scale in the direction which connects the pinch roller and capstan, as shown by the arrow in detail figure "a" and wait until the pinch roller moves free from the capstan and the pinch roller stops rotating. Return the tension scale in the capstan direction and check that the value indicated on the scale is between 3.7 and 4.0kg when the pinch roller starts to rotate again. If this value is not satisfied, adjust as follows.
12. Turn the adjustment screw in accordance with the symptom, as shown in detail figure "b."
13. With the pinch roller pressed into position, check that the clearance between the pinch lever and stopper is 0.3±0.1mm, as shown in detail figure "b." If this value is not satisfied, adjust the stopper position. Then apply retaining compound to the threaded section of the adjustment screw.
14. Press the [8] key while pressing the blue [OUT] key in the 21-key section.
    (This causes the pinch roller to move away.)
15. Press the [F], [3] and [SET] keys in the 21-key section in sequence.
    (This causes the capstan to stop rotating.)
16. Press the RESET switch S3 on the SV-90 board.
    (Operation will now be returned to the ordinary operation mode.)

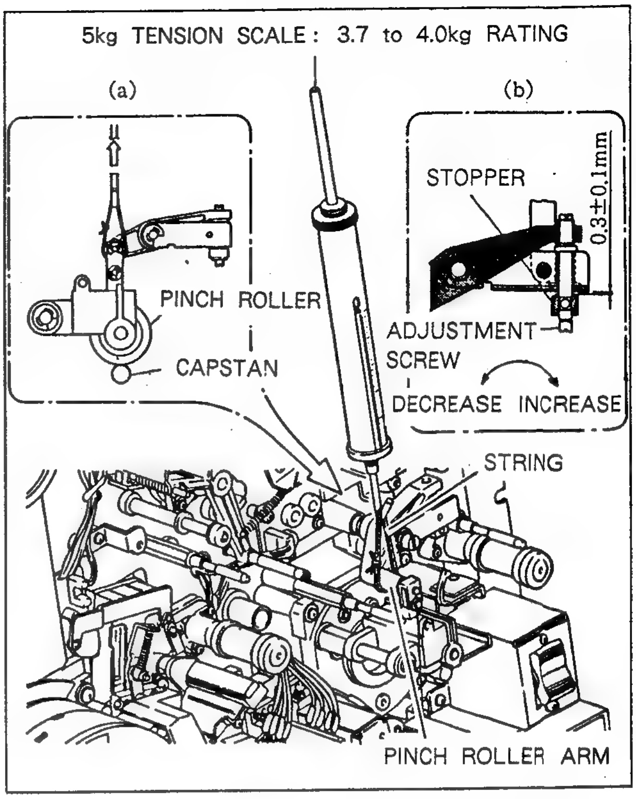


Fig.6-35. Pinch Roller Pressure Adjustment

Motor FG Duty Cycle Adjustment

17. Press the [0] key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
18. Press the [F], [8] and [SET] keys in the 21-key section in sequence.
19. While keeping the blue [OUT] key in the 21-key section depressed, press the blue [IN] key untill the first and last 2 digits (part shown by the arrow in Fig.6-36) of the 4-digit indication at the bottom left of the display enter in D0-DA.
20. Press the [F], [3] and [SET] keys in the 21-key section in sequence.
    (This causes the capstan motor to stop.)
21. Press the [C], [T] and [F] keys in sequence while pressing the blue [OUT] key in the 21-key section.
22. Press the [SET] key and then press the [+] key until "PUSH NVWR SW" appears on the display.
23. Press the NVWR button on the SV-90 board.
24. Press the RESET switch S3 on the SV-90 board. (Operation will now be returned to the ordinary operation mode.)

Motor Speed Adjustment

25. Set the REC INHIBIT switches on the meter panel to ON.
26. Press the [0] key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
27. Play back the alignment tape.
28. Press the [C], [C], [0] and [SET] keys in sequence in the 21-key section.
29. Keep pressing the blue [IN] key while pressing the blue [OUT] key in the 21-key section until the 4-digit "abcd" display (part shown by the arrow in Fig.6-37) at the bottom left of the display enters 0FA0±5 (0F9B to 0FA5).
30. Set the machine to the standby off mode.
31. Press the [C], [T] and [F] keys in sequence while pressing the blue [OUT] key in the 21-key section.
32. Press the [SET] key and then press the [+] key until "PUSH NVWR SW" appears on the display.
33. Press the NVWR button on the SV-90 board.
34. Press the [C], [0] and [SET] keys in sequence in the 21-key section.
35. Press the [SET] key while pressing the blue [OUT] key in the 21-key section.
    (Operation will now be returned to the ordinary operation mode.)

Step	Display Reading
17	>_
18	>F8 CFG ADJ abcd XXXX XXXX>
21	>NVW
22	>PUSH NVWR SW
23	>PUSH NVWR SW_>READY_ >_

Fig.6-36. Motor FG Duty Cycle Adjustment

Step	Display Reading
28	>CC0 >CAP SPEED ADJ abcd XXXX XXXX>
31	>NVW
32	>PUSH NVWR SW
33	>PUSH NVWR SW_>READY_ >_

Fig.6-37. Motor Speed Adjustment

6-10. PINCH ROLLER REPLACEMENT

Preliminary Information

A. Provide the following for the adjustments and checks.
  - Tension scale (5kg) Sony Part No. J-6041-640-A

Replacement

1. Remove the E-ring shown in the figure and then remove the pinch roller assembly.
2. Loosen sufficiently the two setscrews which secure the pinch roller shaft and remove the pinch roller from the pinch roller assembly.
3. Replace the pinch roller with a new unit and re-mount the part by following the above steps 2 and 1 in the reverse order.

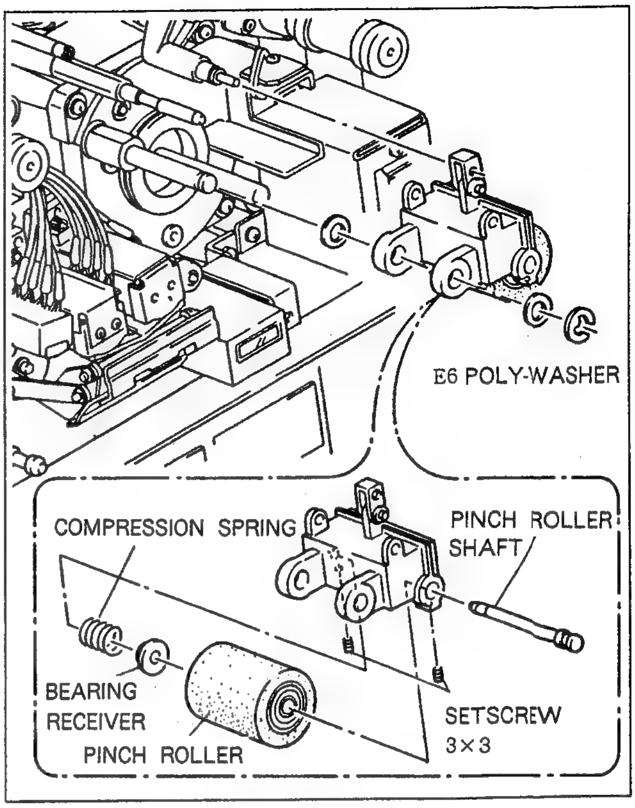


Fig.6-38. Pinch Roller replacement

Pinch Roller Pressure Adjustment

4. Press the [0] key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
5. Press the [F], [0] and [SET] keys in the 21-key section in sequence.
   This causes the following to appear on the display;

>FO	>PINCH

6. Press the [7] key while pressing the blue [OUT] key in the 21-key section.
   (This causes the pinch roller to be pressed into position.)
7. Using the string, attach the 5kg tension scale to the pinch roller arm. Stretch the tension scale in the direction which connects the pinch roller and capstan, and free the pinch roller from the capstan. After the pinch roller has stopped rotating, return it slowly in the capstan direction and check that the value indicated on the scale is between 3.7 and 4.0kg when the pinch roller has started to rotate again. If this value is not satisfied, adjust using the pressure adjustment screw.
8. When the pressure has been adjusted, check that the clearance between the pinch lever and stopper is 0.3±0.1mm, as shown in Fig.6-40, when the pinch roller is pressed into position. If this value is not satisfied, adjust the stopper position. After the check or adjustment, apply retaining compound to the threaded section of the adjustment screw.
9. Press the [7] key while pressing the blue [OUT] key in the 21-key section.
   (This causes the pinch roller to move away.)
10. Press the [F], [3] and [SET] keys in the 21-key section in sequence.
    (This causes the capstan to stop rotating.)
11. Press the RESET switch S3 on the SV-90 board.
    (Operation will now be returned to the ordinary operation mode.)

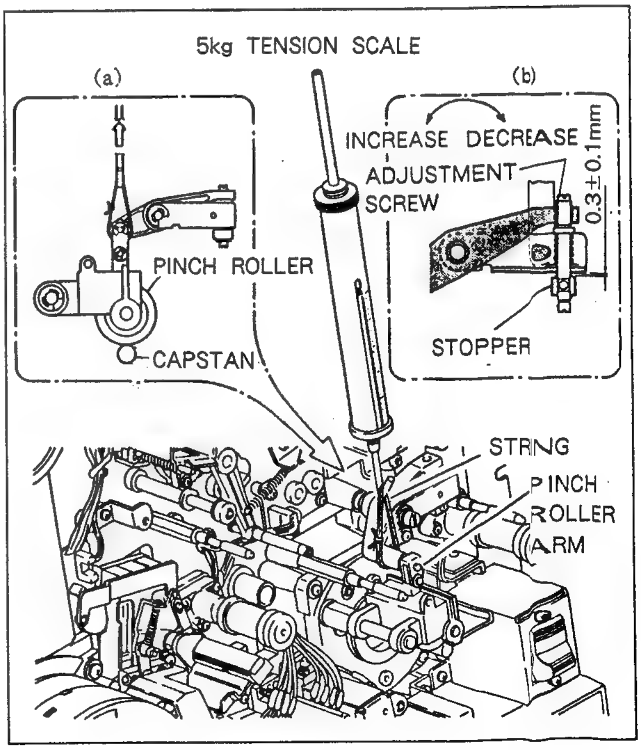


Fig.6-39. Pinch Rroller Pressure Adjustment

6-11. PINCH ROLLER SOLENOID REPLACEMENT

Preliminary Information

A. When the solenoid has been mounted on the bracket, its mounting position must be adjusted. If it is not adjusted properly, it will not be possible to adjust properly the pressure applied by the pinch roller, the clearance between the capstan and pinch roller will not be correct and it may become difficult to thread the tape.

B. After the solenoid has been replaced, the pressure applied by the pinch roller must be adjusted.

Replacement

1. Disconnect connector CN008 from the DS-19 board. If the harness is held in place anywhere, free it.
2. Remove the E-ring (E2.3) and three screws (PSW4 ×10) shown in Fig.6-40 and then rotate the support screw and remove the pinch roller solenoid assembly.
3. While referring to the figure, replace the solenoid with a new unit and re-assemble. Secure the solenoid loosely so that it can still be moved by hand.

Pinch Roller Solenoid Position Adjustment

4. With the solenoid plunger caused to be adsorbed, as shown in Fig.6-40, adjust the mounting position of the pinch roller solenoid so that the clearance between the connecting rod and cushion is set to 7.0±0.2mm. After making the adjustment, tighten up the four screws (PSW3×6).
5. Mount the pinch roller solenoid assembly following steps 2 and 1 in the reverse order.

Pinch Roller Pressure Adjustment

6. Press the [0] key in the 21-key section while keeping the S2 button on the SY-103 board depressed.
7. Press the [F], [0] and [SET] keys in the 21-key section in sequence.
   This causes the following to appear on the display;

>FO	>PINCH

8. Press the [7] key while pressing the blue [OUT] key in the 21-key section.
   (This causes the pinch roller to be pressed into position.)
9. Using the string, attach the 5kg tension scale to the pinch roller arm.(Refer to Fig.6-39.) Stretch the tension scale in the direction which connects the pinch roller and capstan, and free the pinch roller from the capstan. After the pinch roller has stopped rotating, return it slowly in the capstan direction and check that the value indicated on the scale is between 3.7 and 4.0kg when the pinch roller has started to rotate again. If this value is not satisfied, adjust using the pressure adjustment screw.

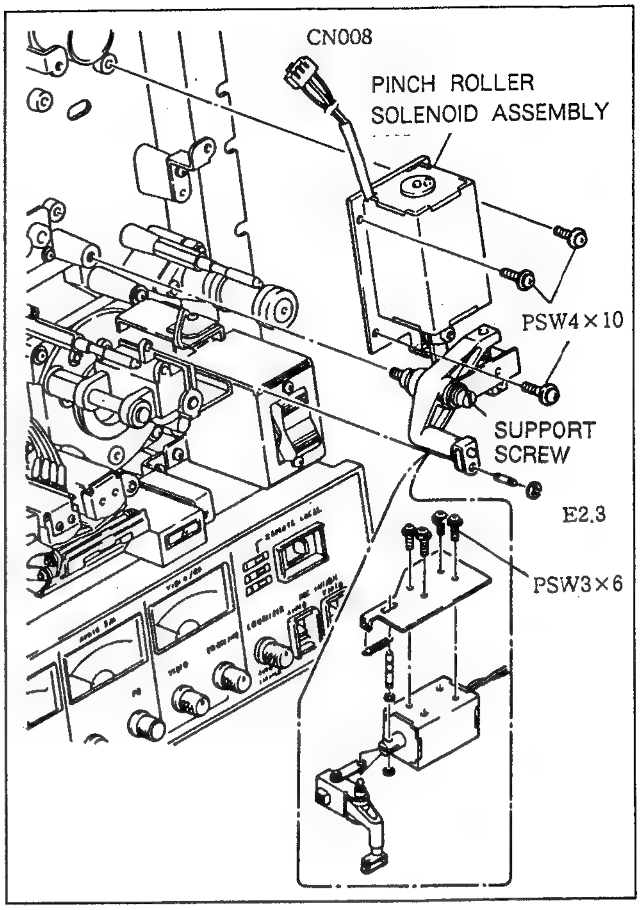


Fig.6-40. Pinch Roller Solenoid Replacement

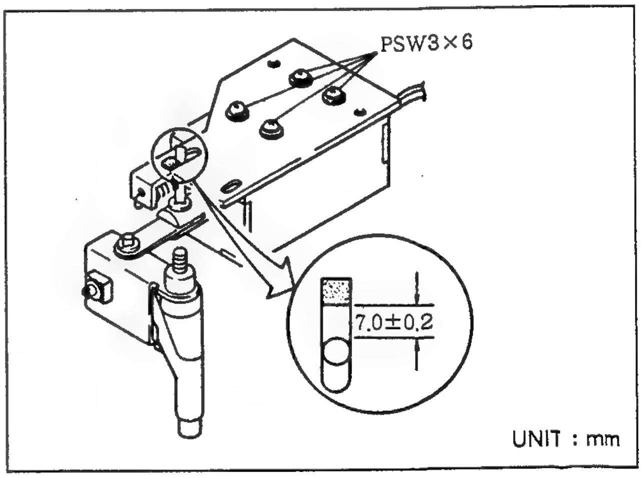


Fig.6-41. Pinch Roller Solenoid Position Adjustment

10. When the pressure has been adjusted, check that the clearance between the pinch lever and stopper is 0.3 ± 0.1mm, as shown in Fig.6-39, when the pinch roller is pressed into position. If this value is not satisfied, adjust the stopper position. After the check or adjustment, apply retaining compound to the threaded section of the adjustment screw.
11. Press the $\boxed{8}$ key while pressing the blue $\boxed{\text{OUT}}$ key in the 21-key section.
    (This causes the pinch roller to move away.)
12. Press the $\boxed{\text{F}}$, $\boxed{3}$ and $\boxed{\text{SET}}$ keys in the 21-key section in sequence.
    (This causes the capstan to stop rotating.)
13. Press the RESET switch S3 on the SV-90 board.
    (Operation will now be returned to the ordinary operation mode.)

6-12. GUIDE POST REPLACEMENT

Preliminary Information

A. The BVH-3000 employs four guide posts, as shown in the figure below.

B. The guide posts and taper guide have an important effect on the recording and playback of the audio and video signals and so after they have been replaced, the following items must be adjusted or checked.
   - Guide Post 1 : Check the tape transport around the guide post 1 in accordance with the instructions for the tape transport adjustments.
   - Guide Post 2 : After having checked the tape transport around the guide post 2 in accordance with the instructions for the tape transport adjustments, it is necessary to perform the checks or adjustments subsequent to the audio/CTL R/P head adjustments (Section 9-9) detailed in the flow chart in Section 9-1.
   - Taper guide : It is necessary to perform the checks or adjustments subsequent to the tape transport adjustments (Section 9-3) detailed in the flow chart in Section 9-1.

Replacement

1. Replace the necessary parts while referring to the figure below.
   Note : Take note of the mounting direction of the spring when replacing the taper guide.
2. Adjust the various items in accordance with "B" in the preliminary information.
   Note : If the guide connected to the tension arm is particularly worn, rotate it so that the worn area does not make contact with the tape.

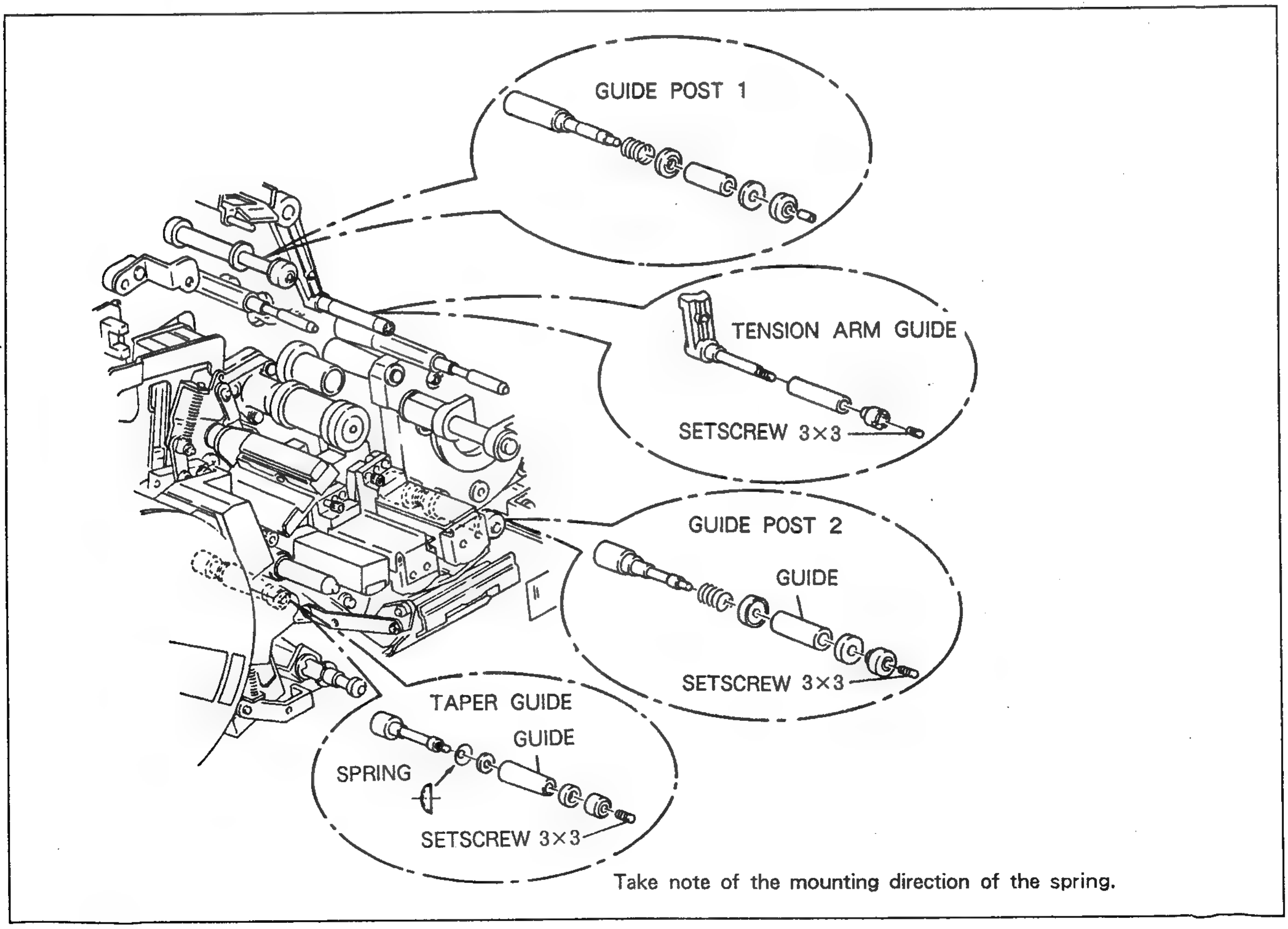


Fig.6-42. Guide Post Replacement

6-13. AUDIO/CTL R/P HEAD

Preliminary Information

When the audio/CTL R/P head (hereafter referred to simply as "the head") is replaced, the resulting azimuth, height and position of the head may differ from the settings prior to the replacement. Adjustments must therefore be made after its replacement with reference to Section 6-13-2.

6-13-1. Audio/CTL R/P Head Replacement

Parts Removal

1. Remove the R/P shield cover.
2. Disconnect the wiring from the head.
3. Remove the two screws (C3×16 and C3×10) shown in Fig.6-43-A and then remove the head.
   Note : Do not remove any other screws.
4. Remove the HD-07 board from the head assembly.
5. Remove the two screws (PS2.6×6) shown in Fig. 6-43-B and remove the head.
   Note : The head can also be replaced without removing the shield case.

Parts Mounting

6. Secure the two screws (PS2.6×6) so that the new head is pressed against the back of the shield case.
   Note : If the shield case has been removed, first secure it loosely to the head base, then place the head assembly on a level stand, as shown in Fig.6-43-C, place a thickness gauge with a 0.4mm thickness between the head and the level stand and, while pressing down lightly on the shield case, tighten up the screws which were secured loosely above.
7. Solder the HD-07 board to the head assembly.

Head Assembly Mounting

8. Align the pin of the head base with the hole shown in Fig.6-43-B and mount it using the two screws which were removed in step 3.
   Note 1 : Tighten up the two screws so that the head is positioned parallel to the audio/CTL erase head located at its side.
   Note 2 : Finally, tighten up the two screws with a 6 to 8kg-cm torque. Take care not to tighten up the screws too much since this may cause the head movement angle to change.
9. Solder the leads to the head while referring to Fig.6-43-D.
10. Replace the R/P shield cover.

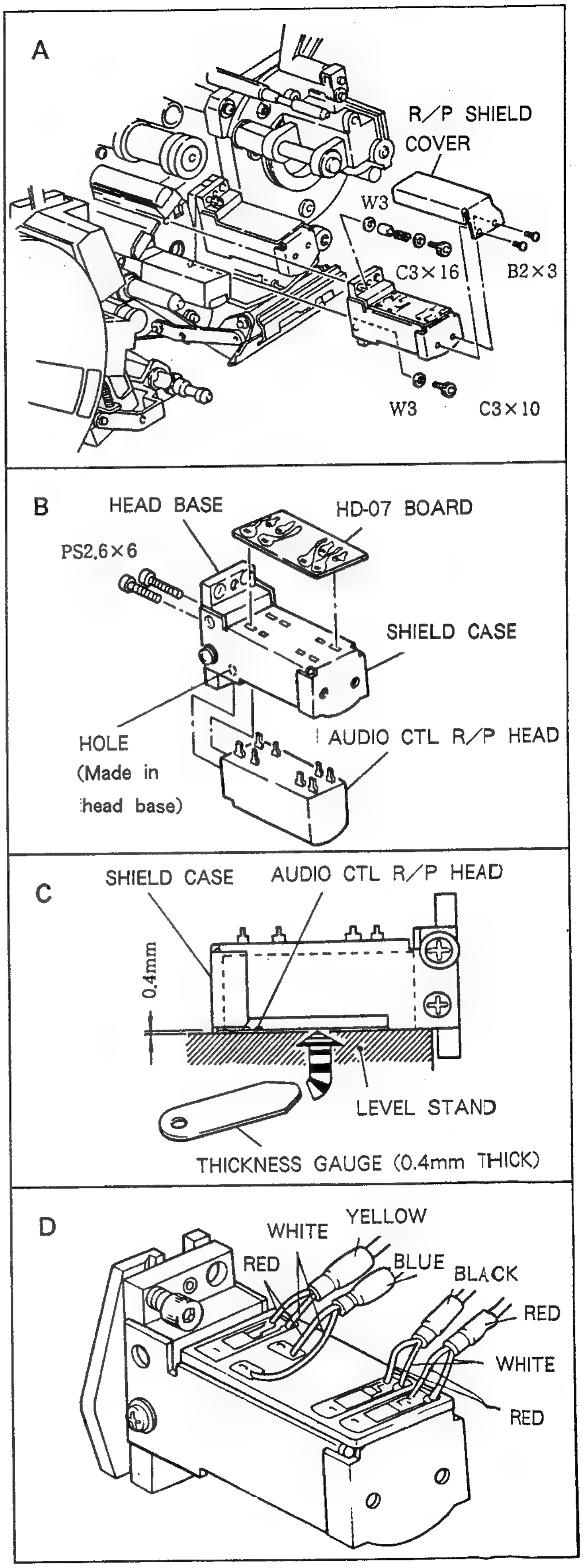
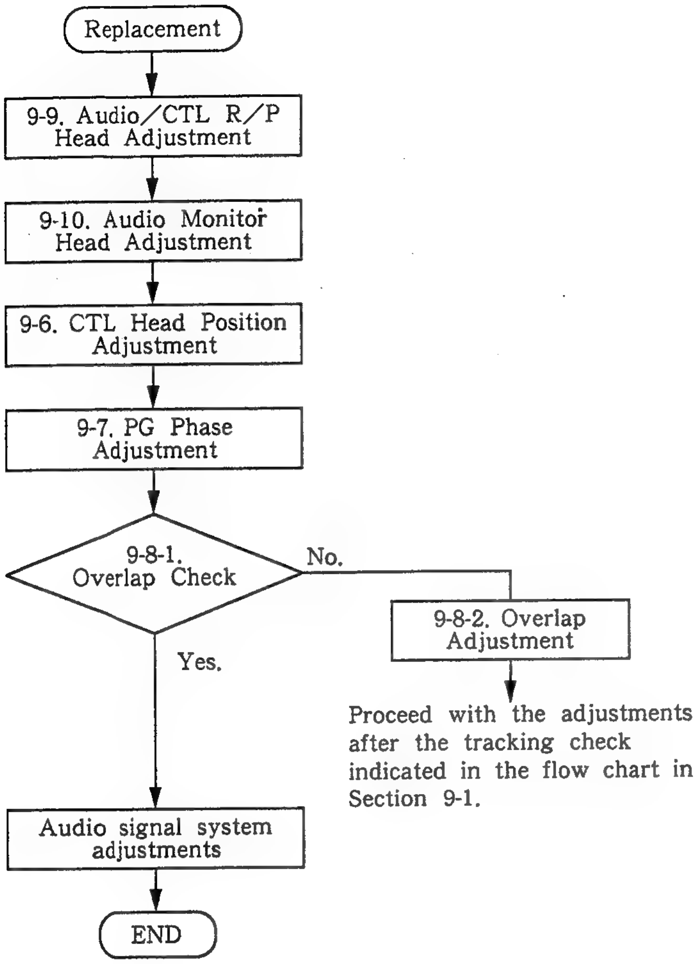


Fig.6-43. Audio/CTL R/P Head Replacement

6-13-2. Adjustments After Audio/CTL R/P Head Replacement



6-14. AUDIO MONITOR HEAD

Preliminary Information

When the audio monitor head (hereafter referred to simply as "the head") is replaced, the resulting azimuth, height and position of the head may differ from the settings prior to the replacement. Adjustments must therefore be made after replacement with reference to Section 6-14-2.

6-14-1. Audio Monitor Head Replacement

Parts Removal

1. Disconnect the wiring from the monitor head.
2. Remove the two screws (C3×16 and C3×10) shown in Fig.6-44-A and then remove the monitor head.
   Note : Do not remove any other screws.
3. Remove the HD-07 board from the head assembly.
4. Remove the two screws (PS2.6×6) shown in Fig. 6-44-B and remove the head.
   Note : The head can also be replaced without removing the shield case.

Parts Mounting

5. Secure the two screws (PS2.6×6) so that the new head is pressed against the back of the shield case.
   Note : If the shield case has been removed, first secure it loosely to the head base, then place the head assembly on a level stand, as shown in Fig.6-44-C, then place a thickness gauge with a 0.4mm thickness between the head and the level stand and, while pressing down lightly on the shield case, tighten up the screws which were secured loosely above.
6. Solder the HD-07 board to the head assembly.

Head Assembly Mounting

7. Align the pin of the head base with the hole shown in Fig.6-44-B and mount it using the two screws which were removed in step 2.
   Note 1 : Tighten up the two screws so that the monitor head is positioned parallel to the audio/CTL R/P head located at its side.
   Note 2 : Finally, tighten up the two screws with a 6 to 8kg-cm torque. Take care not to tighten up the screws too much since this may cause the head movement angle to change.
8. Solder the leads to the head while referring to Fig.6-44-D.

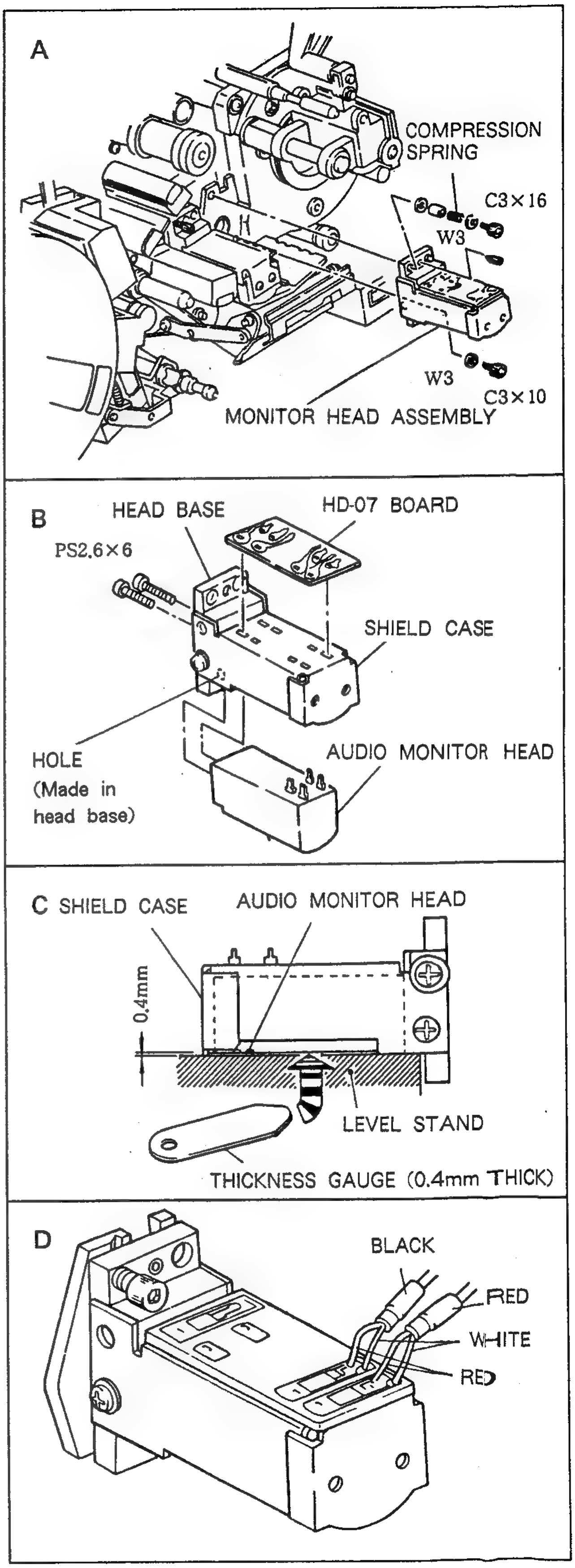
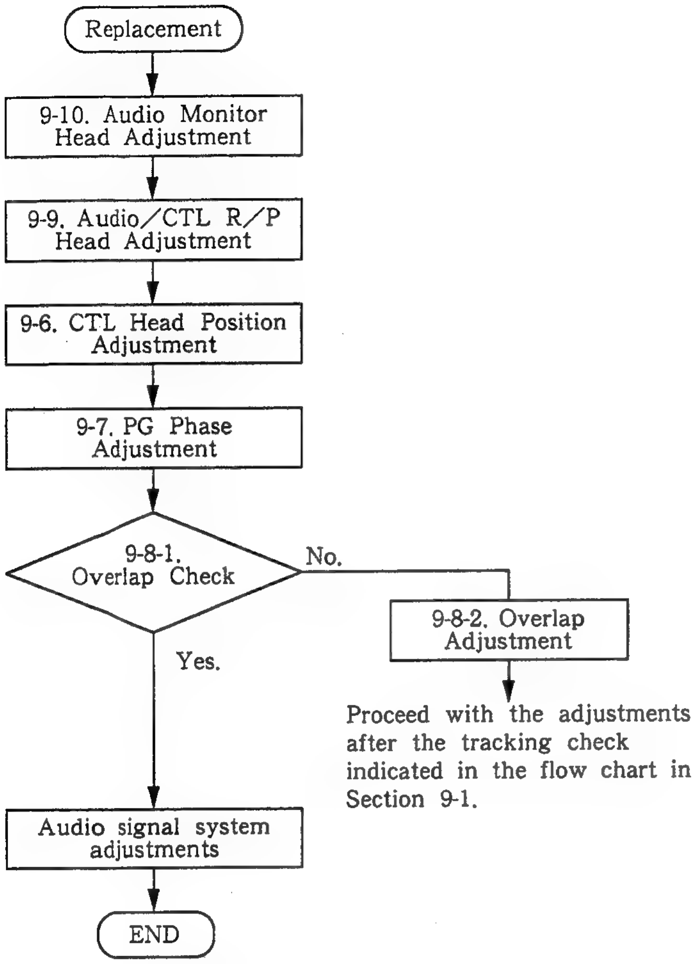


Fig.6-44. Audio Monitor Head Replacement

6-14-2. Adjustments After Audio Monitor Head Replacement



6-15. AUDIO/CTL ERASE HEAD

Preliminary Information
When the audio/CTL erase head (hereafter referred to simply as "the head") is replaced, the height of the head may differ from the setting prior to the replacement. Adjustment must therefore be made after replacement with reference to Section 6-15-2.

6-15-1. Audio/CTL Erase Head Replacement

Parts Removal
1. Disconnect the wiring from the erase head.
2. Remove the two screws shown in Fig.6-45-A and then remove the erase head.
   Note : Do not remove any other screws.
3. Remove the CEH-2 board from the head assembly.
4. Remove the two screws shown in Fig.6-45-B and remove the erase head.

Parts Mounting
5. Secure new head using the two screws (PS2.6×6) to the head base so that the head can be moved lightly.
6. Place the head on a flat stand, as shown in Fig. 6-45-C and, while pressing down from above, tighten up the two screws.
7. Solder the CEH-2 board so that it is brought into tight contact with the rear of the head.

Erase Head Assembly Mounting
8. Mount the erase head assembly onto the machine using the two screws (PS3×8).
9. Solder the leads to the erase head while referring to Fig.6-45-D.

6-15-2. Adjustments After Audio/CTL Erase Head Replacement

(Replacement)
↓
9−11. Audio/CTL Erase Head Height Adjustment
↓
Audio Signal System Adjustment
↓
(END)

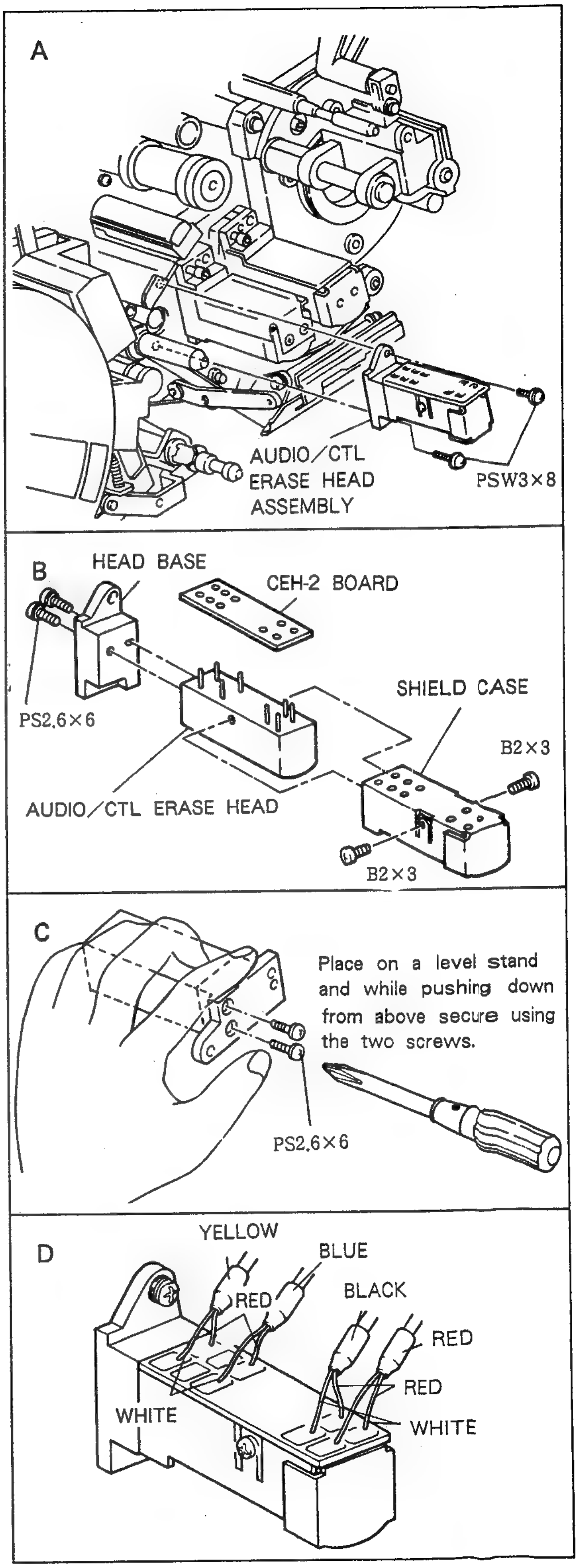


Fig.6-45. Audio/CTL Erase Head Replacement

6-16. BLOWER REPLACEMENT

6-16-1. Take-up Side Blower Replacement

1. Remove the head cover, drum panel and reel panel from the front of the machine.
2. Move to the rear of the machine, loosen the four screws (PSW3×8) securing the rear cover and open the power supply section.
3. Remove the three screws (PSW4×16) securing the RM-43 board and draw the board down to the front, as shown in the figure.
4. Remove the screw (PSW4×10) securing the DD case.
5. Remove the two screws (PSW3×8) securing the DD-7 board.
6. Remove connector CN011 on the DS-19 board at the front of the machine.
7. Remove the four screws (PSW3×8, PSW3×12) securing the blower, replace the blower with a new unit and remount.
   Note : Make sure that the harness projects from the top of the blower mounting area, as shown in the figure.
8. Pass blower connector CN011 through the inside of the RM-43 board, lead it to the top from the hole in the base plate and connect it to the prescribed position on the DS-19 board.
9. Reinstall the parts by proceeding in reverse from Step 5.
10. Install the reel, close the front cover and check that the "air threading" can be made.

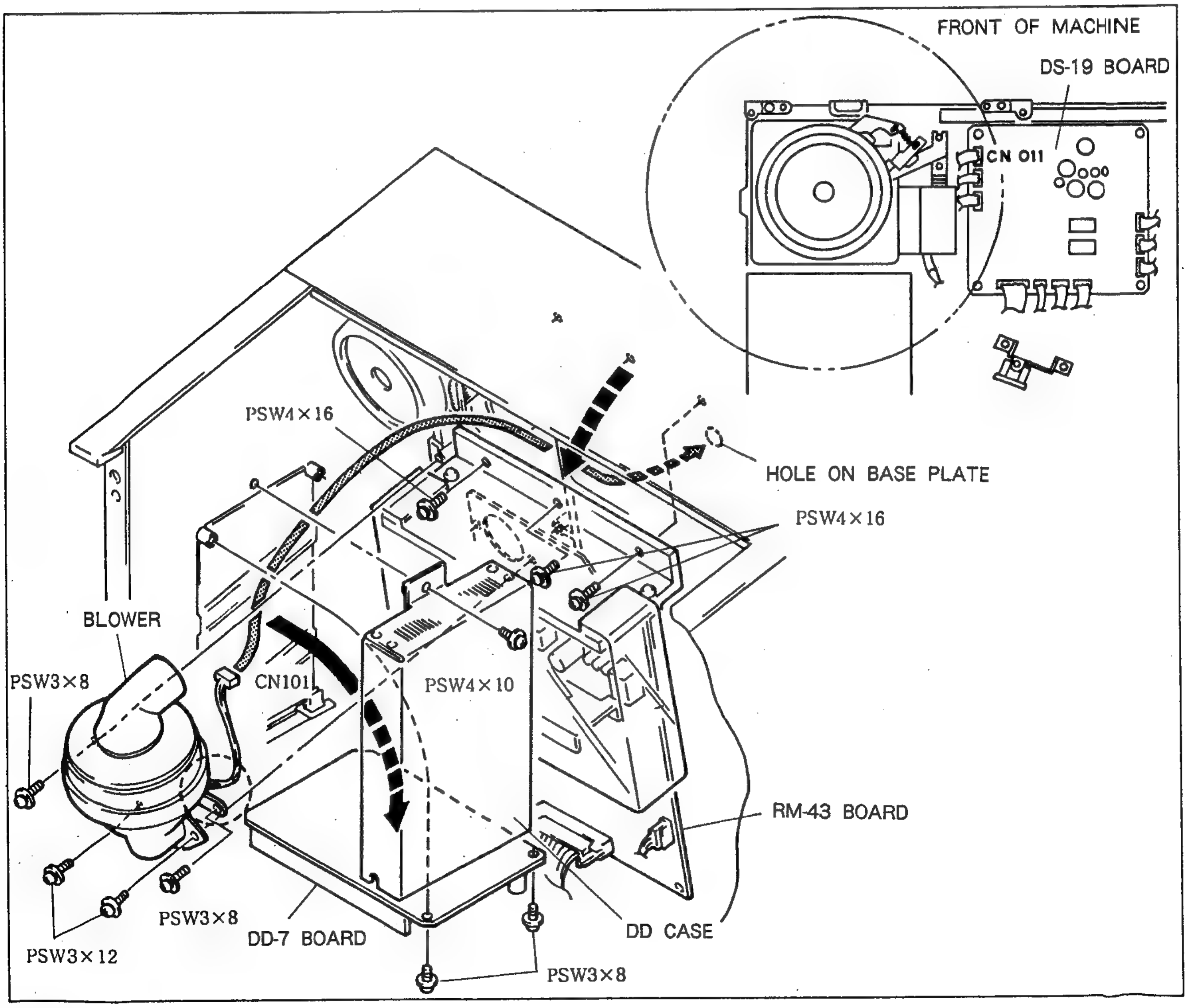


Fig.6-46. Take-up Side Blower Replacement

6-16-2. Supply Side Blower Replacement

1. Move to the rear of the machine, loosen the four screws securing the rear cover and open the power supply section.
2. Disconnect connector CN103 of the CD-36 board.
3. Remove the two screws securing the CD-36 board.
4. Remove the four screws (PSW3×8, PSW3×12) securing the blower, replace the blower with a new unit and remount.
5. Secure the CD-36 board using the two screws (PSW3×8).
6. Connect connector CN103 to its original position on the CD-36 board and lead the harness around the parts as before.
7. Close the power supply section and secure the rear cover.
8. Install the reel, close the front cover and check that the "air threading" can be made.

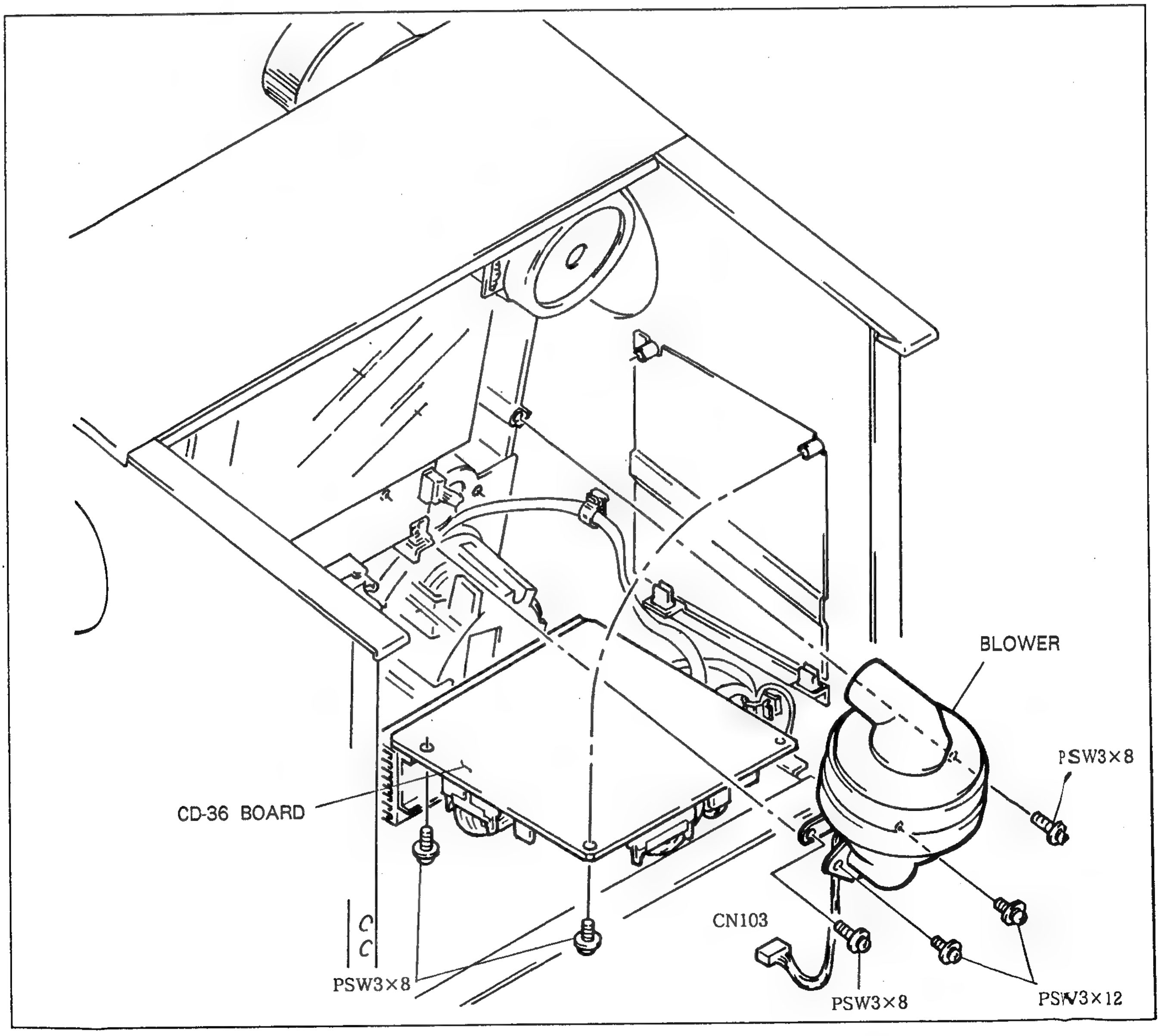


Fig.6-47. Supply Side Blower Replacement

6-17. FULL ERASE HEAD/VS ERASE HEAD REPLACEMENT

Preliminary Information

A. The NTSC/PAL-M machine is provided with the full erase head and the PAL/SECAM model with the VS erase head.

B. The tape wrap angle near the full erase head or VS erase head is small and so the head mounting position must be adjusted.

C. Besides the adjustment of the mounting position of the VS erase head, the height of this head must also be adjusted.

D. The VS erase head is judged to have the proper height if the CH-1 and CH-3 audio signals are not erased by this head when the signals are recorded in the assemble mode.

6-17-1. Full Erase Head Replacement (for NTSC/PAL-M Model)

1. Remove the screw (B3×6) and remove the air guide.
2. Loosen the support screw sufficiently and remove the full erase head assembly.
3. Disconnect the wiring from the full erase head assembly.
4. Replace the full erase head with a new unit, place it on a flat stand as shown in Fig.6-49, align the side of the head and the side of the base and secure using the two screws (PS2.6×10) whose ends have been coated with the retaining compound given below.
   Adhesive : 1401B or 1401C made by Three Bond, or equivalent
5. Remount the full erase head assembly in the machine from step 3 and proceed in the reverse order to its removal.

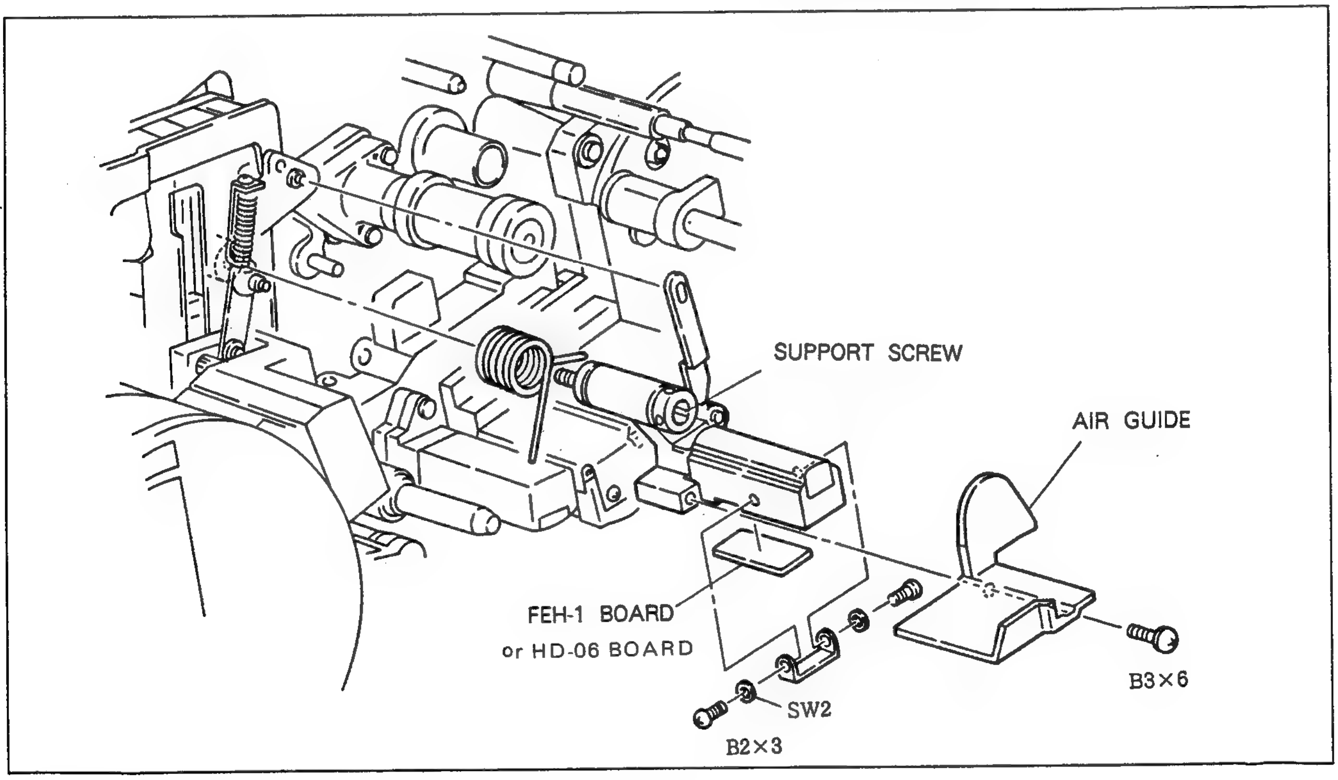


Fig.6-48. Full Erase Head/VS Erase Head Replacement

6-17-2. VS Erase Head Replacement (for PS Model)

1. Remove the screw (B3×6) and remove the air guide.
2. Loosen the support screw sufficiently and remove the VS erase head assembly.
3. Disconnect the wiring from the VS erase head assembly.
   Note : Do not misplace the spacer if a spacer has been mounted between the VS erase head and base.
4. Replace the VS erase head with a new unit, place it on a flat stand as shown in Fig.6-49, align the side of the head and the side of the base and secure using the two screws (PS2.6×10) whose ends have been coated with the retaining compound given below.
   Note : Mount the spacer again if a spacer has been mounted between the VS erase head and base.
   Adhesive : 1401B or 1401C made by Three Bond, or equivalent
5. Remount the VS erase head assembly in the machine from step 3 and proceed in the reverse order to its removal.
6. Record 3kHz signals onto audio channels CH-1 and CH-3.
7. Rewind the portion recorded in step 6 part of the way and then record the video signals onto the video and sync channels in the assemble mode.
8. Connect the oscilloscope to the AUDIO-1 and AUDIO-3-OUT connectors on the connector panel.
9. Check that the oscilloscope waveforms do not change before and after the assemble IN point when the portion recorded in steps 6 and 7 is played back. If any change is registered, proceed with the following adjustment.

Adjustment

10. Loosen the support screw sufficiently and remove the VS erase head assembly.
11. Depending on the symptom, change the thickness of the spacer, as shown in the figure.
    a. Reduce the thickness of the spacer when the AUDIO-1 waveforms change.
    b. Increase the thickness of the spacer when the AUDIO-3 waveforms change.
    Note : When securing the head, refer to step 4 and adjust the position of the head.
    Spacers with the following thicknesses are supplied.

Thickness (mm)	Sony Part No.
0.05	3-651-419-01
0.1	3-651-419-21

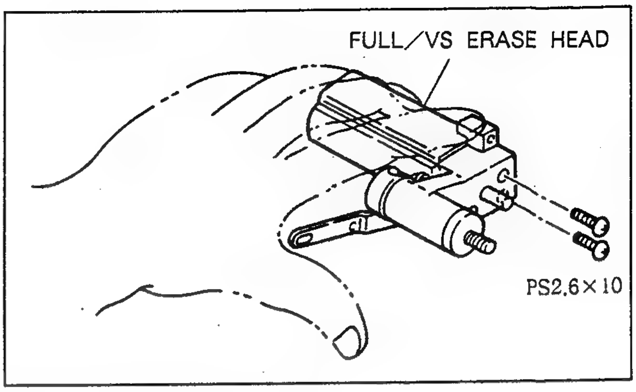


Fig.6-49. Position Adjustment

12. After the VS erase head has been remounted, perform steps 6 through 9 again and check the head height.

SECTION 7
GENERAL INFORMATION FOR ALIGNMENT

7-1. INDEX OF ADJUSTMENT COMPONENTS

The following table lists the adjustment components on the circuit boards and the section number of their adjustment procedures.

PR-92/98 board

CT1 14-6

LV2 14-27
LV3 14-27
LV4 14-31
LV5 14-31

RV1 14-34
RV2 14-34
RV3 14-5
RV4 14-26
RV5 14-5
RV6 14-6
RV7 14-6
RV8 14-5
RV9 14-4
RV10 14-4
RV11 14-4
.... 14-38
RV12 14-3
RV13 14-28
RV14 14-28
RV15 14-27
RV16 14-29
RV17 14-29
RV18 14-29
RV19 14-29
RV20 14-29
RV21 14-32
RV26 14-28
.... 14-30
RV27 14-34
RV28 14-33

S1 14-38
S2 14-38

RD-7 board

RV3 13-9
.... 13-10
RV4 13-4
RV5 13-7
RV6 13-8
RV7 13-6
RV8 13-9
.... 13-10
RV9 13-10
RV11 13-5
RV12 13-14
RV13 13-14
RV14 13-14
RV15 14-15
RV16 14-21
RV17 14-15
RV19 14-24
RV20 14-22
RV21 14-25
.... 14-35
RV22 14-36
RV24 14-37
RV25 14-37
RV26 14-25
RV27 14-15
RV28 14-23
RV29 13-9
.... 13-11
RV30 13-3

RP-32 board

LV1 12-18
LV2 12-18

RV1 12-13
RV2 12-13
RV3 12-18
RV4 12-18

SP-01 board

RV171 8-2
RV201 8-2
RV202 8-2
RV203 8-2

SP-02 board

RV201 8-6
RV203 8-5
RV204 8-5
RV205 8-5
RV206 8-5
RV207 8-5
RV208 8-5
RV209 8-5
RV210 8-5
RV471 8-6
RV671 8-5
RV672 8-5

SP-03 board

RV201 8-3
RV202 8-3
RV203 8-4
RV271 8-3
RV571 8-3

SV-90 board

RV1 10-3
RV2 10-3
RV3 10-3

VO-16 board

CT1 12-19

RV1 12-5
RV2 12-6
RV3 12-8
RV4 12-7
RV5 12-20
RV6 12-19
RV7 12-19
RV8 12-19
RV9 12-11
RV10 12-11
RV11 12-4
RV12 12-14
.... 12-21
RV13 12-16
RV15 12-6
RV16 12-6
RV17 12-9
RV18 12-9
RV19 12-14
.... 12-21
RV20 12-14
.... 12-21
RV21 12-14
.... 12-21
RV22 12-14
.... 12-21
RV23 12-15
RV24 12-15
RV25 12-15
RV26 12-15
RV27 12-15
RV28 12-15
RV29 12-17
RV30 12-15
.... 12-16
RV31 12-22
RV32 12-22
RV34 12-8
RV35 12-16
RV36 12-16
RV37 12-8
RV39 12-4
RV40 12-6
RV41 12-10

VR-51 board

RV3 11-3
(A1 REC level preset)
RV5 11-4
(A1 PB level preset)
RV7 11-3
(A2 REC level preset)
RV9 11-4
(A2 PB level preset)
RV11 11-3
(A3 REC level preset)
RV11 11-3
(A3/A4 REC level preset)
RV13 11-3
(A3 PB level preset)
RV13 11-3
(A3/A4 PB level preset)
RV15 12-4
(VIDEO level preset)
RV19 11-3
(A3 REC level preset)
RV20 11-4
(A3 PB level preset)

VS-30 board

RV1 12-3
RV2 12-23
RV3 12-3
RV4 12-3

7-2. EQUIPMENTS AND TOOLS

The following equipments and tools, other than general tools, are required for alignment. As for items 1 through 12, see section 2-7.

1. EX-136 Extender
Sony Part No. A-6001-007-A

2. BR5-2PS-A4 Alignment Tape
Sony Part No. 8-944-005-63

3. Tension Scale, 5k grams
Sony Part No. J-6041-640-A

4. Tension Adjustment Tool
Sony Part No. J-6251-960-A

5. Drum Eccentricity Adjustment Gauge
Sony Part No. J-6250-800-A
(or J-6040-750-A/B)

6. Tapered Screw
Sony Part No. J-6040-460-A

7. Thickness Gauge
Sony Part No. J-6041-670-A

8. Flat Plate
Sony Part No. J-6040-160-A

9. IC Test Clip
TC-16 Sony Part No. J-6041-770-A
TC-20 Sony Part No. J-6041-780-A

10. L-shaped Hexagonal Wrench Set
Sony Part No. J-6041-700-B
(or 7-700-736-00)

11. Hexagonal Screwdriver
2.5mm Sony Part No. 7-700-766-04
3mm Sony Part No. 7-700-766-05

12. Brake Adjustment Fixture
Sony Part No. J-6043-720-A

13. Digital Voltmeter
Effective digits : more than 4½ digits
Accuracy : less than 0.02%, ±1 count

14. Oscilloscope

15. Electronic Load
Input load voltage : 5 to 100Vdc or greater
Input load current : 0 to 7A min.
(constant current mode)
Allowable load power : 100W min.
Equivalent product : PLZ152W /Kikusui International
Used for section 8-5. variable voltage system adjustments.

16. DC Power Supply
Output voltage : +5V to +8V
(Current : several milliamps or below)
Used for section 8-5. variable voltage system adjustments.

17. Audio Oscillator

18. Audio Level Meter

19. 1kHz Bandpass Filter
Q : more than 5
Attenuation : more than 12dB/oct.
S/N ratio : more than 70dB
Used for section 11-17. PB A1-PB A2 crosstalk adjustment.

20. 15kHz Bandpass Filter
Q : more than 5
Attenuation : more than 12dB/oct.
S/N ratio : more than 70dB
Used for section 11-17. PB A1-PB A2 crosstalk adjustment.

21. PAL Test Signal Generator
The generator must generate the signals shown in section 7-3.
Equivalent product :
1411/Tektronix
and the following plug-in units
SPG12 Sync generator
TSG11 Color bar generator
TSG13 Linearity generator
TSG15 Pulse & bar generator
TSG16 Multiburst generator

22. PAL Waveform Monitor
Equivalent product : 1481/Tektronix

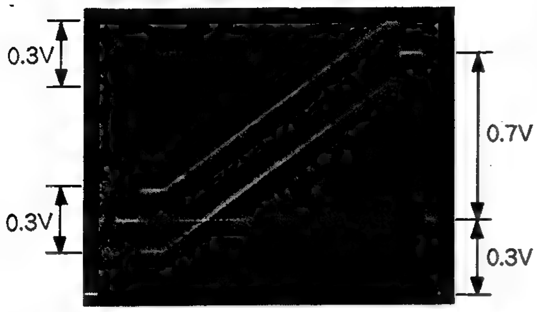
23. PAL Vectorscope
Equivalent product : 521A/Tektronix

24. SC-H Phase Monitor
Equivalent product : 1751/Tektronix
Used for sections 13-14. reference SC-H adjustment and 14-18. TBC OUT SC-H adjustment.

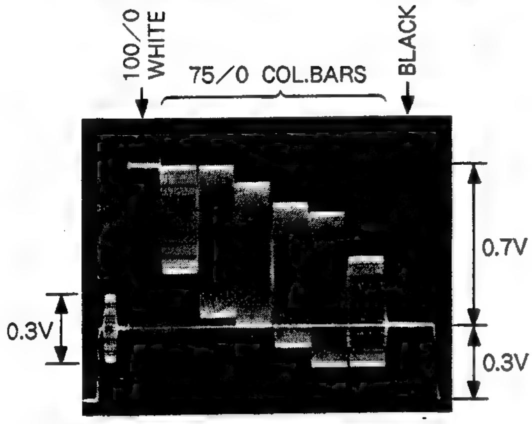
25. Spectrum Analyzer
Equivalent product : 141T/Hewlet Packard
Used for sections 12-8. EE moire adjustment, 12-16. playback moire adjustment and 12-20. recording system moire adjustment.

7-3. TEST SIGNALS

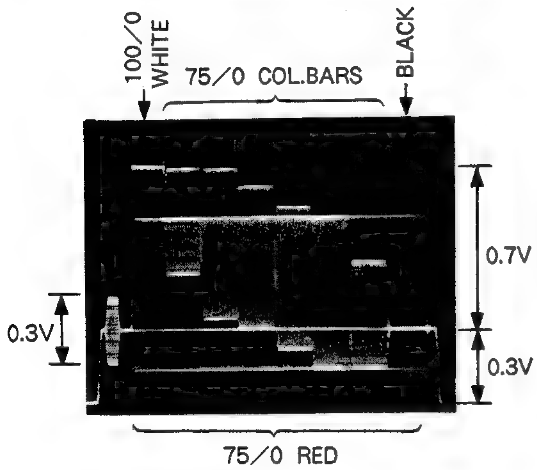
PAL RAMP LINEARITY



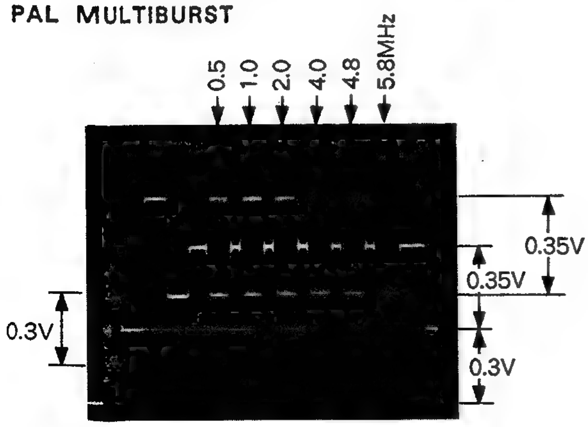
PAL COLOR BARS



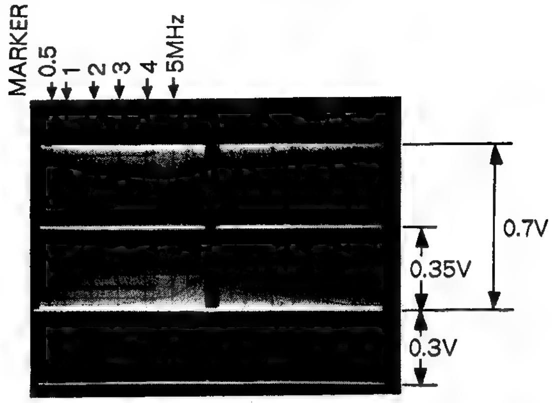
PAL HALF-RED COLOR BARS



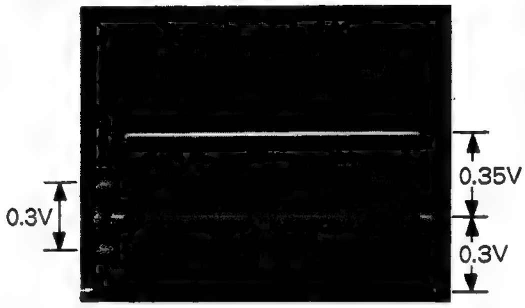
PAL MULTIBURST



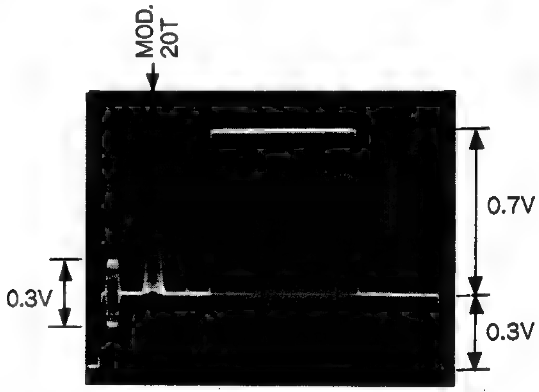
PAL VIDEO SWEEP (FIELD RATE)



PAL 50% FLAT FIELD



PAL MOD 20T (AND BAR)

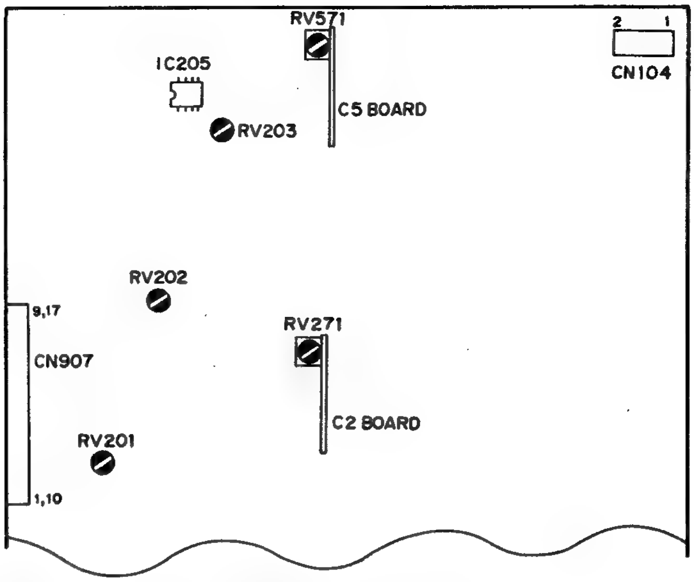


MOIRE SIGNAL

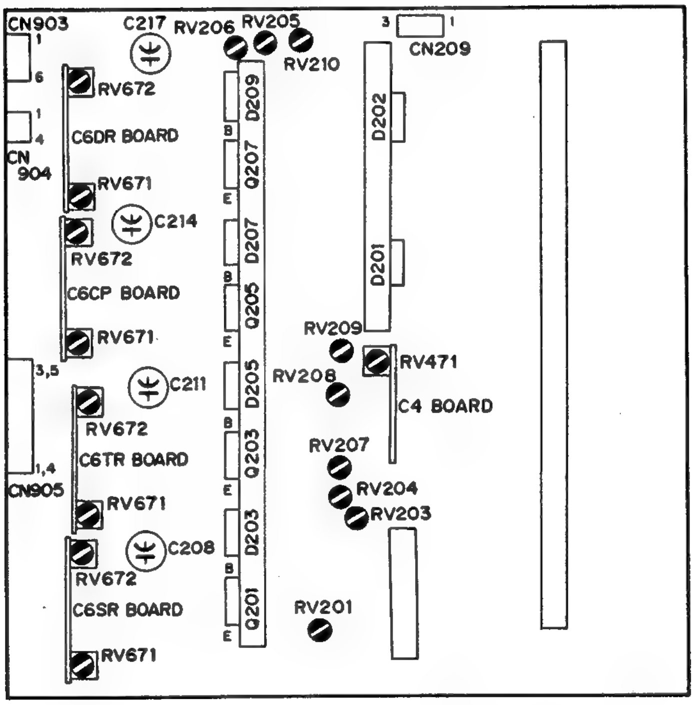
See section 12-8.

SECTION 8
POWER SUPPLY ALIGNMENT

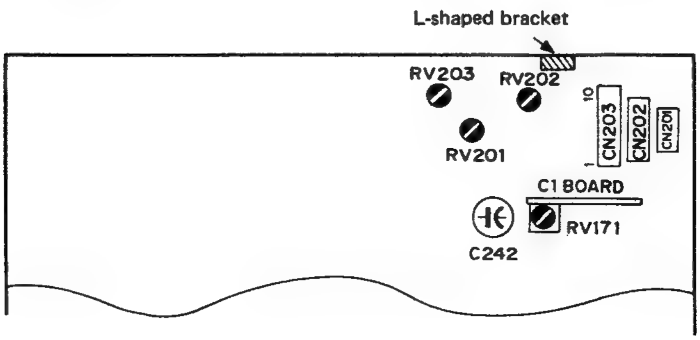
SP-03 Board
(Component Side)



SP-02 Board
(Component Side)



SP-01 Board
(Component Side)



[CAUTION 1]
The power supply boards contain primary side parts and high-voltage parts and so care should be taken to avoid touching them when they are "live" and receiving an electric shock. Read through "Section 2-3. Notes on Power Unit" before proceeding with the inspection and adjustment.

[CAUTION 2]
The heat sinks on the boards have a thermal capacity which is rated on the assumption that cooling will be provided by the fans. Care should thus be taken not to operate the VTR over prolonged periods of time during inspection and at other such times without fan cooling.

8-1. DIAGNOSIS

When something has gone wrong with the power supply section, visually inspect whether foreign matter has entered inside or whether any of the parts have been discolored or deformed before proceeding to check the operation of each board. An alternative method of conducting inspections is to bring your hands near the power supply section and locate any parts which have been heated up by high temperatures. Yet another method of inspection which is effective in locating trouble areas is to use a VOM (Volt/Ohm meter) to check the conductivity of the components and check the polarities of the semiconductors in accordance with the schematic diagrams with no power supplied.

Since this power unit consists of four switching regulators of the half-bridge inverter type, four switching regulators of the DC/DC converter type, and six series regulators, trouble spots can also be effectively located by comparing and contrasting the characteristics of the regulators.

Half-bridge inverter type of switching regulators

T101/SP-01 board	+5V
T101/SP-02 board	PRE-REGULATOR (+90V)
T101/SP-03 board	+13V SOL
T105/SP-03 board	±18V

DC/DC converter type of switching regulators

Q201/SP-02 board	S-REEL VH
Q203/SP-02 board	T-REEL VH
Q205/SP-02 board	CAPSTAN VH
Q207/SP-02 board	DRUM VH

Series regulators

Q202/SP-01 board	+17V
Q209/SP-01 board	−5V
Q209/SP-02 board	F+17V
Q201/SP-03 board	+12V
Q204/SP-03 board	−12V
IC206/SP-03 board	+12V FAN/+12V CON

A great deal can be accurately guessed about the trouble from the nature of trouble itself. Reference should be made to the flow chart below.
When the supply power output has been stopped, set the power switch to OFF, wait for at least 30 seconds (or at least 2 minutes with a 220/240V AC power line voltage), check the situation and then turn it back to ON again.

(1) Is the AC power line breaker ON?

The AC power breaker will be tripped if the AC power supply capacity is inadequate.

NO

YES

Provide a connection to an AC power supply with a higher capacity.

(2) Is the AC input voltage adequate?

If the VTR is set to the F. FWD or REW mode when the AC line impedance is high or when equipment with a high power consumption is connected to the same AC line, the AC voltage supplied to the VTR may drop and the VTR may stop operating or the VTR's input breaker (AC-82 board) may be tripped.

NO

YES

Check whether the supply/take-up reel motor drive circuit/RM-43 board is overloaded.
If the input breaker CB1/AC-82 board is OFF, set it back to ON.

(3) Has the OVERHEAT alarm been given?

When it is no longer possible to cool the power unit or when an abnormal load is kept applied to +5V/+18V/−18V/+13V SOL system, the supply power output will shut down in order to protect the power circuitry from overheating. In cases like this, the OVERHEAT alarm will appear on the control panel and the VTR will then stop before the power output shuts down. Check the situation immediately prior to the power output shutdown and then switch the power back on.

YES

NO

Check whether the trouble lies in the fans.
Check which of the +5V/+18V/−18V/+13V SOL systems has been heated up to a high temperature and inspect the load of that system.

(4) Has the rush current limiting relay been activated?

Relay RY101/SP-01 board inside the power unit is activated immediately after the power has been switched on. If you listen at the rear panel of the VTR, you can check that the relay is activated by the sound it makes when the power switch is set to ON. If the relay is activated, the rectifier section, starter section and +5V switching regulator will be activated.

NO

YES

Inspect the rectifier section (D101/SP-01 surrounding parts).
Inspect the starter section (IC102/SP-01 surrounding parts).
Inspect the +5V switching regulator (T101/SP-01 surrounding parts).

(5) Does the power output stop several seconds after the power has been switched on?

Note : Set the power switch to OFF, wait for at least 30 seconds (or at least 2 minutes with a 220/240V AC power line voltage), and then turn it back to ON again.

YES

NO

(6) Do the LEDs of the audio meters light?

NO

YES

Inspect +18V (pin 4/CN907/SP-03), −18V (pin 16/CN907/SP-03) and +17V (pin 2/CN207/SP-03).

(7) Are the fans working?

NO

YES

Inspect +13V SOL (pin 12/CN907/SP-03).

(8) Are the +12V, −12V and −5V voltages being output?

Insert the extension circuit board into card rack slot 5 and check the voltages at the +12V, −12V and −5V pins on the extension circuit board.

NO → Inspect +12V (pin 13/CN907/SP-03), −12V (pin 17/CN907/SP-03) and −5V (pin 12/CN902/SP-01).

YES ↓

(9) Is the pre-regulator (+/C205/SP-02) voltage about +90V?

NO → Check the T101/SP-02 surrounding parts.

YES ↓

(10) Is the F+17V (collector/Q209/SP-02) voltage about +17V?

NO → Check the Q209/SP-02 surrounding parts.

NO ↓

(11) Has INITIALIZE appeared on the control panel?

NO → Inspect the IC205/SP-03 surrounding parts unless PW ACT-SYS (pin 2/CN906/SP-03) is 0V DC.

YES ↓

(12) Are the fans working?

NO → Inspect +12V FAN (pin 1/CN206/SP-03).

YES ↓

(13) Is the drum rotating?

NO → Inspect the drum motor system.

YES ↓

(14) Is the take-up reel rotating?

NO → Inspect the take-up reel motor system.

YES ↓

(15) Is the supply reel rotating?

NO → Inspect the supply reel motor system.

YES ↓

(16) Is the capstan rotating?

NO → Inspect the capstan motor system.

8-2. +17V/+5V/−5V ADJUSTMENTS

[Preparations]

Refer to Section 2-3-6 and take out the SP-01 board from the power unit. Connect all the connectors on the board. Insert the extension circuit board into card rack slot 5. Switch on the power and set the VTR to the stop (STANDBY OFF) mode.

[Adjustments]

Adjustment item	Measuring point Cold pin in parentheses	Specifications	Adjustment
+17V	Pin2/CN203/SP-01 board (L-shaped bracket nearby CN203)	+17.0±0.1Vdc	⊘RV201/SP-01 board
+5V	+5V pin/extension circuit board/slot 5	+5.00±0.05Vdc	⊘RV202/SP-01 board (⊘RV171/C1 board/SP-01 board)
	If the adjustment cannot be made by ⊘RV202, first use ⊘RV171 for the coarse adjustment and then use ⊘RV202 for the fine adjustment.		
−5V	−5V pin/extension circuit board/slot 5	−5.00±0.02Vdc	⊘RV203/SP-01 board

After the adjustments switch off the power and return the SP-01 board to the inside of the power unit.

8-3. +13V SOL/+12V/−12V/+18V ADJUSTMENTS

[Preparations]

Refer to Section 2-3-6 and take out the SP-03 board from the power unit. Connect all the connectors on the board. Insert the extension circuit board into card rack slot 5. Switch on the power and set the VTR to the stop (STANDBY OFF) mode.

[Adjustments]

Adjustment item	Measuring point Cold pin in parentheses	Specifications	Adjustment
+13V SOL	Pin 12/CN907/SP-03 board (Pin 3/CN907)	+13.6±0.1Vdc	⊘RV271/C2 board/SP-03 board
+12V	+12V (+18V) pin/extension circuit board/slot 5	+12.00±0.02Vdc	⊘RV201/SP-03 board
−12V	−12V (−18V) pin/extension circuit board/slot 5	−12.00±0.02Vdc	⊘RV202/SP-03 board
+18V	*Pin 4/CN907/SP-03 board (Pin 14/CN907)	+19.0±0.2Vdc	⊘RV571/C5 board/SP-03 board

*Use 1a/CN-B/extension circuit board/slot 5 (1b/CN-B) as the measuring point for the following models.
BVH-3000 (UC) #10701 and higher
BVH-3100 (UC) #10701 and higher
BVH-3000PS (EK) #10401 and higher
BVH-3100PS (EK) #10601 and higher

Leave the SP-03 board on top of the power unit as it is and proceed with next adjustment.

8-4. PW ACT ADJUSTMENT

[Preparations]

Same as for previous section.

[Adjustments]

Measure the DC voltage at pin 1 (pin 2=cold) /CN104/SP-03 board. This is now taken to be V_B.
[CAUTION] V_B is the primary side voltage. Proceed cautiously so as to avoid electric shocks.

Adjust the DC voltage at pin 5 (pin 4=cold) /IC205/SP-03 board as follows :

Spec : $\frac{2.5}{90} \times V_B$ ⊘RV203/SP-03 board

(Note) V_B depends on the AC power line voltage. When the AC power line voltage is 100Vac, V_B will be approximately 100Vdc.

After the adjustment switch off the power and return the SP-03 board to the inside of the power unit.

8-5. VARIABLE VOLTAGE SYSTEM ADJUSTMENTS

The following 4 systems are included in the variable voltage system :

S-REEL VH
T-REEL VH
CAPSTAN VH
DRUM VH

Proceed with the following 4 adjustments for each of these four systems.

Output current limiting adjustment
Output power limiting adjustment (with maximum voltage)
Output power limiting adjustment (with minimum voltage)
Output voltage adjustment

The following equipments are required for these adjustments.

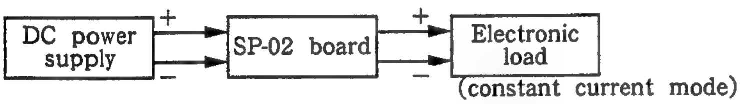
[CAUTION] Do not attempt to undertake these adjustments if this equipment is not available.

Electronic load	Input load voltage :	5 to 100Vdc or greater
	Input load current :	0 to 7A min.(constant current mode)
	Allowable load power :	100W min.
	Equivalent product :	PLZ152W by Kikusui International
DC power supply	Output voltage :	+5V to +8V (Current : several milliamps or below)
DC voltmeter		
Oscilloscope		

[Preparations]

Refer to Section 2-3-6 and take out the SP-02 board from the power unit. Leave connectors CN903, 904 and 905, which connect the SP-02 board with the VTR, disconnected from the SP-02 board. Connect all the other connectors.

Connect the DC power supply and electronic load to the SP-02 board. Use the electronic load in the constant current mode.



Refer to step (1) and following for the settings of the DC power supply and electronic load and for the destinations of the connections on the SP-02 board.

[CAUTION] When the DC power supply and electronic load are connected, set the power of the equipment ON and OFF in accordance with the following sequence.

ON : VTR → DC power supply → Electronic load
OFF : VTR → DC power supply → Electronic load

Switch off the power here as quickly as possible.

(1) S-REEL VH adjustments

Connect the DC power supply and electronic load as follows.
DC power supply (+) → Pin 5/CN903/SP-02 board
DC power supply (−) → Pin 6/CN903/SP-02 board
Electronic load (+) → Pin 4/CN905/SP-02 board
Electronic load (−) → Pin 1/CN905/SP-02 board

Following the table below, set the output voltage of the DC power supply and the load current of the electronic load, and proceed to adjust.

Adjustment item	DC power supply	Electronic load (constant current)	Measuring point (SP-02 board) Cold pin in parentheses	Specifications/adjustment (SP-02 board)
Output current limiting	+8.00±0.05V	5.0A	Cathode/D203 (Heat sink for D203)	Turn ⊘RV203 counterclockwise, then rotate it slowly clockwise and stop at point where pulses vanish. Take care not to rotate ⊘RV203 too far.  (After adjustment, the power supply will stop automatically.)
Output power limiting (with max. voltage)	+8.00±0.05V	1.1A	Pin 4/CN905 (Pin 1/CN905)	+78.5±0.5Vdc ⊘RV671/C6SR board/SP-02 board
Output power limiting (with min. voltage)	+8.00±0.05V	4.4A	Pin 4/CN905 (Pin 1/CN905)	+20.0±0.2Vdc ⊘RV207
Output voltage	+5.00±0.01V	1.6A	Pin 4/CN905 (Pin 1/CN905)	+49.5±0.2Vdc ⊘RV672/C6SR board/SP-02 board

(2) T-REEL VH adjustments

Connect the DC power supply and electronic load as follows.

DC power supply (+) → Pin 4/CN903/SP-02 board
DC power supply (−) → Pin 6/CN903/SP-02 board
Electronic load (+) → Pin 5/CN905/SP-02 board
Electronic load (−) → Pin 3/CN905/SP-02 board

Following the table below, set the output voltage of the DC power supply and the load current of the electronic load, and proceed to adjust.

Adjustment item	DC power supply	Electronic load (constant current)	Measuring point (SP-02 board) Cold pin in parentheses	Specifications/adjustment (SP-02 board)
Output current limiting	+8.00±0.05V	5.0A	Cathode/D205 (Heat sink for D205)	Turn ⊘RV204 counterclockwise, then rotate it slowly clockwise and stop at point where pulses vanish. Take care not to rotate ⊘RV204 too far.  (After adjustment, the power supply will stop automatically.)
Output power limiting (with max. voltage)	+8.00±0.05V	1.1A	Pin 5/CN905 (Pin 3/CN905)	+78.5±0.5Vdc ⊘RV671/C6TR board/SP-02 board
Output power limiting (with min. voltage)	+8.00±0.05V	4.4A	Pin 5/CN905 (Pin 3/CN905)	+20.0±0.2Vdc ⊘RV208
Output voltage	+5.00±0.01V	1.6A	Pin 5/CN905 (Pin 3/CN905)	+49.5±0.2Vdc ⊘RV672/C6TR board/SP-02 board

(3) CAPSTAN VH adjustmets

Connect the DC power supply and electronic load as follows.
- DC power supply (+) → Pin 3/CN903/SP-02 board
- DC power supply (−) → Pin 6/CN903/SP-02 board
- Electronic load (+) → Pin 4/CN904/SP-02 board
- Electronic load (−) → Pin 2/CN904/SP-02 board

Following the table below, set the output voltage of the DC power supply and the load current of the electronic load, and proceed to adjust.

Adjustment item	**DC power supply**	**Electronic load (constant current)**	**Measuring point (SP-02 board) Cold pin in parentheses**	**Specifications/adjustment (SP-02 board)**
Output current limiting	+8.00±0.05V	3.5A	Cathode/D207 (Heat sink for D207)	Turn ⊘RV206 counterclockwise, then rotate it slowly clockwise and stop at point where pulses vanish. Take care not to rotate ⊘RV206 too far.  (After adjustment, the power supply will stop automatically.)
Output power limiting (with max. voltage)	+8.00±0.05V	0.55A	Pin 4/CN904 (Pin 2/CN904)	+39.5±0.2Vdc ⊘RV671/C6CP board/SP-02 board
Output power limiting (with min. voltage)	+8.00±0.05V	2.2A	Pin 4/CN904 (Pin 2/CN904)	+10.0±0.1Vdc ⊘RV209
Output voltage	+5.00±0.01V	0.8A	Pin 4/CN904 (Pin 2/CN904)	+24.75±0.1Vdc ⊘RV672/C6CP board/SP-02 board

(4) DRUM VH adjustments

Connect the DC power supply and electronic load as follows.

DC power supply (+) → Pin 2/CN903/SP-02 board
DC power supply (−) → Pin 6/CN903/SP-02 board
Electronic load (+) → Pin 3/CN904/SP-02 board
Electronic load (−) → Pin 1/CN904/SP-02 board

Following the table below, set the output voltage of the DC power supply and the load current of the electronic load, and proceed to adjust.

Adjustment item	**DC power supply**	**Electronic load (constant current)**	**Measuring point (SP-02 board) Cold pin in parentheses**	**Specifications/adjustment (SP-02 board)**
Output current limiting	+8.00±0.05V	5.5A	Cathode/D209 (Heat sink for D209)	Turn ⊘RV205 counterclockwise, then rotate it slowly clockwise and stop at point where pulses vanish. Take care not to rotate ⊘RV205 too far.  (After adjustment, the power supply will stop automatically.)
Output power limiting (with max. voltage)	+8.00±0.05V	1.25A	Pin 3/CN904 (Pin 1/CN904)	+39.5±0.2Vdc ⊘RV671/C6DR board/SP-02 board
Output power limiting (with min. voltage)	+8.00±0.05V	5.0A	Pin 3/CN904 (Pin 1/CN904)	+10.0±0.1Vdc ⊘RV210
Output voltage	+5.00±0.01V	1.8A	Pin 3/CN904 (Pin 1/CN904)	+24.75±0.1Vdc ⊘RV672/C6DR board/SP-02 board

Upon completion of the adjustments, switch off the power and disconnect the DC power supply and electronic load from the SP-02 board. With the SP-02 board placed on top of the power unit, connect connectors CN903, 904 and 905 to the SP-02 board and proceed with next adjustments.

8-6. F+17V/PRE-REGULATOR ADJUSTMENTS

[Preparations]
Take out the SP-02 board from the power unit and connect all the connectors on the board. Switch on the power and set the VTR to the stop (STANDBY OFF) mode.

[Adjustments]

Adjustment item	Measuring point Cold pin in parentheses	Specifications	Adjustment
F+17V	Collector/Q209/SP-02 board (Heat sink for Q209)	+17.1±0.1Vdc	⊘RV201/SP-02 board
PRE REG	Pin 1/CN209/SP-02 board (Heat sink for D201 & D202)	+93.5±0.5Vdc	⊘RV471/C4 board/SP-02 board Turn ⊘RV471 counterclockwise, then rotate it clockwise.

After the adjustments switch off the power and return the SP-02 board to the inside of the power unit.

8-7. DT DRIVE CURRENT LIMITING ADJUSTMENT

[CAUTION] RV1 on the DD-7 board should not be touched unless either it or the DC-DC converter transformer T1 has been replaced.

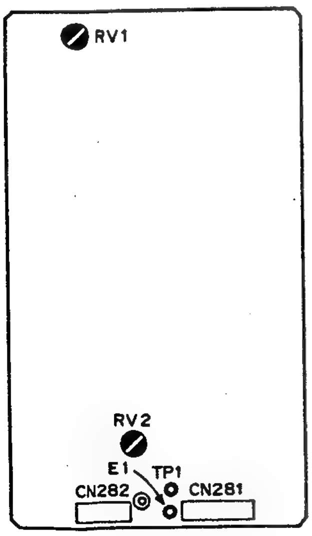
[Adjustment]
Set ⊘RV1/DD-7 board to its mechanical center point.

8-8. REG +12V ADJUSTMENT

[Preparations]
Select the PLAY head for playing back using the PLAY/IN key on the 21-key section.

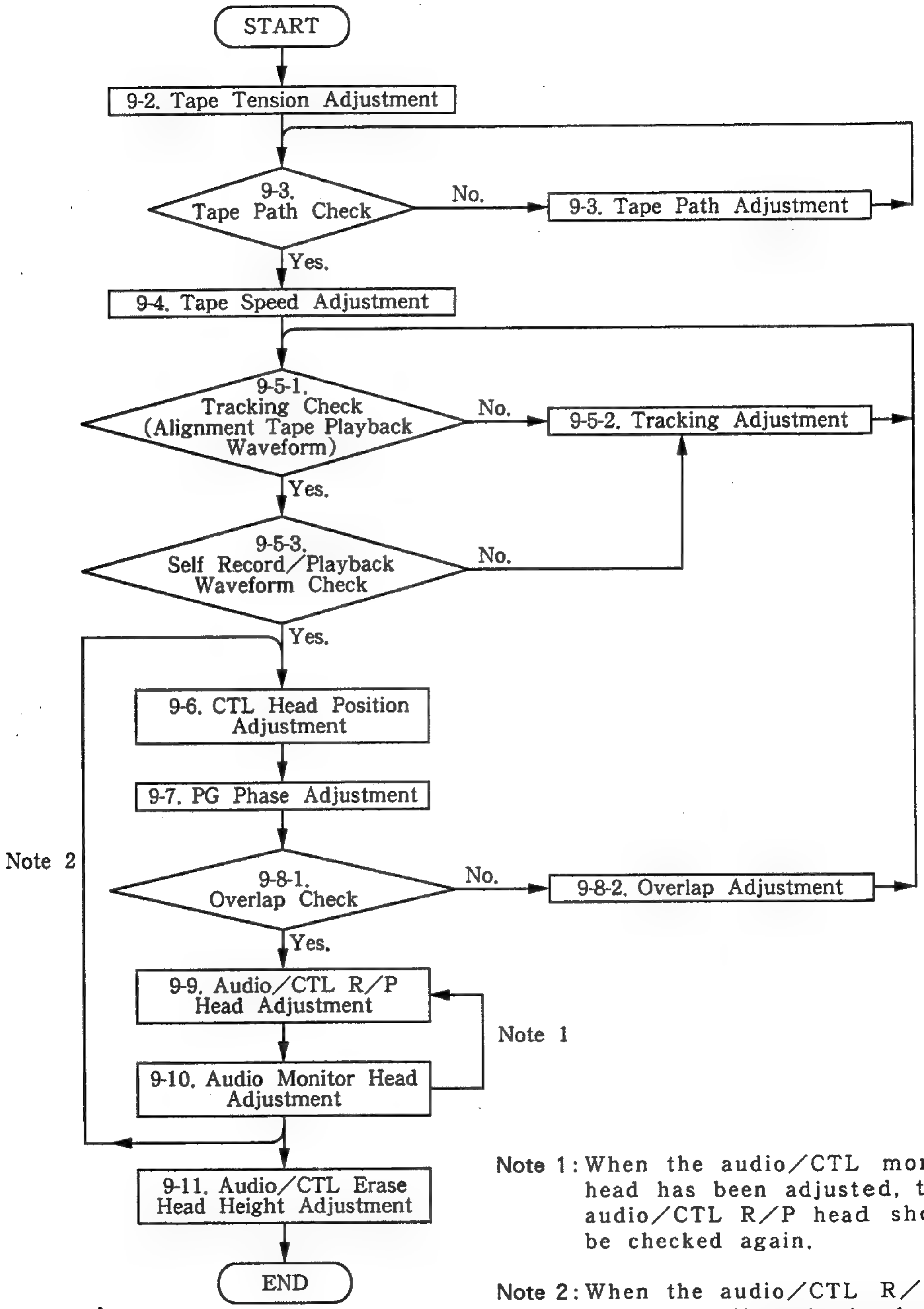
[Adjustment]
TP1/DD-7 board : +12.00±0.02Vdc
⊘RV2/DD-7 board

DD−7 Board (Component Side)



SECTION 9
TAPE PATH SYSTEM ALIGNMENT

9-1. ADJUSTMENT FLOWCHART



Note 1: When the audio/CTL monitor head has been adjusted, the audio/CTL R/P head should be checked again.

Note 2: When the audio/CTL R/P head has been adjusted, check again the CTL head position, PG phase and overlap after having adjusted the audio monitor head.

9-2. TAPE TENSION ADJUSTMENT

Preliminary Information

A. Provide the following tension adjustment tool in order to conduct the adjustments :
Sony Part No. J-6251-960-A

B. If the guide shaft is worn out, replace it with reference to Section 6-8 or shift the worn surface of the shaft for re-use.
The whole assembly should be replaced if any other component of the assembly is worn out or damaged.

Checks and Adjustments

1. Loosen the screw securing stopper (1) and move it in direction C.
2. Mount the adjustment post of the tension adjustment tool at the position shown in Fig.9-2.
3. Connect a digital voltmeter to TP22 on the SV-90 board and switch on the VTR's power.
Press $\boxed{0}$ on the 21-key section while keeping switch S2 on the SY-103 board depressed. (Alternatively, select "TTP ADJ" of the test menu T17. Reference should be made to Section 3-2.) This operation causes the following to appear on the control panel display :

>_

4. Check that the voltage at TP22 is 0±0.02V. If it is not, adjust it following the method in ⓐ.
5. Remove the adjustment post and slip the adjustment weight of the tension adjustment tool over the guide post.
6. Check that the voltage at TP22 is 0±0.02V. If it is not, loosen the two screws securing the spring holder of the tension arm so that it can be moved lightly, adjust the position of the spring holder and then tighten up the two screws.
7. Move the weight lightly and check that the voltage at TP22 is 0±0.02V when the weight comes to rest again. If the voltage differs, repeat step 6.
8. Check that the voltage at TP22 is 2.0±0.1V when the weight is removed from the tension arm. If it is not, adjust it following the method in ⓑ.
9. Attach the weight again and carry out step 7. If the voltage still does not tally, adjust it following the method in ⓐ and repeat steps 7 through 9 until both voltages are adjusted properly.

Fig.9-1. Tension Adjustment Tool

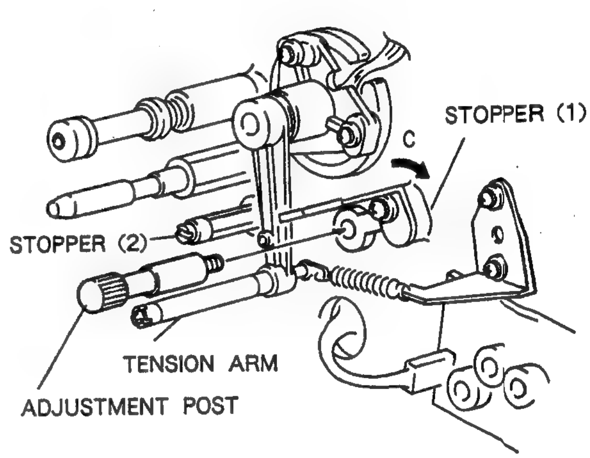


Fig.9-2. Tension Adjustment

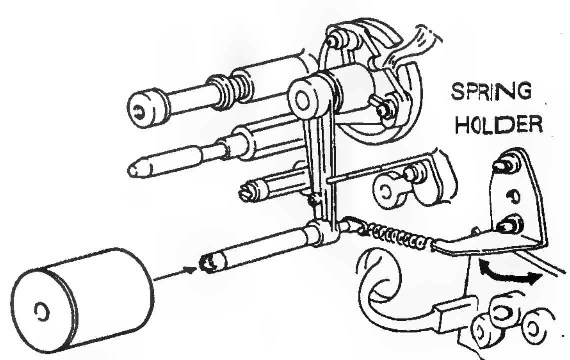


Fig.9-3. Spring Holder Position Adjustment

10. Tighten the screw so that the clearance between stopper (1) and the tension arm is brought to between 0.3 and 0.7mm.
11. The results of the above adjustments are written into the non-volatile RAM and so proceed until step 13. Press the [C], [T] and [F] keys in sequence with blue colored [OUT] on the 21-key section depressed. Next, press [SET].
This operation causes the following to appear on the control panel display :

>TEN SNS XXXX _	>NVW_
XXXX XXXX XXXX	>_

12. Press [+] on the 21-key section and keep this depressed until the following appears on the control panel display :

>XXXX XX-XX	>XXXX XX-XX
XXXX XXXX XXXX	>PUSH NVWR SW_

13. Press the NVWR switch on the SV-90 board. This operation causes the following to appear on the control panel display :

>PUSH NVWR SW_	>READY_
XXXX XXXX XXXX	>_

14. Press the [C], [0] and [SET] keys in sequence on the 21-key section.
This operation causes the following to appear on the control panel display :

>CO_	>TEST MODE OFF_
	>_

15. Press the [SET] key while keeping the blue colored [OUT] key on the 21-key section depressed. This operation causes a return to the normal operating mode.
ⓐPress the [C], [7], [0] and [SET] keys in sequence on the 21key section.
This operation causes the following to appear on the control panel display :

>C70_	>TEN SNS OFFSET_
XXXX XXXX XXXX	>_

- Press [7], [8], [9] or [IN] while keeping blue colored [OUT] on the 21-key section depressed and adjust the voltage at TP22 to 0±0.02V. In this case, [7] signifies (− −), [8](−), [9](+) and [IN] (+ +).

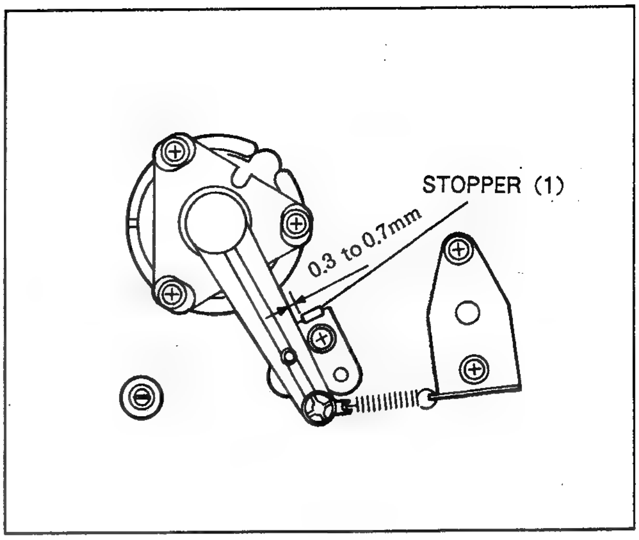


Fig.9-4. Stopper (1) Adjustment

ⓑPress the [C], [7], [1] and [SET] keys in sequence on the 21key section.
This operation causes the following to appear on the control panel display :

>C71_	>TEN SNS GAIN _
XXXX XXXX XXXX	>_

- Press [7], [8], [9] or [IN] while keeping blue colored [OUT] on the 21-key section depressed and adjust the voltage at TP22 to 2.0±0.1V. In this case, [7] signifies (− −), [8](−), [9](+) and [IN] (+ +).

9-3. TAPE PATH CHECK AND ADJUSTMENT

Preliminary Information

1. Check that the tape does not touch the reel flange too firmly and that there is no abnormal tape curling near each guide in the tape path as the tape runs in the REC, F.FWD, REV×1 programmed jog and REW modes.
2. When the height of the guides has been adjusted, first tighten up the set screws and check again.

Tape Path Check

1. Thread a tape which is free from wrinkles and damage on both edges and whose reel flanges are characterized by minimal deflection on to the reel table.
2. Set the VTR to the recording mode and check the tape path in the following locations.
   - Supply reel : The tape should barely touch the reel flange while it is running.
   - Guide post 1 : The tape should make contact with the upper flange of the guide but should barely curl at all.
   - Guide roller 1 : The tape should make contact with the lower flange of the guide but should barely curl at all.
   - Entrance and exit slant guides : The tape should not curl along the guide flanges.
   - Taper guide : The tape should make contact with the upper flange of the guide but should barely curl at all.
   - Guide post 2 : The tape should make contact with the lower flange of the guide but should barely curl at all.
   - Guide roller 2 : The tape should make contact with the upper flange of the guide but should barely curl at all.
   - Take-up reel : The tape should barely touch the reel flange while it is running.
3. If the tape path fails to satisfy the above conditions, adjustment should be made following the required procedure.
4. Check that there is no abnormal tape curling in the F.FWD, REV×1 programmed jog and REW modes, in that order.

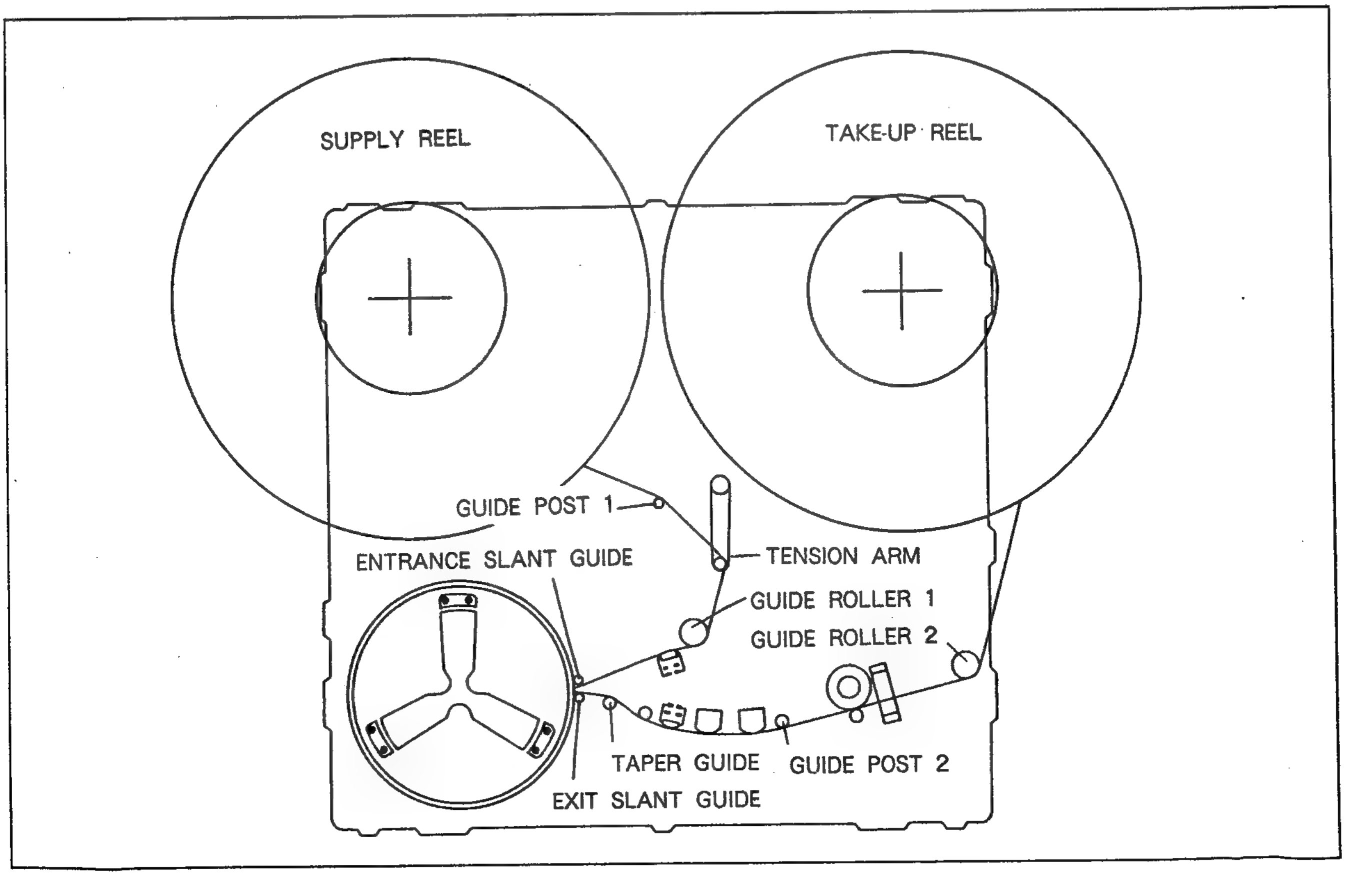


Fig.9-5. Tape Path Check

Guide Height Adjustment

The heights of the guides are shown in Fig.9-6. When a part is to be replaced, first adjust the height beforehand to the value shown below and then proceed with the mounting.

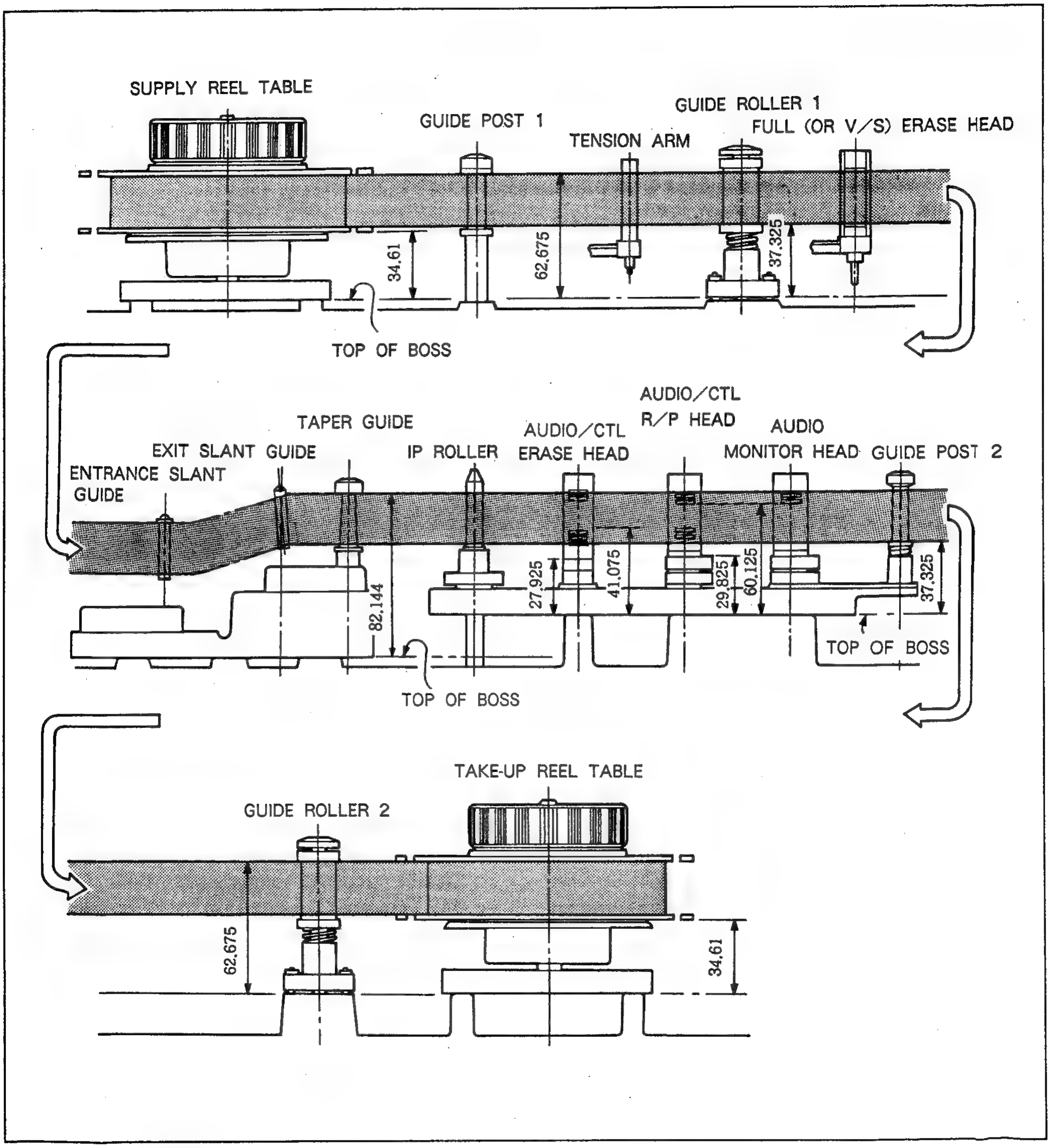


Fig.9-6. Guide Heights

Supply and Take-up Reel Table Height Adjustment

1. Remove the cover.
2. Loosen setscrews A and B.
3. To adjust the height of the reel table, adjust setscrew C while pushing the reel table lightly in the direction of the arrow in the figure.
   Note 1 : Adjust the height of the reel table so that the tape will run without touching the reel flange.
   Note 2 : Refer to Fig.9-6 for the height from the reel sheet to the top of the boss mounted on the reel motor.
4. While pushing the reel table lightly in the direction of the arrow in the figure, tighten up setscrews A and B and replace the cover.

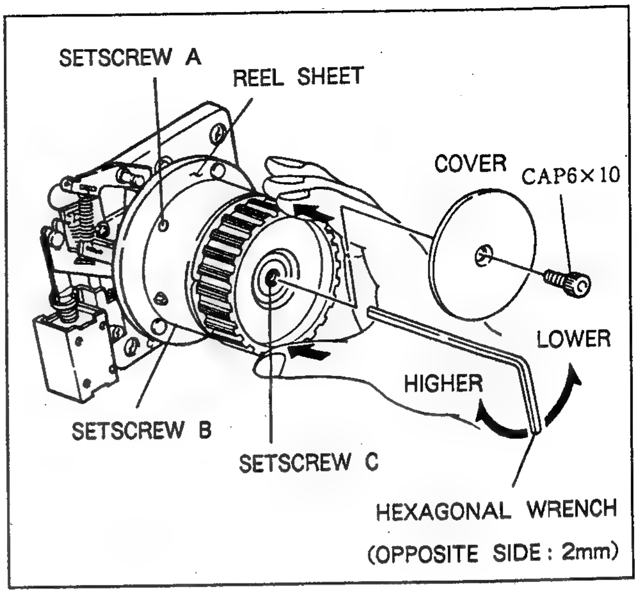


Fig.9-7. Reel Table Height Adjustment

Guide Roller 1 Height Adjustment

Note 1 : Guide roller 1 serves as the reference for the tape path height. It should not be adjusted for normal tape path adjustments.

Note 2 : Guide roller 1 is adjusted with guide post 1 and the supply reel table so that in the recording mode the tape will touch the GR lower flange lightly with hardly any curling. Check that there is no abnormal curling in the other modes.

Note 3 : When guide roller 1 is replaced as an assembly, its height is not adjusted. Instead, proceed to adjust the tape path according to the method in Note 2.

Note 4 : When guide roller 1 has been disassembled and its bearing or any other parts have been replaced, refer to Fig.9-6 and first adjust the height beforehand according to the method below before replacing the parts.

1. Loosen the setscrew.
2. Adjust the height of the guide roller by rotating the GR cap.
3. Tighten up the setscrew.
   Note: When the setscrew is tightened up, the height will be changed if the cap is allowed to rotate. Tighten up the setscrew, therefore, taking care that the cap does not rotate.
4. Check the height again.

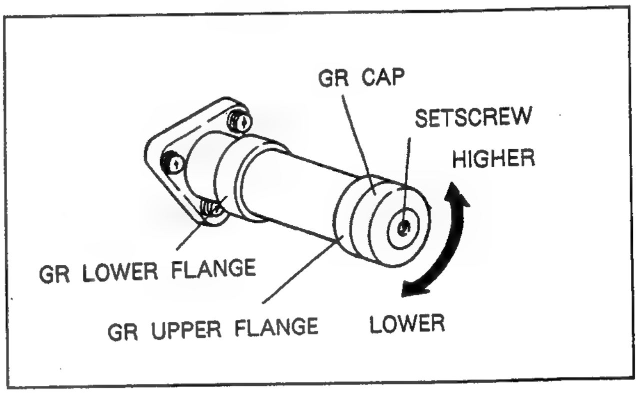


Fig.9-8. Guide Roller 1 and 2 Height Adjustment

Guide Roller 2 Height Adjustment

Note 1 : When proceeding with normal tape path adjustments, this guide roller should not be adjusted unless absolutely necessary. Adjustment should be made finely when it is not possible to eliminate the curling at guide roller 2.

Note 2 : When guide roller 2 is to be replaced, refer to Fig.9-6, adjust the height of the roller beforehand and then replace it.

1. Loosen the setscrew.
2. Adjust the height of the guide roller by rotating the GR cap.
   Note : Adjust guide roller 2 so that in the recording mode the tape will make light contact with the GR upper flange with hardly any curling as it runs. Also check that there is no abnormal curling in the other modes.
3. Tighten up the setscrew.
   Note : When the setscrew is tightened up, the height will be changed if the cap is allowed to rotate. Tighten up the setscrew, therefore, taking care that the cap does not rotate.
4. Check the height again.

Guide Post 1 Height Adjustment

Note : When replacing this guide post, refer to Fig. 9-6, adjust its height beforehand and then replace.

1. Loosen the setscrew.
2. Set the VTR to the recording mode. Adjust the height of the guide post by rotating the cap so that the tape will make light contact with the upper flange of this post with hardly any curling. Also check that there is no abnormal curling in the other modes.
3. Tighten up the setscrew.
   Note : When the setscrew is tightened up, the height of guide post 1 will be changed if the cap is allowed to rotate. Tighten up the setscrew, therefore, taking care that the cap does not rotate.
4. Check the tape path again.

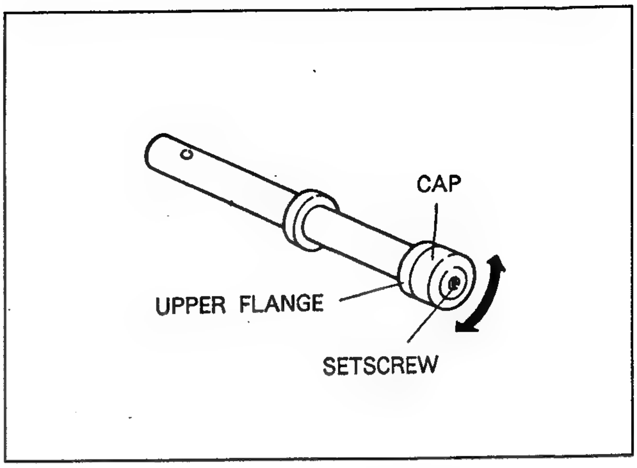


Fig.9-9. Guide Post 1 Height Adjustment

Taper Guide Height Adjustment

Note : In this tape path section, there is no particular need for this adjustment unless the tape curls at the guide flange area. The final height adjustment should be performed with the tracking adjustment in Section 9-5.

1. Loosen the setscrew on the top of the taper guide.
2. Rotate the cap of the taper guide so that the tape does not curl when the VTR is set to the recording mode.
3. Tighten up the setscrew.
   Note : When the setscrew is tightened up, the height of the taper guide will be changed if the cap is allowed to rotate. Tighten up the setscrew, therefore, taking care that the cap does not rotate.
4. Check the tape path again.

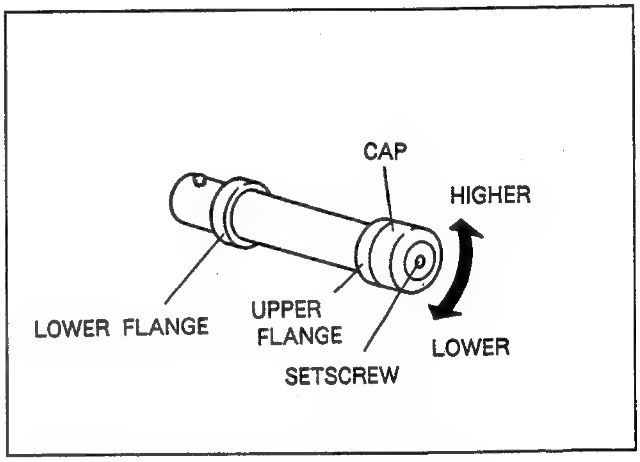


Fig.9-10. Taper Guide Height Adjustment

Guide Post 2 Height Adjustment

Note : When replacing a component part of this guide post, refer to Section 6-12.

1. Loosen the setscrew.
2. Set the VTR to the recording mode. Adjust the height of the guide post by rotating the cap so that the tape will make light contact with the lower flange of this post with hardly any curling. Also check that there is no abnormal curling in the other modes.
3. Tighten up the setscrew.
   Note : When the setscrew is tightened up, the height of guide post 2 will be changed if the cap is allowed to rotate. Tighten up the setscrew, therefore, taking care that the cap does not rotate.
4. Check the tape path again.

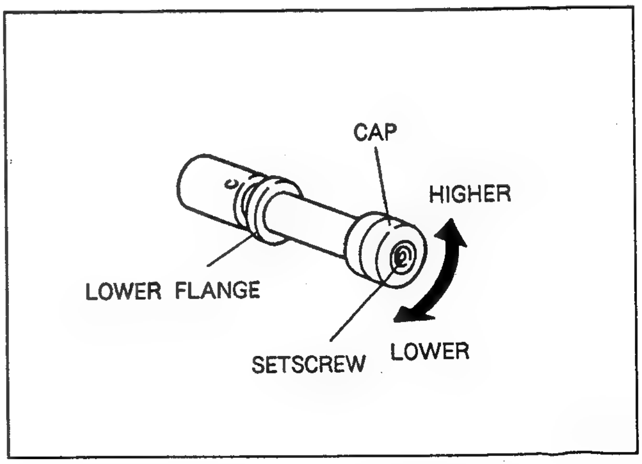


Fig.9-11. Guide Post 2 Height Adjustment

9-4. CAPSTAN SERVO ADJUSTMENT

Preliminary Information

A. In this section, the capstan lock time (playback mode) is adjusted in the specifications.

B. This adjustment is required only when the capstan motor has been replaced.

C. Adjust the constant of the servo system so that the frequency of the FG pulses generated by the capstan motor will be set to the reference frequency.

FG Duty Cycle Adjustment

1. Press [0] on the 21-key section while keeping switch S2 on the SY-103 board depressed. (Alternatively, select "TTP ADJ" of the test menu T17. Reference should be made to Section 3-2.) This operation causes the following to appear on the control panel display :

	>_

2. Press [F], [8] and [SET] in sequence on the 21-key section. This operation causes the capstan to rotate. Next, while keeping the blue [OUT] key depressed, press the blue [IN] key untill the following display appears on the control panel. This operation causes the FG duty cycle to be adjusted to 50%.

	>F8 CFG ADJ _
D5D5 XXXX XXXX	>_

Spec. : D5±2 (D3 to D7)

Check that the display is within the specifications.

3. Press [F], [3] and [SET] in sequence on the 21-key section.
This operation causes the capstan to stop rotating and the following to appear on the control panel display :

>F8 CFG ADJ_	>F3 STOP_
XXXX XXXXXXXXXX	>_

4. The results of the above adjustments are written into the non-volatile RAM and so proceed until step 6. Press the [C], [T] and [F] keys in sequence with blue colored [OUT] on the 21-key section depressed. Next, press [SET].
This operation causes the following to appear on the control panel display :

>F3 STOP_	>NVW_
XXXX XXXXXXXXXX	>XXXX XX-XX

5. Press [+] on the 21-key section and keep this depressed until the following appears on the control panel display.

>XXXX XX-XX	>XXXX XX-XX
XXXX XXXX XXXX	>PUSH NVWR SW_

6. Press the NVWR switch on the SV-90 board. This operation causes the following to appear on the control panel display :

>PUSH NVWR SW_	>READY_
XXXX XXXX XXXX	>_

7. Press the RESET switch on the SV-90 board or alternatively switch off the VTR's power temporarily.

Capstan Free Speed Adjustment

8. Thread a general-purpose tape and switch on the power if it was off. Now set the VTR to the playback mode.
9. Proceed in the same way as for step 1.
10. Press $\boxed{C}$, $\boxed{C}$, $\boxed{0}$ and $\boxed{SET}$ in sequence on the 21-key section. This operation causes the following to appear on the control panel display :

```
>CCO_                          >CAP SPEED ADJ _
    0FA0 XXXX XXXX             >_
```

Spec. : 0FA0±5 (0F9B to 0FA5)

Check that the display is within the specifications. If it is not, adjust by pressing $\boxed{IN}$ while keeping blue colored $\boxed{OUT}$ on the 21-key section depressed.

11. Set the VTR to the stop mode (STANDBY OFF).
12. The results of the above adjustments are written into the non-volatile RAM and so proceed until step 14. Press the $\boxed{C}$, $\boxed{T}$ and $\boxed{F}$ keys in sequence with blue colored $\boxed{OUT}$ on the 21-key section depressed. Next, press $\boxed{SET}$.
This operation causes the following to appear on the control panel display :

```
>CAP SPEED ADJ_                >NVW_
    XXXX XXXX XXXX             >_
```

13. Press $\boxed{+}$ on the 21-key section and keep this depressed until the following appears on the control panel display :

```
>XXXX XX-XX                    >XXXX XX-XX
    XXXX XXXX XXXX             >PUSH NVWR SW_
```

14. Press the NVWR switch on the SV-90 board.
This operation causes the following to appear on the control panel display :

```
>PUSH NVWR SW_                 >READY_
    XXXX XXXX XXXX             >_
```

15. Press $\boxed{C}$, $\boxed{0}$ and $\boxed{SET}$ in sequence on the 21-key section.
This operation causes the following to appear on the control panel display :

```
>CO_                           >TEST MODE OFF_
                               >_
```

16. Press $\boxed{SET}$ on the 21-key section while keeping blue colored $\boxed{OUT}$ depressed. This operation causes a return to the normal operating mode.

9-5. TRACKING ADJUSTMENT

9-5-1. Tracking Check (Alignment Tape Playback Waveform Check)

When the upper drum has been replaced, run a tape in the playback or recording mode for about 20 minutes in order to get a good head-to-tape touch before performing the tracking check.

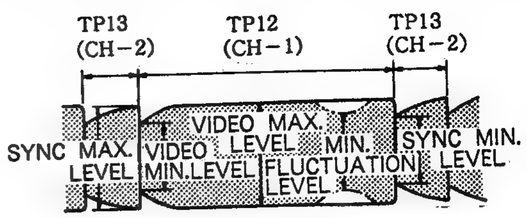
1. Press [0] on the 21-key section while keeping switch S2 on the SY-103 board depressed. (Alternatively, select "TTP ADJ" of the test menu T17. Reference should be made to Section 3-2.) This operation causes the following to appear on the control panel display :

```
                 >_
```

2. Press [C], [8], [0] and [SET] in sequence on the 21-key section. This operation causes the following to appear on the control panel display :

```
>C80_                    >TRACKING ADJ_
     XXXX XXXX XXXX      >_
```

3. Connect TP12 on the VO-16 board to CH-1 of the oscilloscope and connect TP13 to CH-2. (CH-2 is not connected for the BVH-3100).
4. Play back the "WHITE" section of the alignment tape and adjust the TRACKING control so that the RF amplitude is set to its maximum level.
5. Check that the video and sync RF waveforms satisfy the specifications in Fig.9-12. If they do not, the tracking must be adjusted.



VIDEO RF (CH-1) $\frac{\text{VIDEO MIN. LEVEL}}{\text{VIDEO MAX. LEVEL}} \times 100 \geq 80\%$

SYNC RF (CH-2) $\frac{\text{SYNC MIN. LEVEL}}{\text{SYNC MAX. LEVEL}} \times 100 \geq 70\%$

(BVH-3000 ONLY)

Fig.9-12. Alignment Tape Playback Waveform Check

9-5-2. Tracking Adjustment

Preliminary Information

A. This adjustment is conducted in order to make the head trace the recorded pattern of the alignment tape correctly and to bring the heads into contact with the tape properly so that tape interchangeability is maintained.

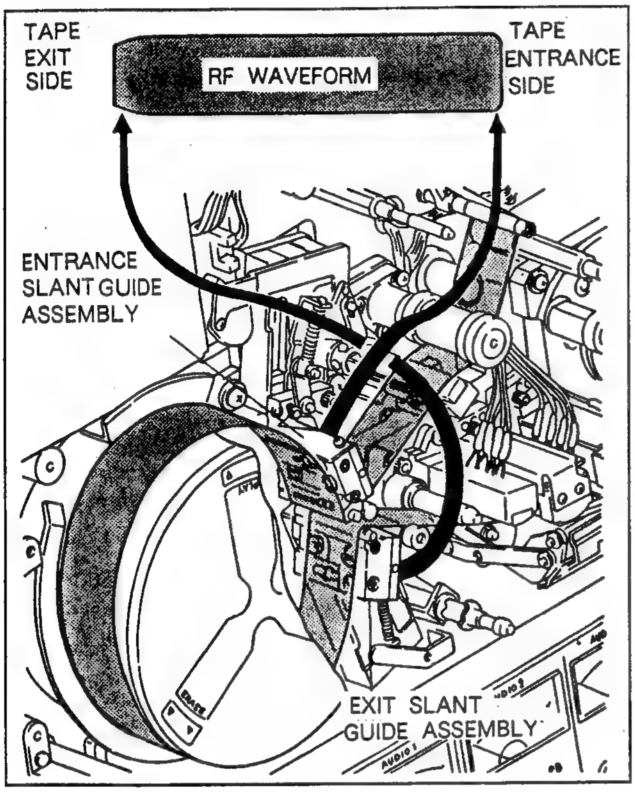


Fig.9-13. Tracking Adjustment

B. Adjustment points
- The RF waveform at the tape entrance side must be adjusted first. Then proceed to adjust the RF waveform at the tape exit side.
- Before rotating the adjustment screw of the slant guide, press the tape lightly with your finger and check the direction in which the slant guide should move. When touching the tape, be sure to touch the back-coated surface and not the magnetized surface.
- Refer to Fig.9-14 and 9-15 for the relationship between the rotation direction of the adjustment screw and the movement direction of the slant guide.
- The height of the taper guide should be adjusted while the RF waveform is being checked at the same time as the height of the exit slant guide is adjusted.

C. Use a Phillips head screwdriver for M3 screws in order to adjust the adjustment screw of the slant guide.

D. If the tracking cannot be correctly adjusted due to wear of the entrance slant guide, exit slant guide or tape guide section of the head drum assembly, replace the worn parts in accordance with the sections below.

Head drum assembly :	Section 6-2
Entrance slant guide assembly :	Section 6-4-1
Exit slant guide assembly :	Section 6-4-2

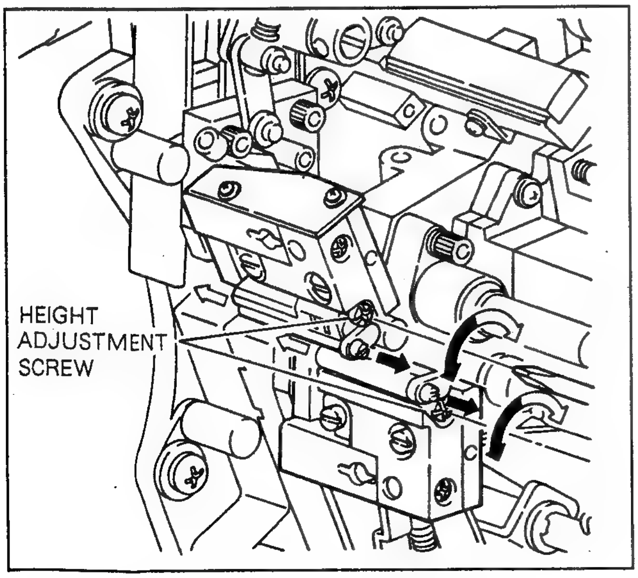


Fig.9-14. Slant Guide Height Adjustment

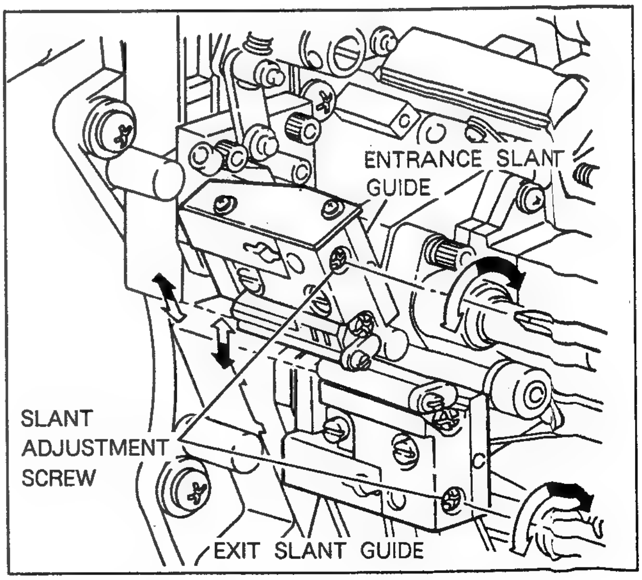


Fig.9-15. Slanting Adjustment of Slant Guide

Adjustment

1. Follow the procedure below to check the clearance between the upper part of the guide bracket of the entrance slant guide assembly and upper drum.
   a. Loosen the two screws securing the fence and retract the fence in direction A shown in the figure.
   b. Check the clearance between the upper part of the guide bracket of the entrance slant guide assembly and upper drum as follows.
      Thickness gauge with a 0.09mm thickness passes through.
      Thickness gauge with a 0.13mm thickness does not pass through.
   If the above clearances are satisfied, proceed to step i. If not, adjust as follows.
   c. Loosen screw N by one-half to one full turn. Screw M must not be loosened.
   d. When the clearance is too small: First rotate setscrew ② counterclockwise and then rotate setscrew ① clockwise to adjust the clearance.
   When the clearance is too grate: First rotate setscrew ① counterclockwise and then rotate setscrew ② clockwise to adjust the clearance.
   e. Tighten up screws N and M.
   f. Rotate the upper drum by hand so that the head is distanced from the entrance slant guide assembly.
   g. Use the thickness gauge to check the clearance between the upper part of the guide bracket and upper drum.
   h. Rotate setscrews ① and ② so that they rest lightly on the guide holder and apply adhesive to them (paint-lock them).
   i. Adjust the clearance between the fence and upper drum to 0.15±0.05mm and tighten up the two screws.
2. Follow the procedures below to check the clearance between the upper drum and guide post and 1mm underneath the guide flange of the exit slant guide.
   a. Thickness gauge with a 0.08mm thickness passes through.
   b. Thickness gauge with a 0.10mm thickness does not pass through.
   If the above clearances are not satisfied, adjust as follows:
   c. Loosen screw N by one-half to one full turn. Screw M must not be loosened.
   d. When the clearance is too small: First rotate setscrew ② counterclockwise and then rotate setscrew ① clockwise to adjust the clearance.
   When the clearance is too great: First rotate setscrew ① counterclockwise and then rotate setscrew ② clockwise to adjust the clearance.

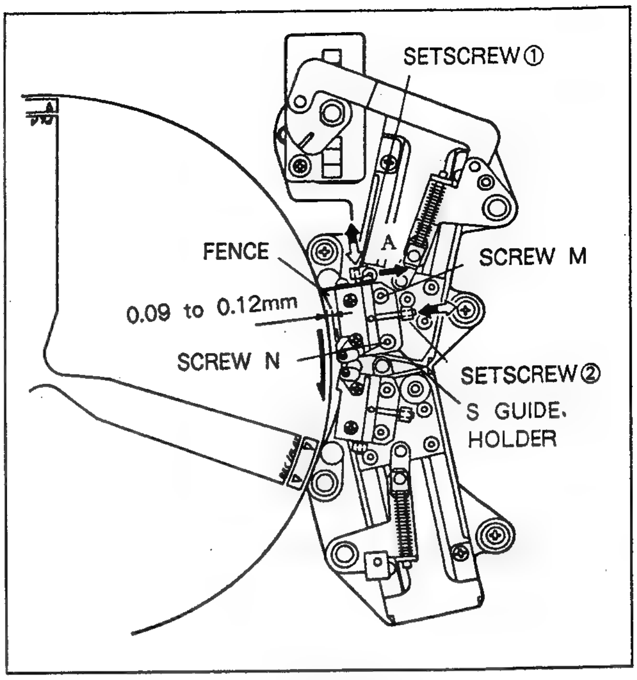


Fig.9-16. Entrance Slant Guide/Upper Drum Clearance Adjustment

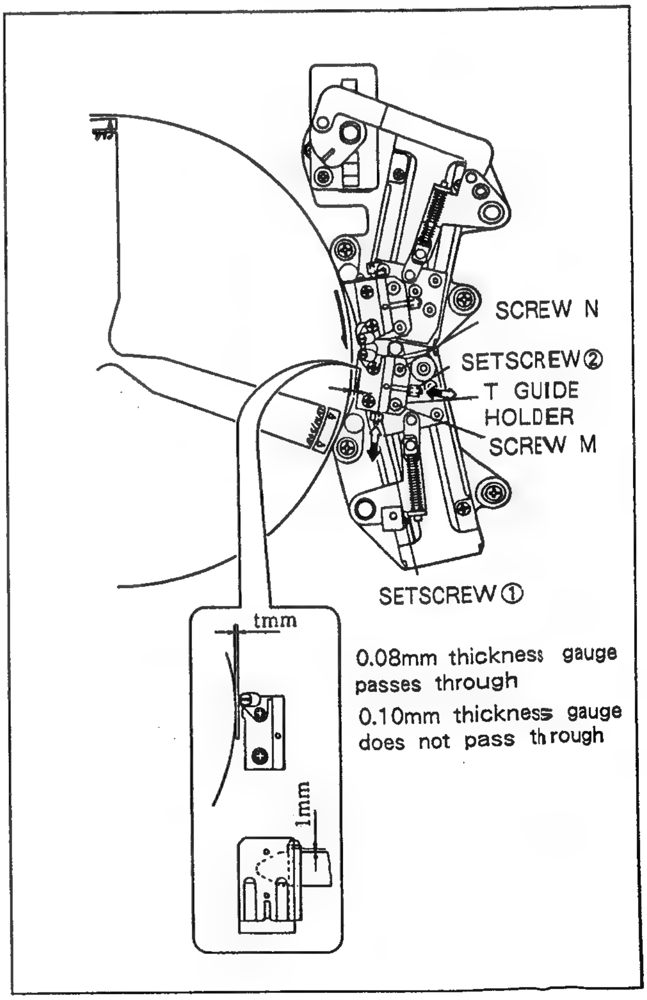


Fig.9-17. Exit Slant Guide/Upper Drum Clearance Adjustment

e. Tighten up screws N and M.
f. Rotate the upper drum by hand so that the head is distanced from the exit slant guide assembly.
g. Use the thickness gauge to check the clearance between the guide flange of the exit slant guide assembly and upper drum.
h. Rotate setscrews ① and ② so that they rest lightly on the guide holder and apply adhesive to them (paint-lock them).

3. Press [0] on the 21-key section while keeping switch S2 on the SY-103 board depressed. (Alternatively, select "TTP ADJ" of the test menu T17. Reference should be made to Section 3-2.) This operation causes the following to appear on the control panel display :

>_

4. Press [C], [8], [0] and [SET] in sequence on the 21-key section. This operation causes the following to appear on the control panel display :

>C80_	>TRACKING ADJ_
XXXX XXXX XXXX	>_

5. Connect CH-1 of an oscilloscope to TP12 on the VO-16 board.
6. Play back the "WHITE" section of the alignment tape.
7. Rotate the TRACKING control counterclockwise and adjust it so that the RF amplitude is set to 4/5 of its maximum level.

Entrance Slant Guide Adjustment

8. Check that, as in Fig.9-20 (a), the RF amplitude at the tape entrance side drops by 10% to 20% when the height adjustment screw of the entrance slant guide is rotated about 180° in the counterclockwise direction. If it does not, adjust the slant adjustment screw of the slant guide as follows.
   a. Press the top or bottom edge of the tape while it is running, as shown in Fig.9-18, and find the edge where the RF waveform becomes flat as in Fig.9-20 (a).
   b. If the RF waveform flattens when the bottom edge of the tape is pushed, rotate the slant adjustment screw counterclockwise ; if the waveform flattens when the top edge of the tape is pushed, rotate the screw clockwise.
9. Rotate the height adjustment screw of the entrance slant guide slowly clockwise and, as in Fig.9-20 (b), adjust it so that the RF waveform at the tape entrance side is made flat and its fluctuations are minimized.
10. Check that the RF waveform at the tape entrance side changes virtually in parallel when the TRACKING control is rotated CCW and CW.
11. Check that the tape does not curl at the guide flange section. Check that the heads of the height and slant adjustment screws do not project or sit below the surface A of the entrance slant guide assembly to an abnormal extent.

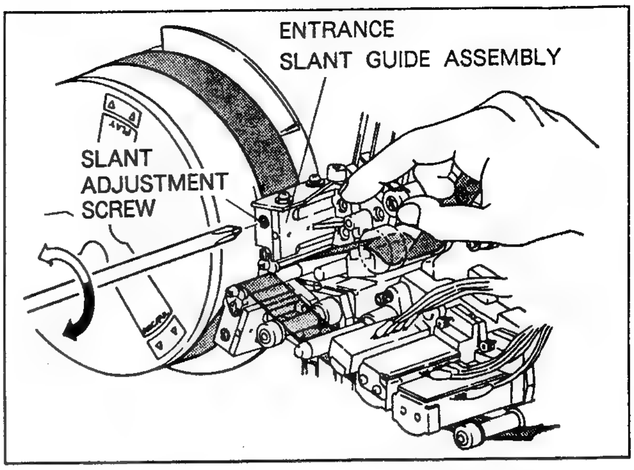


Fig.9-18. Slant Adjustment of Entrance Slant Guide

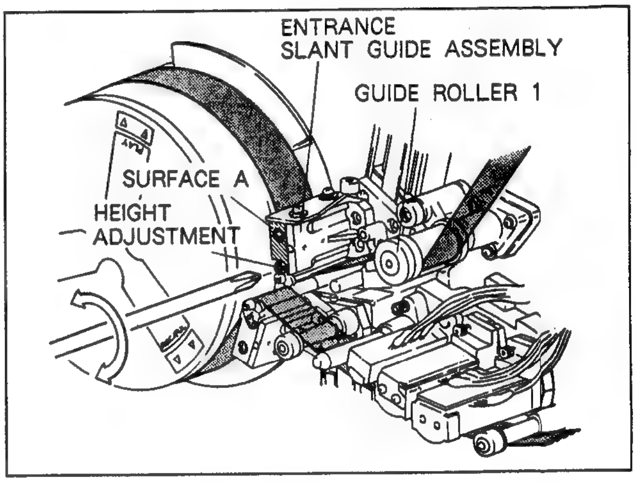


Fig.9-19. Height Adjustment of Entrance Slant Guide

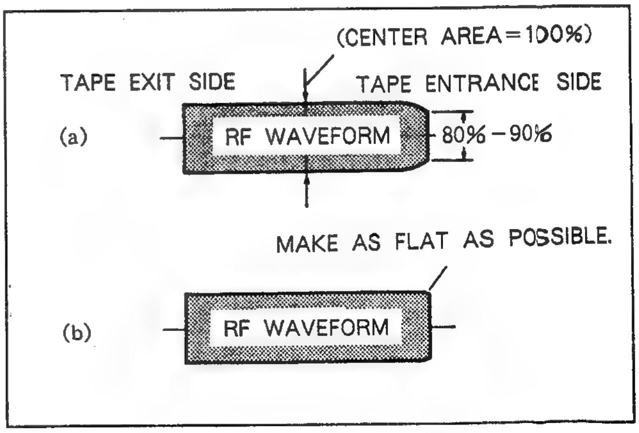
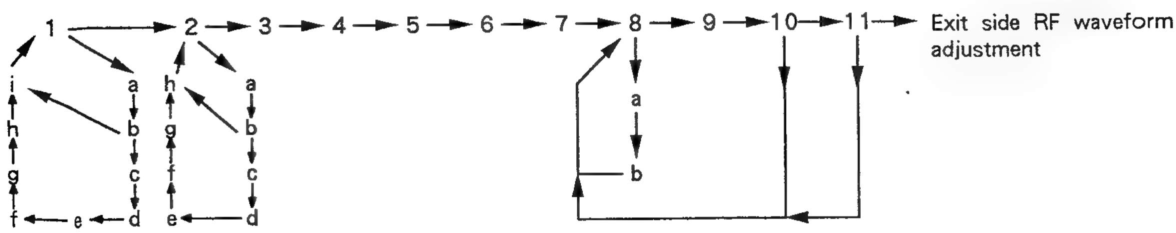


Fig.9-20. Entrance Side RF Waveform Adjustment

Reference : The steps taken to adjust the RF waveform at the tape entrance side are indicated below in the form of a flowchart :



Exit Slant Guide and Taper Guide Adjustment

12. Rotate the TRACKING control counterclockwise and adjust it so that the RF amplitude is 4/5 of its maximum level.
13. Loosen the taper guide setscrew and rotate the cap 90° counterclockwise.
14. Check that the RF waveform appears as in Fig. 9-21 (a) when the height adjustment screw of the exit slant guide is rotated about 180° in the counterclockwise direction. If it does not, adjust the slant adjustment screw of the exit slant guide as follows.
    a. Press the top or bottom edge of the tape while it is running, as shown in Fig.9-21, and find the edge whose RF waveform becomes flat as in Fig.9-21 (a).
    b. If the RF waveform appears as shown in Fig. 9-21 (a) when the bottom edge of the tape is pushed, rotate the slant adjustment screw of the exit slant guide counterclockwise; if the waveform appears as in Fig.9-21 (a) when the top edge of the tape is pushed, rotate the screw clockwise.
15. Rotate the cap of the taper guide slowly clockwise, adjust the RF waveform so that it appears as in Fig.9-21 (b) and tighten up the setscrew on the cap.
16. Rotate the height adjustment screw of the exit slant guide slowly clockwise and, as in Fig.9-21 (c), adjust it so that the RF waveform at the tape exit side is made as flat as possible.
17. Check that the RF waveform changes virtually in parallel when the TRACKING control is rotated CCW and CW.
18. Check that the tape does not curl at the guide flange section and that it hardly curls at all at the upper flange section of the taper guide. Check that the heads of the slant and height adjustment screws do not project or sit below surface B of the exit slant guide assembly to an abnormal extent.

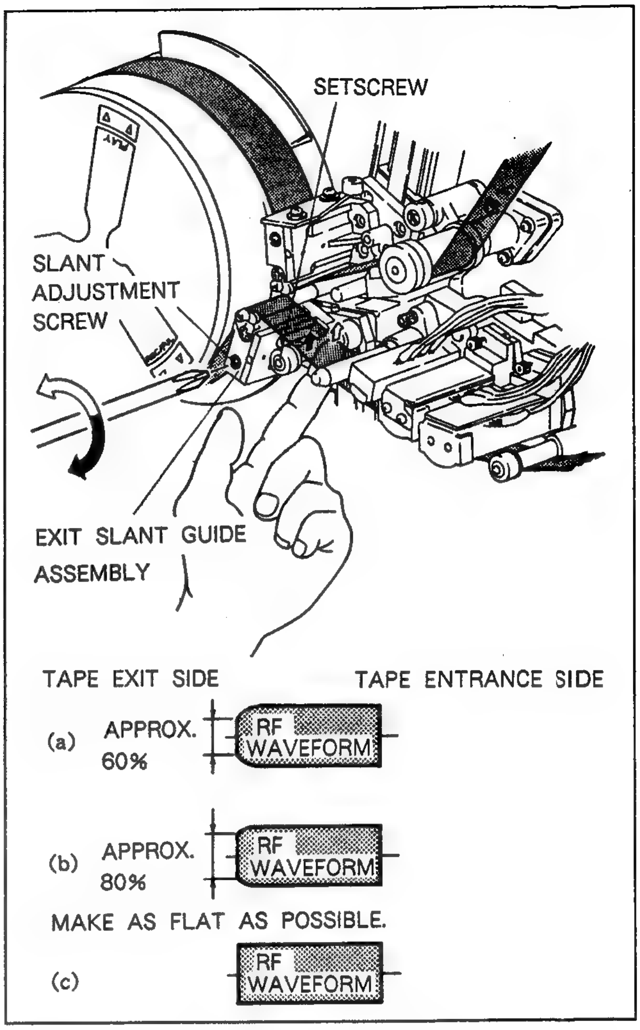


Fig.9-21. Taper Guide Height and Exit Slant Guide Slanting Adjustment

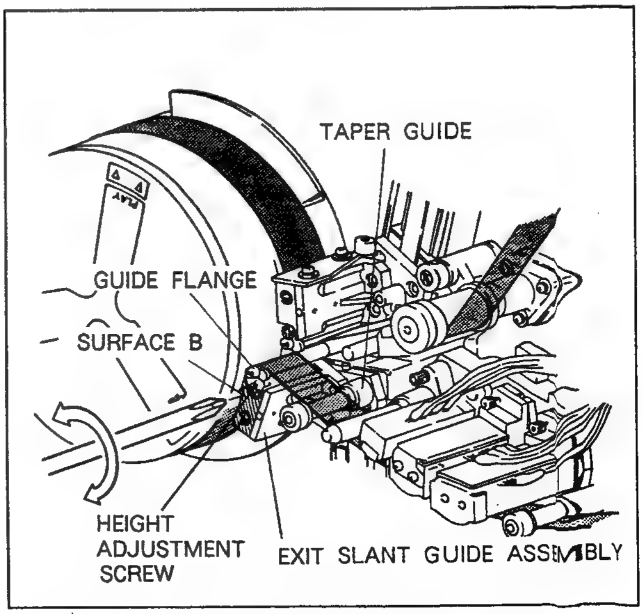


Fig.9-22. Exit Slant Guide Height Adjustment

Checks after Adjustment

19. Thread a recorded tape
    Note: Use a worn-out tape since the tape may be damaged.
20. Set the VTR to the STANDBY ON mode and then to the STANDBY OFF mode at the point when the moving guide has closed.
21. Set the tape running onto the guide flange of the exit slant guide by about 1mm and then tighten the tape by rotating the take-up reel table by hand.
22. Set the VTR to the playback mode and check that the tape, which was forced to run onto the guide flange, has now been restored naturally to normal tape run. If it has not, check out the following.
    a. Is the tape tension correct?
    b. Does the guide flange press too strongly against the tape?
    c. Is the slant of the slant guide correct?
23. Press C, 0 and SET of the 21-key section in sequence.
    This operations causes the following to appear on the control panel display:

```
>CO_                    >TEST MODE OFF_
                        >_
```

24. Press SET while keeping blue colored OUT on the 21-key section depressed. This operation causes a return to the normal operating mode.

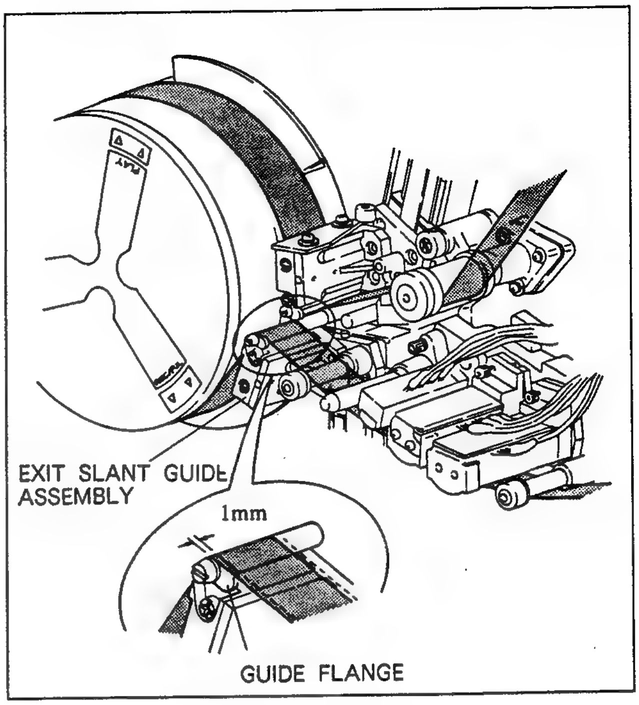
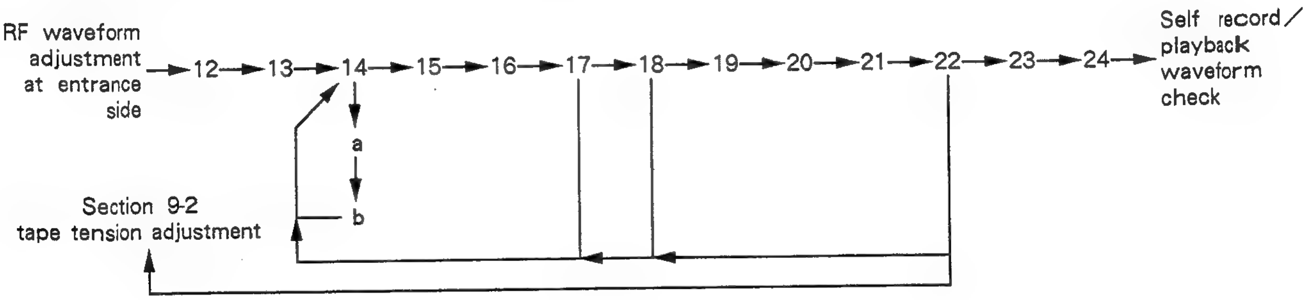


Fig.9-23. Check of Tape Running onto Guide Flange

Reference: The sequence of the adjustment steps for the RF waveform on the tape exit side is as follows:



9-5-3. Self Record/Playback Waveform Check

Preliminary Information

Check the contact between the tape and rotary heads by observing the self record/playback RF waveforms.

Check

1. Connect the oscilloscope to TP12 on the VO-16 board.
2. Press [0] on the 21-key section while keeping switch S2 on the SY-103 board depressed. (Alternatively, select "TTP ADJ" of the test menu T17. Reference should be made to Section 3-2.) This operation causes the following to appear on the control panel display :

>_

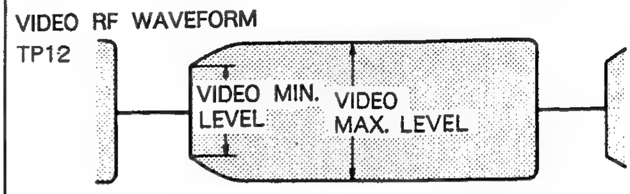
3. Press [C], [8], [0] and [SET] in sequence on the 21-key section. This operation causes the following to appear on the control panel display :

>C80_	>TRACKING ADJ_
XXXX XXXX XXXX	>_

4. Thread a general-purpose tape and record a video signal.
5. Play back the recorded segment and confirm that the RF waveform satisfies the specifications shown in Fig.9-24. If it does not, adjust the tracking again. The tracking adjustment should be performed so that the playback waveform of the alignment tape and the self record/playback waveform satisfy the specifications at the same time.
6. Press [C], [0] and [SET] in sequence on the 21-key section. This operation causes the following to appear on the control panel display :

>C0_	>TEST MODE OFF_
	>_

7. Press [SET] on the 21-key section while keeping blue colored [OUT] depressed. This operation causes a return to the normal operating mode.



$$\frac{\text{VIDEO MIN. LEVEL}}{\text{VIDEO MAX. LEVEL}} \times 100 \geqq 85\ \%$$

Fig.9-24. Self Record/Playback Waveform Check

9-6. CTL HEAD POSITION ADJUSTMENT

Preliminary Information

A. The objective of this adjustment is to maintain tape compatibility by aligning the distance of the video head and CTL head in the longitudinal direction with respect to the recorded pattern on the alignment tape.

B. The PG phase varies greatly when the CTL head is moved, and so the PG phase must always be adjusted after the CTL head has been adjusted.

Checks

1. Press [0] on the 21-key section while keeping switch S2 on the SY-103 board depressed. (Alternatively, select "TTP ADJ" of the test menu T17. Reference should be made to Section 3-2.) This operation causes the following to appear on the control panel display :

```
                    >_
```

2. Press [C], [8], [1] and [SET] in sequence on the 21-key section. This operation causes the following to appear on the control panel display :

```
>C81_                 >CTL ADJ _
   XXXX XXXX XXXX     >_
```

3. Connect the oscilloscope to TP12 on the VO-16 board.
4. Thread the alignment tape and play back the "WHITE" section.
5. Adjust the TRACKING control so that the RF amplitude is brought to its maximum and, at this maximum position, check that the RF amplitude does not change even when the TRACKING control is pushed in. If it changes, the following adjustment must be conducted.

Adjustment

6. Loosen the three screws securing the head base by one-fourth to one-half turn.
7. Check that the TRACKING control has been pushed in and then play back the "WHITE" section of the alignment tape.
8. Insert the hexagonal screwdriver (2.5mm to the opposite side) into the hole shown in Fig.9-25. Move the screwdriver as shown in the figure and set the RF amplitude to its maximum level.
9. Pull the TRACKING control and check that the RF amplitude does not change when the control is pushed in where the RF amplitude is at its maximum. If it changes, repeat steps 6 through 8.

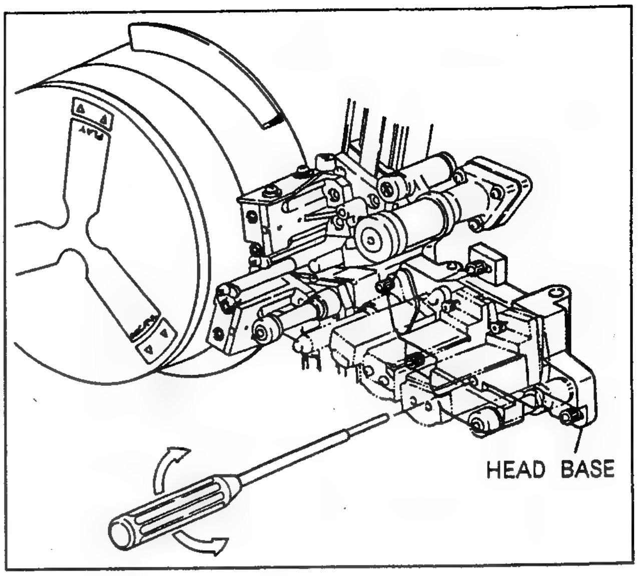


Fig.9-25. CTL Head Position Adjustment

10. Tighten the three screws which were loosened in step 6.
11. Check again.
12. Press the [C], [0] and [SET] keys in sequence on the 21-key section.
    This operation causes the following to appear on the control panel display :

```
>C0_                  >TEST MODE OFF_
                      >_
```

13. Press [SET] while keeping blue colored [OUT] on the 21-key section depressed. This operation causes a return to the normal operating mode.

9-7. PG PHASE ADJUSTMENT

Preliminary Information

A. The objective of this adjustment is to maintain tape compatibility by adjusting the phase of the video head in the track direction with respect to the recorded pattern of the alignment tape.

B. Adjustment must be made from the R/P head side. The play head side should then be adjusted.

C. This adjustment must be performed when the CTL head has been moved.

9-7-1. Playback with R/P Head

Check

1. Connect CH-1 of the oscilloscope to the video input signal (VIDEO IN connector) on the VS-30 connector panel and CH-2 to the WFM MONITOR OUTPUT (or VIDEO MONITOR OUTPUT).
2. Press [0] on the 21-key section while keeping switch S2 on the SY-103 board depressed. (Alternatively, select "TTP ADJ" of the test menu T17. Reference should be made to Section 3-2.) This operation causes the following to appear on the control panel display :

	>_

3. Press [C], [9], [0] and [SET] in sequence on the 21-key section. This operation causes the following to appear on the control panel display :

>C90_	>PG ADJ_
XXXX XXXX XXXX	>_

The R/P head is now selected and the DEMOD OUT signal is output from the MONITOR OUT (WFM) connector.

4. Thread the alignment tape and play it back.
5. Check that the phase difference between VIDEO IN (CH-1) and DEMOD OUT (CH-2) signals is within $1 \pm 1\ \mu$sec. The DEMOD OUT signal should be delayed.
   If it is not within this value, conduct the following adjustment.

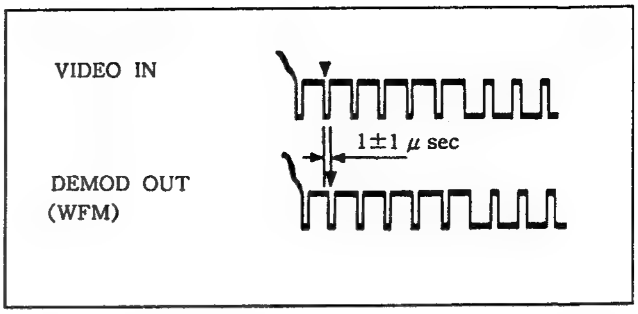


Fig.9-26. Phase Check During R/P Head Playback

Adjustment

6. Adjust the phase difference between VIDEO IN and DEMOD OUT to within $1 \pm 1\ \mu$sec as follows.
   a. When the DEMOD OUT signal is ahead, press [9] or blue [IN] while keeping blue [OUT] on the 21-key section depressed. [9] provides slow forwarding and [IN] fast forwarding. When kept depressed, continuous forwarding results.
   b. When the DEMOD OUT signal is delayed, press [7] or [8] while keeping blue [OUT] on the 21-key section depressed. [8] provides slow forwarding and [7] fast forwarding. When kept depressed, continuous forwarding results.

9-7-2. Playback with PLAY Head

Check

7. Now continue with the PG phase adjustment for the R/P head. Check that the "SET UP" display is flashing. Next press [IN (AUDIO)]. This operation causes the PLAY head to be selected. (When [IN (AUDIO)] is pressed again, the R/P head is selected.)
8. Check that the phase difference between VIDEO IN (CH-1) and DEMOD OUT (CH-2) signals is within $1 \pm 1\ \mu$sec. The DEMOD OUT signal should be delayed.
   If it is not within this value, conduct the following adjustment.
   If it is within the value, proceed to step 10.

Adjustment

9. Adjust the phase difference between VIDEO IN and DEMOD OUT signals to within $1 \pm 1\ \mu$sec as follows.
   a. When the DEMOD OUT signal is ahead, press [9] or blue [IN] while keeping blue [OUT] on the 21-key section depressed. [9] provides slow forwarding and [IN] fast forwarding. When kept depressed, continuous forwarding results.
   b. When the DEMOD OUT signal is delayed, press [7] or [8] while keeping blue colored [OUT] on the 21-key section depressed. [8] provides slow forwarding and [7] fast forwarding. When kept depressed, continuous forwarding results.
10. Set the VTR to the STANDBY OFF mode.
11. The results of the above adjustment (R/P PG and PLAY PG) are written into the non-volatile RAM and so proceed until step 13. Press the [C], [T] and [F] keys in sequence with blue colored [OUT] on the 21-key section depressed. Next, press [SET].
    This operation causes the following to appear on the control panel display :

>PG ADJ -	>NVW_
XXXX XXXX XXXX	>XXXX

12. Press [+] on the 21-key section and keep this depressed until the following appears on the control panel display :

>XXXX XX-XX	>XXXX XX-XX
XXXX XXXX XXXX	>PUSH NVWR SW_

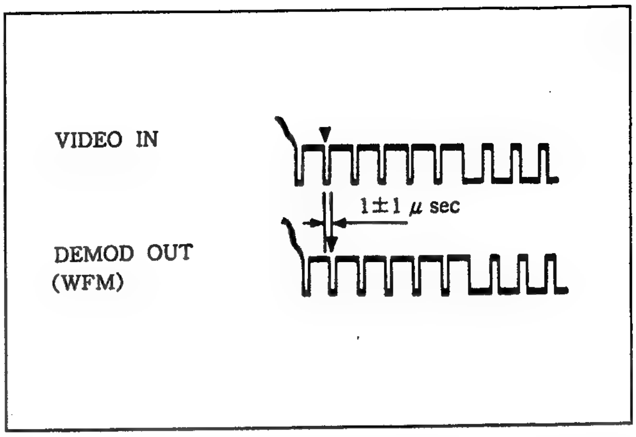


Fig.9-27. Phase Check During PLAY Head Playback

13. Press the NVWR switch on the SV-90 board. This operation causes the following to appear on the control panel display :

>PUSH NVWR SW_	>READY_
XXXX XXXX XXXX	>_

14. Press the [C], [0] and [SET] keys in sequence on the 21-key section.
    This operation causes the following to appear on the control panel display :

>CO_	>TEST MODE OFF_
	>_

15. Press [SET] while keeping blue colored [OUT] on the 21-key section depressed. This operation causes a return to the normal operating mode.

9. TAPE PATH SYSTEM ALIGNMENT

9-8. OVERLAP ADJUSTMENT

Preliminary Information

A. "Overlap" denotes the segment of the played back video RF waveform which is cut off by PB switching.

B. If overlaps B and C in the odd field are adjusted, it is not necessary to adjust dropout A and the overlap on the tape exit side in the even field. See Fig.9-29.

C. After the overlaps have been adjusted, turn off the VTR's power, rotate the drive motor of the moving guide using a flat-blade screwdriver so that the guide is closed, and then check the clearances below using a thickness gauge.
- Clearance between entrance guide bracket and upper drum : 0.09 to 0.12mm.
- Clearance between fence (entrance side) and upper drum : 0.15±0.05mm
- Clearance between exit slant guide and upper drum : 0.09±0.01mm

D. Adjustment points
- When adjusting overlap C on the tape entrance side, set so that the slant guide assembly can be rotated around mounting screw M, and adjust the clearance between the guide bracket and the upper drum.
- The clearance between the guide bracket and the upper drum can be adjusted using the setscrew which is screwed into the boss.
- When adjusting overlap B on the tape exit side, set so that the exit slant guide assembly can be rotated around mounting screw M, and adjust the clearance between the exit slant guide and the upper drum.
- The clearance between the exit slant guide and the upper drum can be adjusted using the setscrew which is screwed into the boss.

E. The following thickness gauge should be provided for these adjustments :
Sony Part No. J-6041-670-A

F. When the overlaps have been adjusted, check again and then complete the operation.

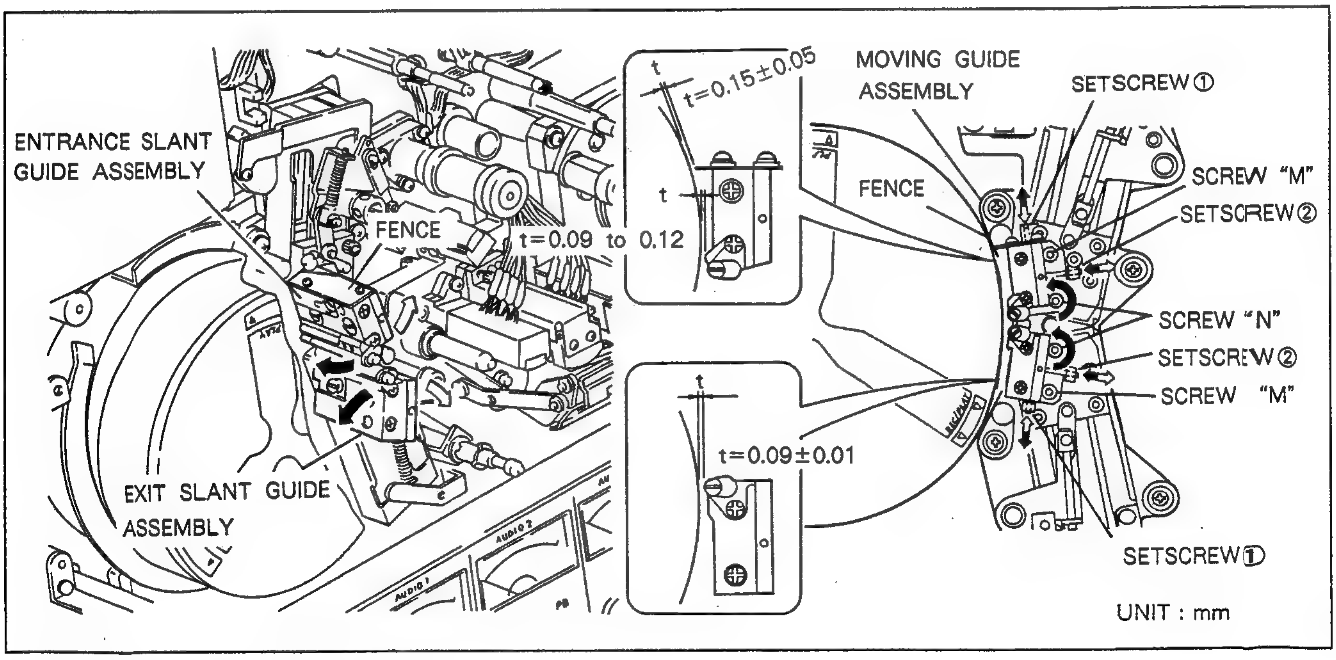


Fig.9-28. Overlap Adjustment Method

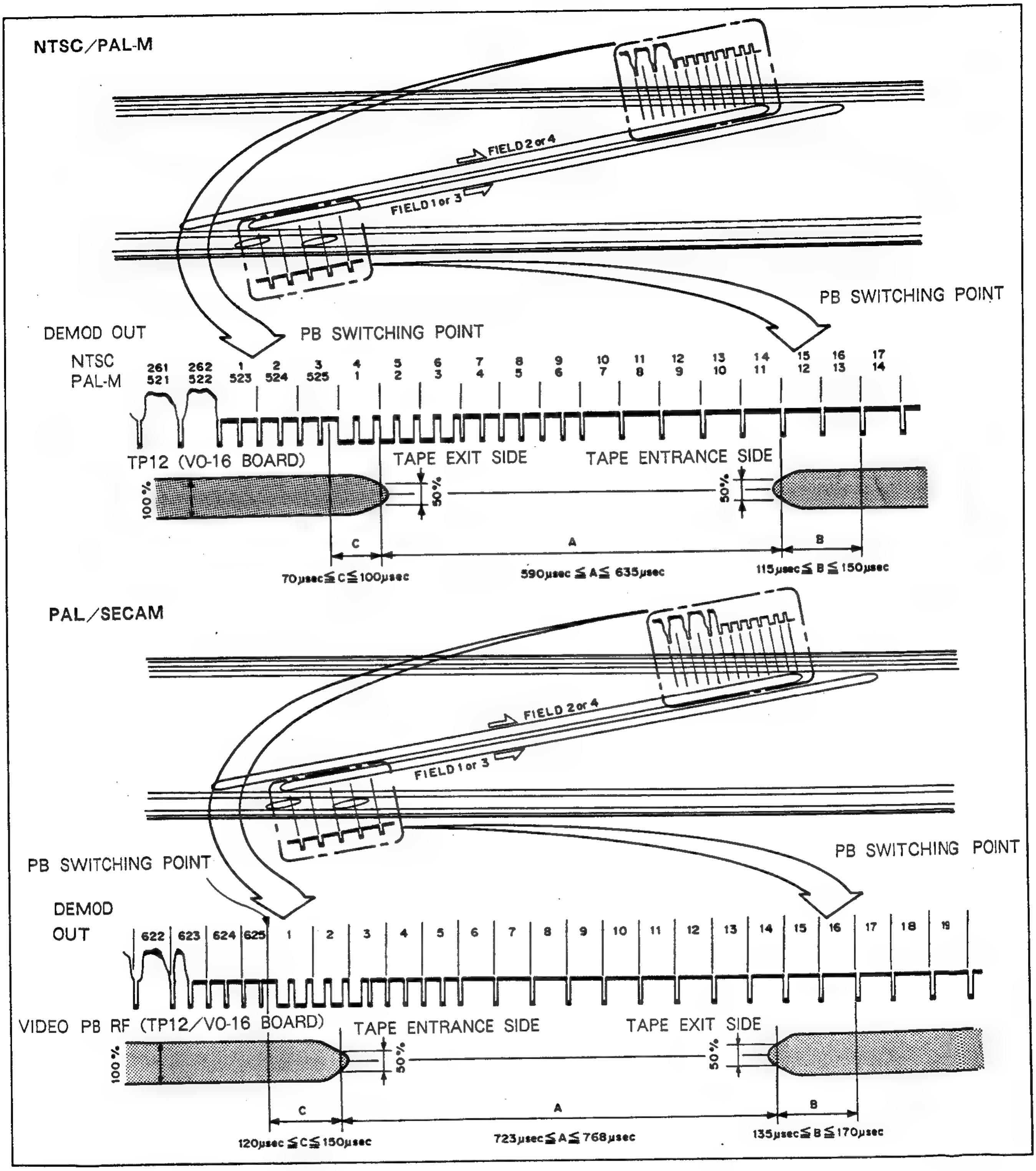


Fig.9-29. Overlap Adjustment

9-8-1. Overlap Check

1. Connect CH-1 of the oscilloscope to TP12 on the VO-16 board and connect CH-2 to the WFM MONITOR OUT connector on the connector panel.
2. Thread a general-purpose tape.
3. Press [0] on the 21-key section while keeping switch S2 on the SY-103 board depressed. (Alternatively, select "TTP ADJ" of the test menu T17. Reference should be made to Section 3-2.) This operation causes the following to appear on the control panel display :

	>_

4. Press [C], [8], [2] and [SET] in sequence on the 21-key section. This operation causes the following to appear on the control panel display :

>C82_	>OVERLAP CHECK _
XXXX XXXX XXXX	>_

The R/P head is now selected and the DEMOD OUT signal is output from the WFM MONITOR OUT connector.

5. Record a video signal.
6. Play back the recorded section and check that overlaps B and C satisfy the value given in Fig. 9-29.
7. Press the [C], [0] and [SET] keys in sequence on the 21-key section.
This operation causes the following to appear on the control panel display :

>CO_	>TEST MODE OFF_
	>_

8. Press [SET] while keeping blue colored [OUT] on the 21-key section depressed. This operation causes a return to the normal operating mode.

9-8-2. Overlap Adjustment

Preliminary Information

A. When the position of the entrance slant guide assembly has been adjusted, check the clearance between the top of the guide bracket and upper drum. See Fig.9-30.
B. When the position of the exit slant guide assembly has been adjusted, check the clearance between the guide post and upper drum.

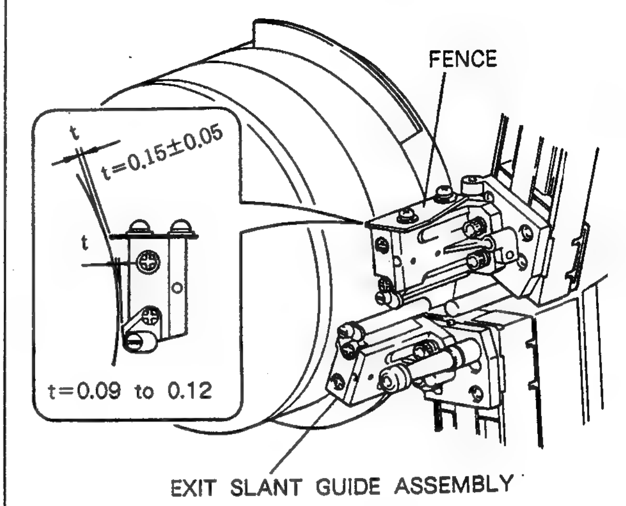


Fig.9-30. Checking Clearance Near Slant Guide Assembly

I. When overlap C does not conform to the specified value

1. Press [0] on the 21-key section while keeping switch S2 on the SY-103 board depressed. (Alternatively, select "TTP ADJ" of the test menu T17. Reference should be made to Section 3-2.) This operation causes the following to appear on the control panel display :

	>_

2. Press [C], [8], [2] and [SET] in sequence on the 21-key section. This operation causes the following to appear on the control panel display :

>C82_	>OVERLAP CHECK _
XXXX XXXX XXXX	>_

The R/P head is now selected and the DEMOD OUT signal is output from the WFM MONITOR OUT connector.

3. Loosen screw N, which mounts the entrance slant guide assembly shown in Fig.9-31, by one-half to one full turn.
   Note : Screw M must not be loosened.
4. Depending on the symptom, adjust setscrews ① and ② which are screwed into the boss.
   a. If overlap C is less than the specified value, reduce clearance S by rotating setscrew ① counterclockwise and setscrew ② clockwise. Position the thickness gauge and adjust by rotating setscrew ①.
   b. If overlap C is more than the specified value, increase clearance S by retracting the fence in direction A, rotating setscrew ② counterclockwise and then by rotating setscrew ① clockwise.
5. Tighten up screws N and M.
6. Rotate the upper drum by hand so that the head is distanced from the entrance slant guide assembly.
7. Use the thickness gauge to check that the clearance between the guide bracket and upper drum is within the specified value.
8. Check overlap C again following check sequence steps 5 and 6 in Section 9-8-1. Repeat the checks and adjustments until overlap C conforms to the specified value.
9. When the fence has been retracted in step 4-b, adjust it to the clearance shown in Fig. 9-30.
10. Press the [C], [0] and [SET] keys in sequence on the 21-key section.
    This operation causes the following to appear on the control panel display :

>CO_	>TEST MODE OFF_
	>_

11. Press [SET] while keeping bule colored [OUT] on the 21-key section depressed. This operation causes a return to the normal operating mode.

II. When overlap B does not conform to the specified value

Adjust the exit slant guide assembly following the same check and adjustment procedure as in I. See Fig.9-32.

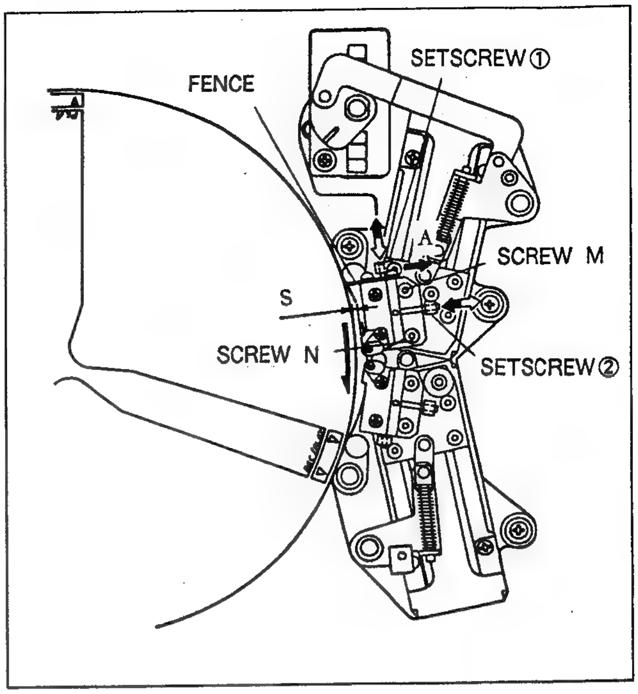


Fig.9-31. Overlap C Adjustment

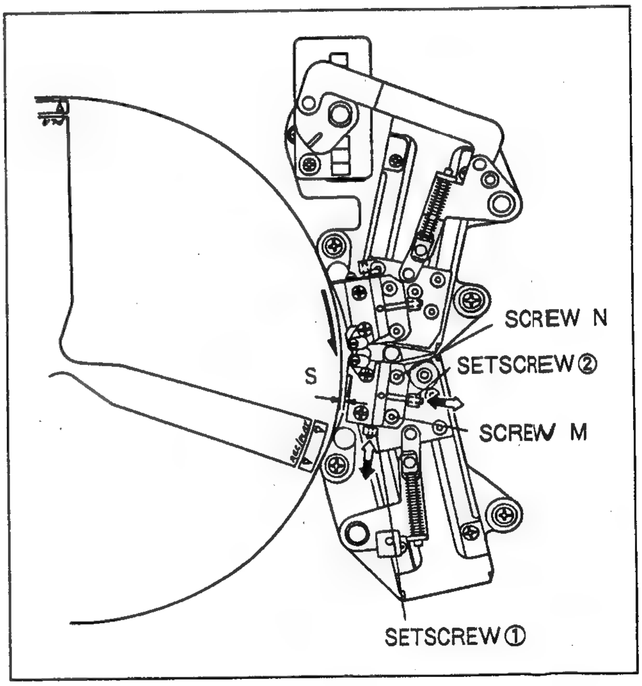
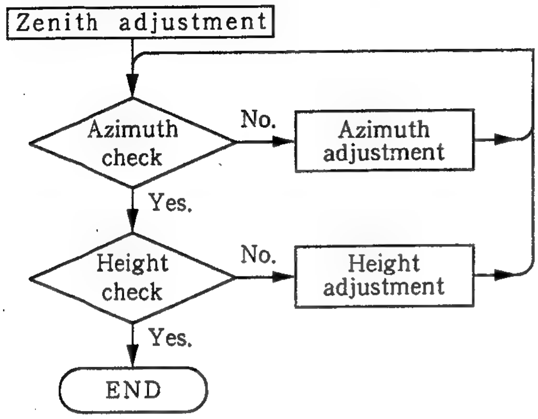


Fig.9-32. Overlap B Adjustment

9-9. AUDIO/CTL R/P HEAD ADJUSTMENT

Preliminary Information

A. A flowchart for the checks and adjustments is provided below.



B. When the guides on the tape path have been adjusted, be sure to check the audio/CTL R/P head (hereafter known as the R/P head; same applies to the other heads), following the above flowchart.

C. Prepare the following flat plate for the zenith adjustment:
Sony Part No. J-6040-160-A

D. The zenith adjustment need not be performed except when the zenith adjustment screw has been moved or when the azimuth screw has been forcibly tightened up.

9-9-1. Zenith Adjustment

1. Place the flat plate which has been provided as shown in Fig.9-34. When the plate has been placed on the erase head without any space left, check that there is no clearance between the R/P head and flat plate.
   Check the clearance in the same way between the R/P head and monitor head and between the monitor head and guide post 2.
2. If some space is left, rotate the zenith adjustment screw of the R/P head and monitor head so that the respective clearances are made the same and minimized.

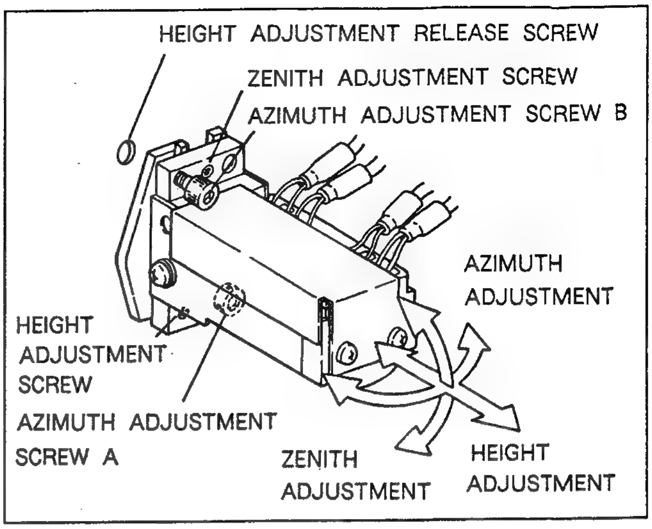


Fig.9-33. Audio/CTL R/P Head Adjustment Screws

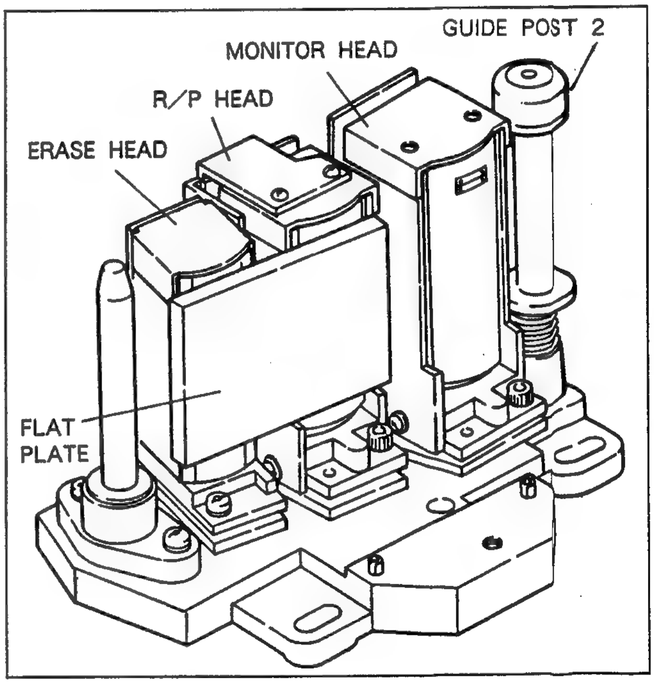


Fig.9-34. Zenith Adjustment

9-9-2. Azimuth Adjustment

Preliminary Information

A. Adjustment is conducted with a frequency of 3kHz serving as the reference. Since this 3kHz reference is used, the 15kHz frequency is used for checking purposes only.

Check and Adjustment

1. Connect the oscilloscope to the AUDIO-1 OUT and AUDIO-2 OUT connectors and set it to the EXT. HORIZONTAL mode.
2. Play back the audio 3kHz segment of the alignment tape and adjust the PB LEVEL control so that 0VU is indicated on both the AUDIO-1 and AUDIO-2 meters on the level control panel. Next, adjust the oscilloscope and set the amplitude of both channels to 6cm.
3. Check that the phase difference between the AUDIO-1 and AUDIO-2 signals is within the specifications in Fig.9-35 when the audio 3kHz segment is played back. The specified phase difference is not more than 5° but adjustment is recommended to 0°.
4. Loosen azimuth adjustment screw B. Now adjust the phase difference to 0° using screw A. Turn screw B slightly in the tightening (clockwise) direction and adjust screw A again so that the phase difference is made 0°. Repeat the same procedure until screws A and B reach the prescribed tightening torque. Check that the phase difference is now zero with the screws completely tightened up.

   Note: Finally, tighten up the two screws with a torque of 6 to 8kg • cm.
5. Play back the audio 15kHz segment of the alignment tape and adjust the oscilloscope so that the AUDIO-1 and AUDIO-2 signal amplitudes are respectively made 6cm.
6. Check that the phase difference applying when the audio 15kHz segment is played back conforms to the specifications in Fig.9-36.

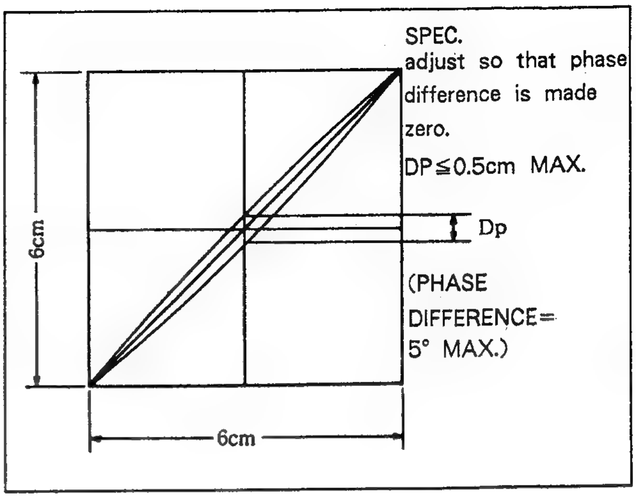


Fig.9-35. Azimuth Adjustment with Audio 3kHz Playback

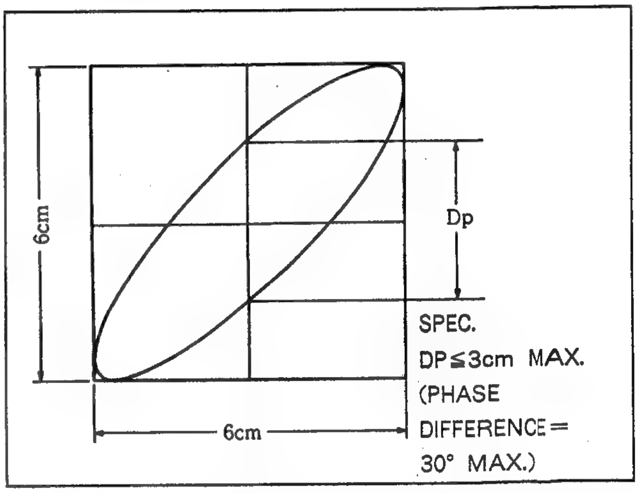


Fig.9-36. Azimuth Check with Audio 15kHz Playback

9-9-3. Height Adjustment

Check

1. Connect the oscilloscope to the AUDIO-1 OUT and AUDIO-2 OUT connectors.
2. Play back the audio 3kHz segment of the alignment tape. Adjust the oscilloscope so that the signal amplitude of both channels is increased and made equal, as shown in Fig.9-37. Observe clearance G.
3. Check that clearance G increases when the tape edge near the audio/CTL R/P head is pushed up or down during playback. If G is reduced, the following adjustment is required.

Adjustment

4. Loosen the height adjustment release screw by one-half to one full turn.
5. Depending on the symptom, rotate the height adjustment screw as follows :
   a. If G is reduced when the tape is pushed down, turn the height adjustment screw clockwise.
   b. If G is reduced when the tape is pushed up, turn the height adjustment screw counterclockwise.
6. Tighten up the height adjustment screw and check the height again by performing step 3 again.

   Note : The height adjustment release screw should be tightened up with a torque or 14 to 16kg • cm.

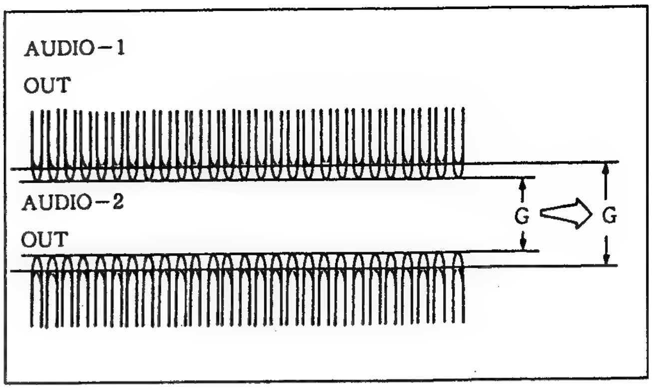


Fig.9-37. Audio Head Height Check

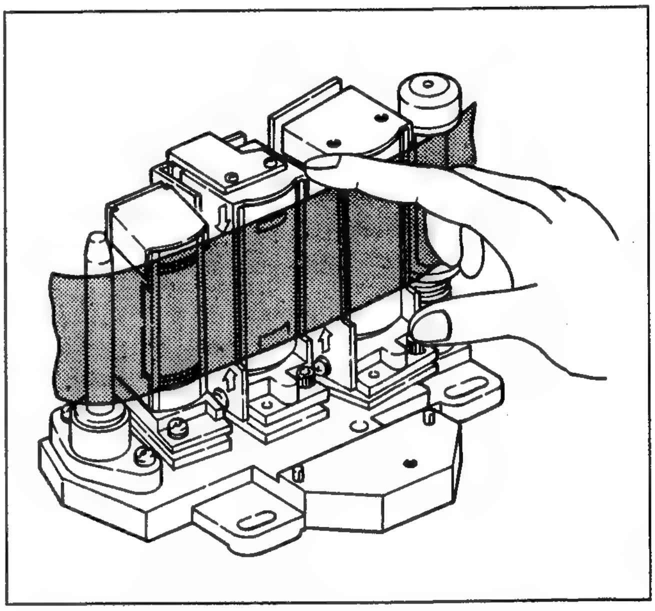
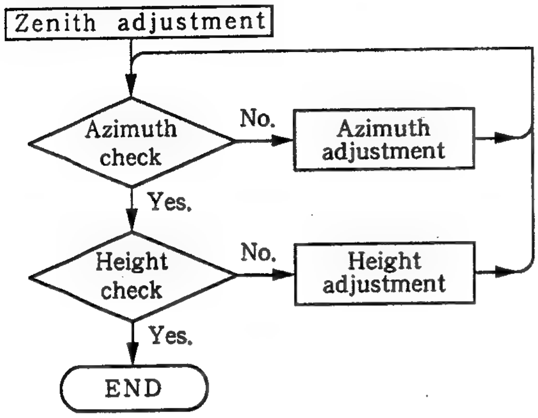


Fig.9-38. Audio/CTL R/P Head Height Check

9-10. AUDIO MONITOR HEAD ADJUSTMENT

Preliminary Information

A. A flowchart for the checks and adjustments is provided below.



B. When the guides on the tape path have been adjusted, be sure to check the audio monitor head (hereafter known as the monitor head), following the above flowchart.

C. Prepare the following flat plate for the zenith adjustment :
Sony Part No. J-6040-160-A

D. The zenith adjustment need not be performed except when the zenith adjustment screw has been moved or when the azimuth screw has been forcibly tightened up.

9-10-1. Zenith Adjustment

1. Place the flat plate which has been provided as shown in Fig.9-40. When the plate has been placed on the audio R/P head without any space left, check that there is no clearance between the monitor head and flat plate.
   Next, check the clearance in the same way between the monitor head and guide post 2.
2. If some space is left, rotate the zenith adjustment screw of the monitor head so that the respective clearances are made the same and minimized.

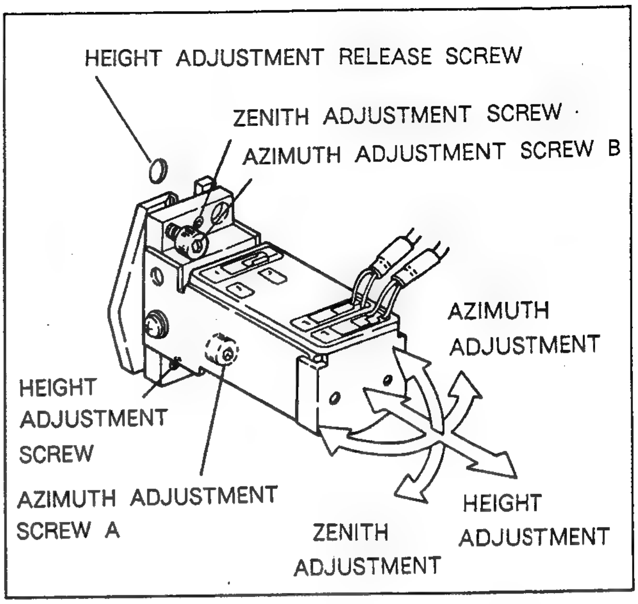


Fig.9-39. Audio Monitor Head Adjustment Screws

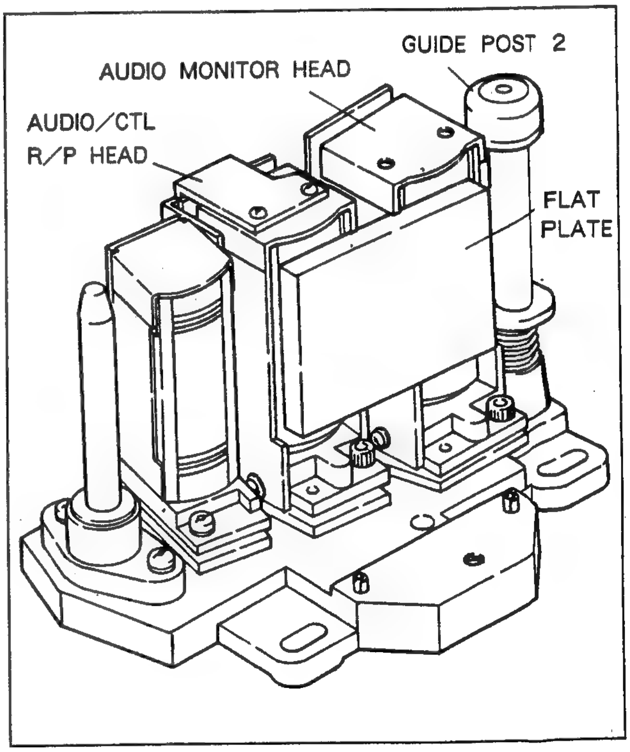


Fig.9-40. Zenith Adjustment

9-10-2. Azimuth Adjustment

Preliminary Information

A. Adjustment is conducted with a frequency of 3kHz serving as the reference. Since a 3kHz reference is used, the 15kHz frequency is used for checking purposes only.

Check and Adjustment

1. Check that the AUDIO MONITOR selector button has been set to AUDIO 1/AUDIO 2. Select the T15 CONFI TEST by means of the test menu and set it ON.(Refer to Section 3-2.) Set it OFF at height adjustment step 7. in Section 9-10-3.
2. Connect the oscilloscope to the MONITOR OUTPUT L and R connectors on the connector panel and set the oscilloscope to the EXT. HORIZONTAL mode.
3. Play back the audio 3kHz segment of the alignment tape, rotate the headphone volume control and adjust the output to 4Vp-p. Now adjust the oscilloscope and set the amplitude of both channels to 6cm.
4. Check that the phase difference between the two channels is within the specifications in Fig.9-41 when the audio 3kHz segment is played back. The specified phase difference is below 5° but adjustment is recommended to 0° .
5. Loosen azimuth adjustment screw B. Now adjust the phase difference to 0° using screw A. Turn screw B slightly in the tightening (clockwise) direction and adjust screw A again so that the phase difference is made 0° . Repeat the same procedure until screws A and B reach the prescribed tightening torque. Check that the phase difference is now zero with the screws completely tightened up.
   Note : Finally, tighten up the two screws with a torque of 6 to 8 kg • cm.
6. Play back the audio 15kHz segment of the alignment tape and adjust the oscilloscope so that the signal amplitudes of both channels are respectively made 6cm.
7. Check that the phase difference applying when the audio 15kHz segment is played back conforms to the specifications in Fig.9-42.

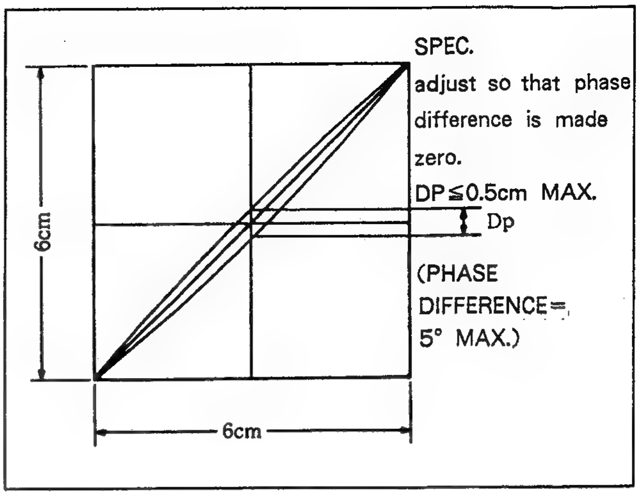


Fig.9-41. Azimuth Adjustment with Audio 3kHz Playback

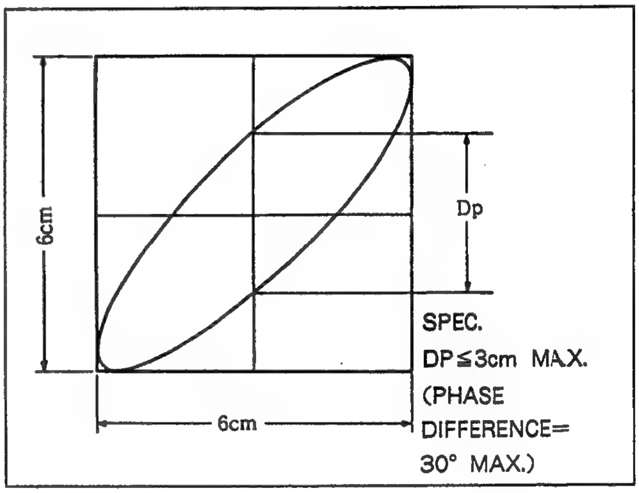


Fig.9-42. Azimuth Check with Audio 15kHz Playback

9-10-3. Height Adjustment

Check

1. With the same set-up as that under step 1 of the azimuth adjustment, connect the oscilloscope to the MONITOR OUTPUT L and R connectors.
2. Play back the audio 3kHz segment of the alignment tape. Adjust the oscilloscope so that the signal amplitude of both channels is increased and made equal, as shown in Fig.9-43. Observe clearance G.
3. Check that clearance G increases when the tape edge near the monitor head is pushed up or down during playback. If G is reduced, the following adjustment is required.

Adjustment

4. Loosen the height adjustment release screw by one-half to one full turn.
5. Depending on the symptom, rotate the height adjustment screw as follows :
   a. If G is reduced when the tape is pushed down, turn the height adjustment screw clockwise.
   b. If G is reduced when the tape is pushed up, turn the height adjustment screw counterclockwise.
6. Tighten up the height adjustment screw and check the height again by performing step 3 again.
   Note : The height adjustment release screw should be tightened up with a torque of 14 to 16kg • cm.
7. Set the test menu T15 CONFI TEST to OFF. (Refer to Section 3-2.)

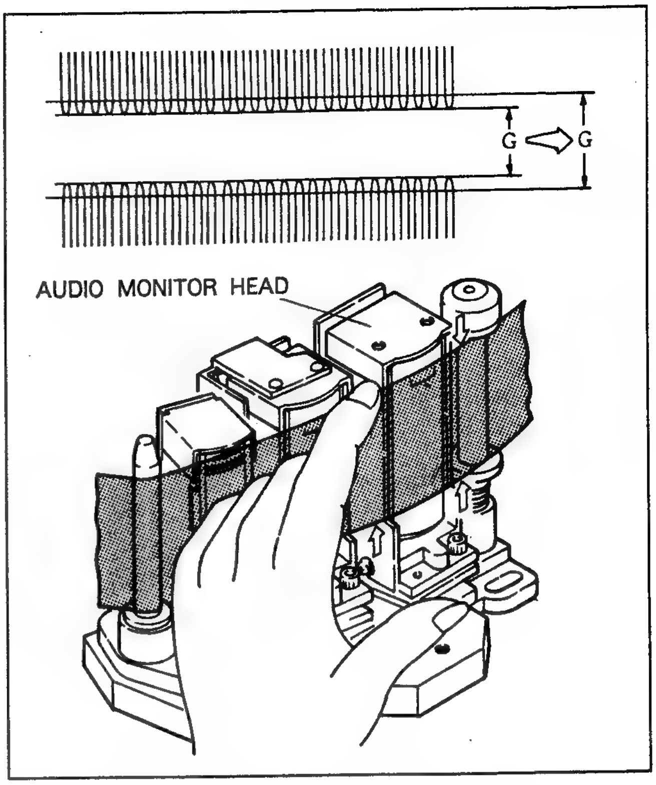


Fig.9-43. Audio Monitor Head Height Check

9-11. AUDIO/CTL ERASE HEAD HEIGHT ADJUSTMENT

Preliminary Information

The audio/CTL erase head height must be checked when this head has been replaced and also when the head drum assembly has been replaced and the height of the guides has been adjusted.

Check

1. Record a 1kHz signal onto the AUDIO-1 and AUDIO-2 channels.
2. Rewind the segment which was recorded in step 1 and record no signals for both channels.
3. Connect the headphones and play back the segment which was recorded without signals in step 2. Check that the 1kHz signal cannot be heard even with the monitor/headphone volume level control at its maximum position. If it can be heard, the following adjustment must be performed.

Adjustment

4. Loosen the adjustment release screw by one-half to one full turn.
5. Referring to Fig.9-44, adjust the head height. The height of the head changes when the height adjustment screw is rotated. After the adjustment release screw has been tightened, repeat steps 1 through 3 and check the head height.

   Note : The adjustment release screw should be tightened up with a torque of 14 to 16kg • cm.

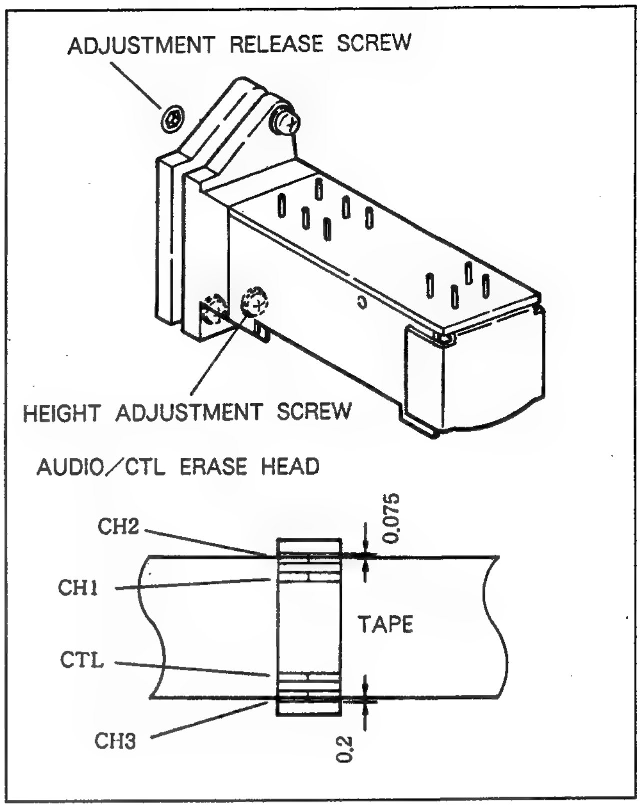
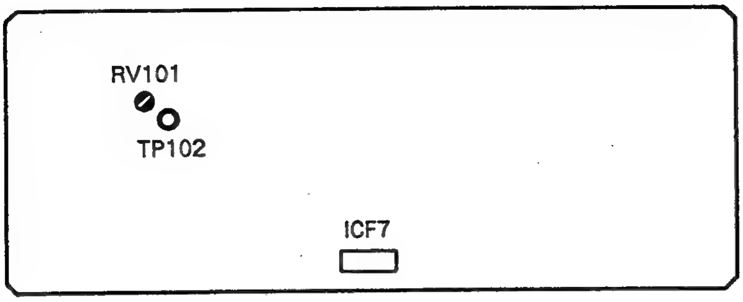


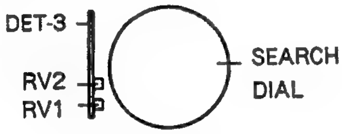
Fig.9-44. Audio/CTL Erase Head Height Adjustment

SECTION 10
SYSTEM CONTROL／SERVO ALIGNMENT

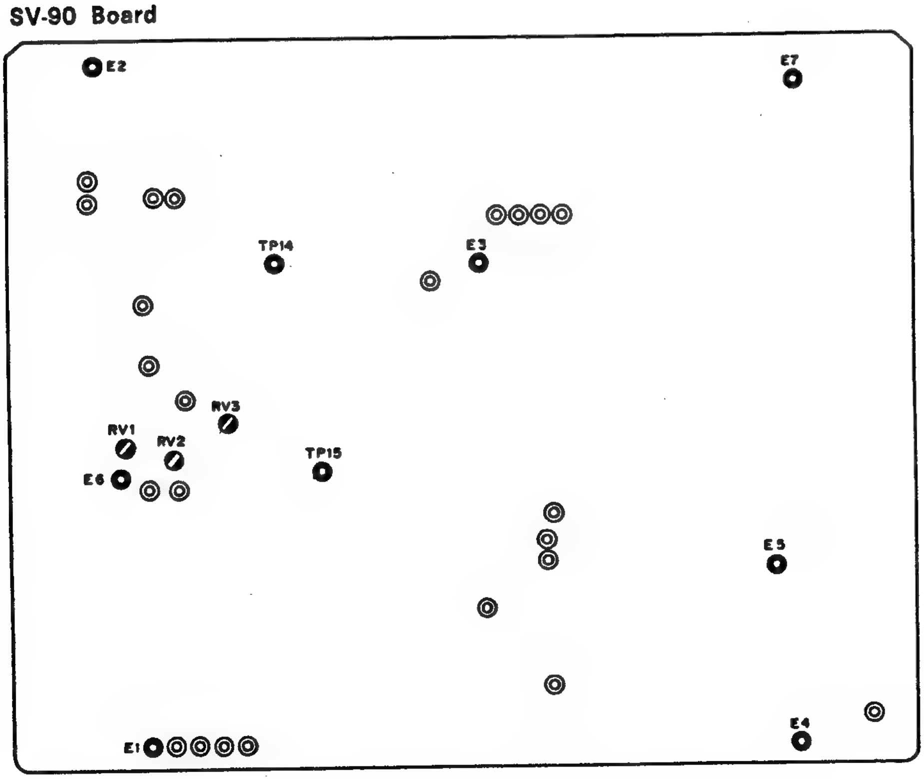
KC-14 Board



DET-3 Board



SV-90 Board

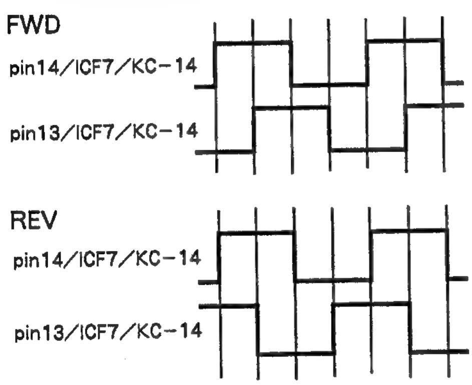


10-1. +5V ADJUSTMENT (CONTROL PANEL)

(1) Take out the KC-14 board from the control panel.
(2) Connect the 8-pin multicable from Mother board to the connector CN701/KC-14 board.
(3) Turn the power on, and adjust as follows.
TP102/KC-14 = +5.0 ± 0.01Vdc
⊘RV101/KC-14 board
(4) Turn the power off, and return the KC-14 board to the control panel.

10-2. DIAL PULSE AMPLIFIER ADJUSTMENT

(1) Set a dual trace oscilloscope to CHOP, DC, 2V/DIV and 2mSEC/DIV. Connect it to pin14 of ICF7 and pin13 of ICF7 on KC-14 board.
(2) Set the VTR to JOG mode and turn ⊘RV1 on DET-3 board CW (clockwise) /CCW (counter-clockwise) while turning the search dial.
Set ⊘RV1 in the middle of the points where the pulse appears at pin14 of ICF7 by turning ⊘RV1 CW/CCW.
(3) Adjust ⊘RV2 on DET-3 borad for pin13 of ICF7 similarly as Step 2.
(4) Make sure that the timing of the pulse is shown below by turning the search dial in the direction of FWD/REV.



10-3. SERVO A/D AND D/A CONVERTER ADJUSTMENT

[Caution]
Do not perform adjustment if the software in the SV, SY, and RD boards is version 1. Before performing adjustment, confirm that the software is version 2 or higher. The version No. is indicated on the label of the IC as shown below.

Board	Ref. No.	Version 1	Version 2
SV-90	ICN5	V0U1-*-*	V0U2-*-*
	ICN3	V1U1-*-*	V1U2-*-*
	ICE15	V2U1-*-*	V2U2-*-*
SY-103	ICH12 (NTSC)	Y0U1-*-*	Y0U2-*-*
	(PS)	Y0A1-*-*	Y0A2-*-*
	ICH11 (NTSC)	Y1U1-*-*	Y1U2-*-*
	(PS)	Y1A1-*-*	Y1A2-*-*
RD-6	ICL15 (NTSC)	RDU1-*-*	RDU2-*-*
RD-7	ICM14 (PS)	RDP1-*-*	RDU2-*-*

(1) Put the VTR in the STOP (STANDBY OFF) mode.
(2) A/D converter reference voltage adjustment
TP15/SV-90 : +3.000±0.002Vdc
using digital voltmeter
⊘RV1/SV-90

(3) D/A converter adjustment
Select [TTP ADJ] of the test menu [T17. MAINTENANCE]. See section 3-3.
Key in $\boxed{C}$, $\boxed{5}$, then press the $\boxed{SET}$ key. [C5. DAC ADJUST] will be selected, and the following will be displayed on the control panel.

>C5	> DAC ADJUST
XXXX	>_

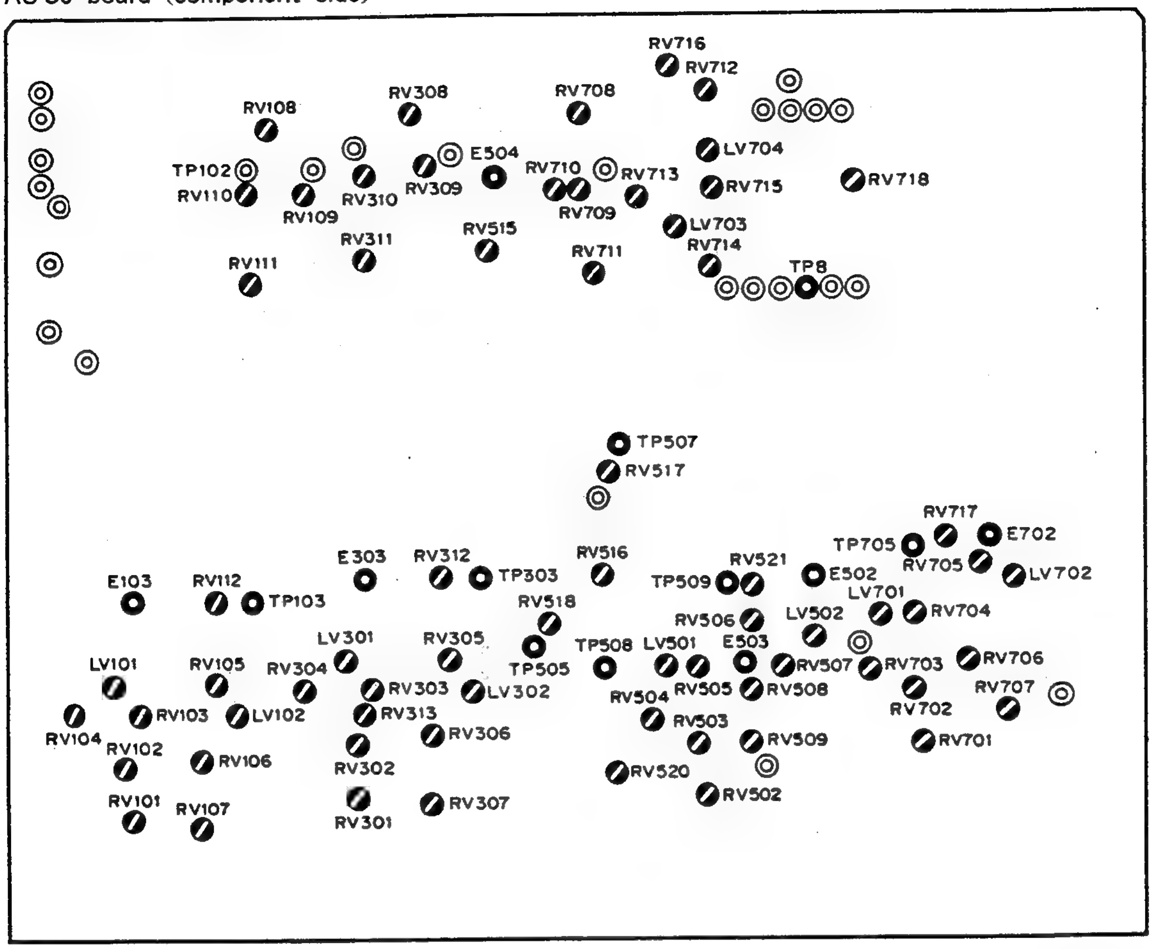
Perform adjustment as follows.
TP14/SV-90 : 0.000±0.001Vdc
using digital voltmeter
⊘RV2/SV-90

Next, press the $\boxed{7}$ key while pressing the blue $\boxed{OUT}$ key, then perform the following adjustment while keeping these keys pressed.
TP14/SV-90 : +2.000±0.002Vdc
using digital voltmeter
⊘RV3/SV90

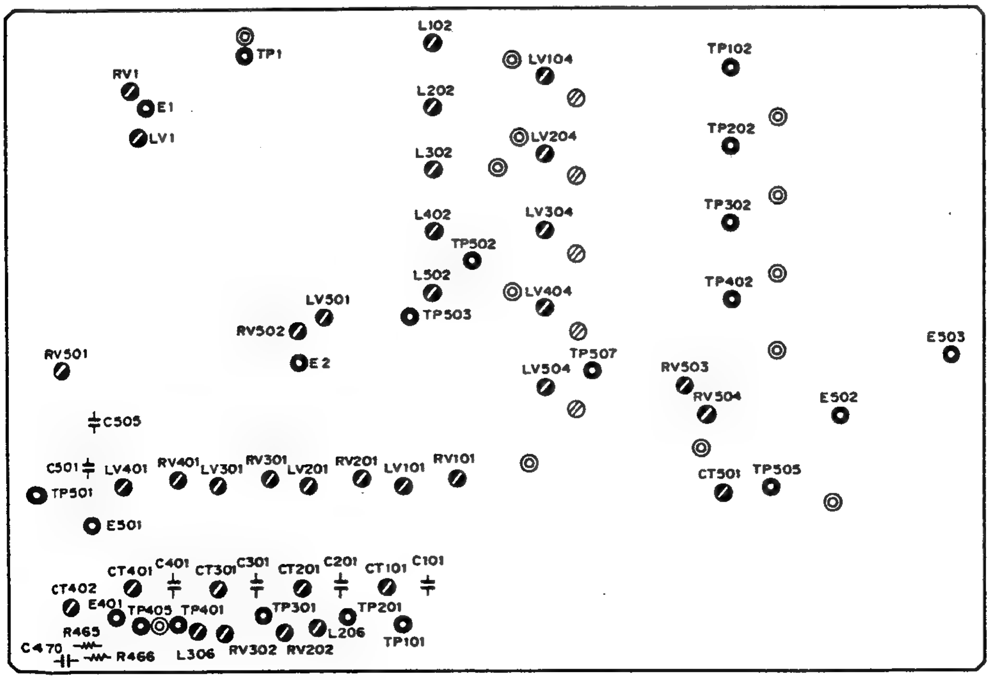
After adjustment, press the $\boxed{C}$, $\boxed{0}$ and $\boxed{SET}$ keys in that sequence, then press the $\boxed{SET}$ key while pressing the blue $\boxed{OUT}$ key.

SECTION 11
AUDIO SIGNAL SYSTEM ALIGNMENT

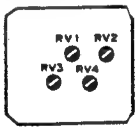
AU-88 board (component side)



AP-15 board (component side)



BC-12 board (component side)



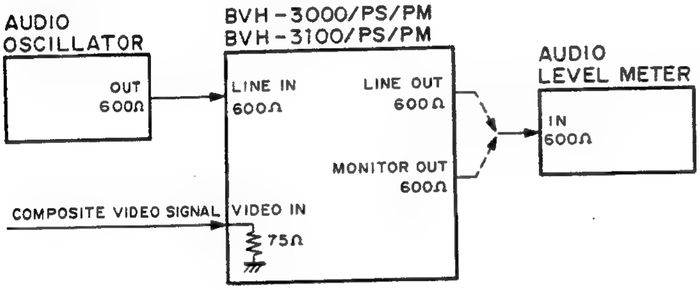
11-1. ADJUSTMENT PREPARATIONS

Note :
The details and descriptions in Section 11 apply to the following models :

BVH-3000/3100 (UC) : NTSC
BVH-3000PS/3100PS : PAL/SECAM-A3
BVH-3000PS-A4/3100PS-A4 : PAL/SECAM-A4
BVH-3000PM/3100PM : PAL-M

Four audio channels are featured only on the BVH-3000PS-A4/3100PS-A4 models. Those details in Section 11 relating to AUDIO CH-4 (A4) apply only to the BVH-3000PS-A4/3100PS-A4 models.

(1) Equipment connections



(2) Menu/switch settings

NR-26 board (option BKH-3080)
NORM/SETUP switch : NORM
CH 1 PB CAL/UNCAL switch : CAL
CH 2 PB CAL/UNCAL switch : CAL
A/OFF/SR switch : OFF

Level control panel
AUDIO LINE OUT level control : Preset
AUDIO 1, 2, 3/4 REC level controls : Preset
AUDIO 1, 2, 3/4 PB level controls : Preset
REC INHIBIT switches : OFF
REMOTE/LOCAL switch : LOCAL

Function control panel
TAPE/IN key : TAPE/EE

Menu
Using the following key operations, load the default menu selection data on the PROM (data supplied with unit at time of shipment) into the RAM.
[SET UP] → [T] → [0] → [SET]

Perform the following setting :
S50. A3 INPUT SELECT : LINE

Also perform the following settings for the PS-A4 model :
S10. SYNC/A4 SELECT : A4
S70. AUDIO METER SELECT :
Set to A3 or A4 as required. This setting enables either the AUDIO 3 or AUDIO 4 signal to be output to the A3/4 meter and AUDIO MONITOR OUTPUT connector.

(3) Reference level of audio input/output

The audio line input/output level of BVH-3000/3100 is set to +8dBm when shipped. However, it is possible to change the line input/output reference level from +8dBm to your studio level. See section 1-7-3 Altering the reference level of audio input/output.

11-2. ADJUSTMENT SEQUENCE

Overall audio system adjustment

- 11-1. Adj. Preparations
- 11-3. REC Level Preset, Line Output Level and Meter Adj.
- 11-4. PB Freq. Response and PB Level Presetting Adj.
- 11-5. CTL PB Level Adj.
- 11-6. Bias Amp. Adj.
- 11-7. Erase Current Adj.
- 11-8. CTL Bias Current Adj.
- 11-9. Audio Bias Adj.
- 11-10. Rec. Level Adj.
- 11-11. Confi. Level Adj.
- 11-12. Rec. Amp. Freq. Response Adj.
- 11-13. A1/A2 Phase Difference Adj.
- 11-14. REC-PB A1/A2, A3/A4 Crosstalk Adj.
- 11-15. CTL Rec. Level Adj.
- 11-16. Audio-CTL Crosstalk Adj.
- 11-17. PB A1-A2, A3-A4 Crosstalk Adj.
- 11-18. Monitor Amp. Freq. Response Adj.
- 11-19. Time Code Duty Adj.
- 11-20. Time Code Level Adj.
- 11-21. Rec. Bias Leak Adj.

Audio R/P head replacement

- 11-1. Adj. Preparations
- 11-4. PB Freq. Response and PB Level Presetting Adj.
- 11-5. CTL PB Level Adj.
- 11-8. CTL Bias Current Adj.
- 11-9. Audio Bias Adj.
- 11-10. Rec. Level Adj.
- 11-11. Confi. Level Adj.
- 11-12. Rec. Amp. Freq. Response Adj.
- 11-13. A1/A2 Phase Difference Adj.
- 11-14. REC-PB A1/A2, A3/A4 Crosstalk Adj.
- 11-15. CTL Rec. Level Adj.
- 11-16. Audio-CTL Crosstalk Adj.
- 11-17. PB A1-A2, A3-A4 Crosstalk Adj.
- 11-18. Monitor Amp. Freq. Response Adj.
- 11-21. Rec. Bias Leak Adj.

Monitor head replacement

- 11-1. Adj. Preparations
- 11-11. Confi. Level Adj.
- 11-18. Monitor Amp. Freq. Response Adj.

Erase head replacement

(AUDIO/FULL/VS)

- 11-1. Adj. Preparations
- 11-7. Erase Current Adj.

AU−88 board replacement

- 11-1. Adj. Preparations
- 11-3. REC Level Preset, Line Output Level and Meter Adj.
- 11-4. PB Freq. Response and PB Level Presetting Adj.
- 11-10. Rec. Level Adj.
- 11-11. Confi. Level Adj.
- 11-12. Rec. Amp. Freq. Response Adj.
- 11-13. A1/A2 Phase Difference Adj.
- 11-14. REC-PB A1/A2, A3/A4 Crosstalk Adj.
- 11-16. Audio-CTL Crosstalk Adj.
- 11-17. PB A1-A2, A3-A4 Crosstalk Adj.
- 11-18. Monitor Amp. Freq. Response Adj.
- 11-19. Time Code Duty Adj.
- 11-20. Time Code Level Adj.
- 11-21. Rec. Bias Leak Adj.

AP−15 board replacement

- 11-1. Adj. Preparations
- 11-5. CTL PB Level Adj.
- 11-6. Bias Amp. Adj.
- 11-7. Erase Current Adj.
- 11-8. CTL Bias Current Adj.
- 11-9. Audio Bias Adj.
- 11-10. Rec. Level Adj.
- 11-11. Confi. Level Adj.
- 11-12. Rec. Amp. Freq. Response Adj.
- 11-13. A1/A2 Phase Difference Adj.
- 11-14. REC-PB A1/A2, A3/A4 Crosstalk Adj.
- 11-15. CTL Rec. Level Adj.
- 11-16. Audio-CTL Crosstalk Adj.
- 11-17. PB A1-A2, A3-A4 Crosstalk Adj.
- 11-18. Monitor Amp. Freq. Response Adj.
- 11-20. Time Code Level Adj.
- 11-21. Rec. Bias Leak Adj.

BC−12 board replacement

- 11-1. Adj. Preparations
- 11-9. Audio Bias Adj.
- 11-10. Rec. Level Adj.
- 11-11. Confi. Level Adj.
- 11-12. Rec. Amp. Freq. Response Adj.
- 11-13. A1/A2 Phase Difference Adj.
- 11-21. Rec. Bias Leak Adj.

VR−51 board replacement

- 11-1. Adj. Preparations
- 11-3. REC Level Preset, Line Output Level and Meter Adj.
- 11-4. PB Freq. Response and PB Level Presetting Adj.

11-3. REC LEVEL PRESET, LINE OUTPUT LEVEL AND METER ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1.
Mode of VTR :	STOP (EE)
Instruments :	Digital voltmeter Audio level meter
AUDIO LINE IN signal :	1kHz/reference level (reference level : See sec. 11-1.)

(1) REC level presetting adjustment
A1 : TP103-E103/AU-88
A2 : TP303-E303/AU-88
A3 : TP509-E502/AU-88
A4 : TP705-E702/AU-88
77.46±1 mVrms on digital voltmeter
⊘REC level preset controls (for each channel)
Note : The REC level preset controls are located on the bottom of the level control panel. Refer to section 2-4-2 in the operation manual.

(2) Line output level adjustment
LINE OUTPUT=reference level
A1 : ⊘RV112/AU-88
A2 : ⊘RV312/AU-88
A3 : ⊘RV521/AU-88
A4 : ⊘RV717/AU-88

(3) Level meter adjustment
Level meter indication=0VU±0.2dB
A1 : ⊘RV111/AU-88
A2 : ⊘RV311/AU-88
A3* : ⊘RV515/AU-88
A4* : ⊘RV711/AU-88

(*) The AUDIO 3/4 meter is set to A3 or A4 using menu [S70. AUDIO METER SELECT] for the adjustment of the PS-A4 model's level meter.

11-4. PB FREQUENCY RESPONSE AND PB LEVEL PRESETTING ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1 and text.
Mode of VTR :	PLAY
Instruments :	Audio level meter
AUDIO LINE IN signal :	Don't care.

(1) Set the REC INHIBIT switches to ON.

(2) Set the AUDIO PB level control to manual.
Perform the following adjustments while playing back the −10VU (or −2dBm) portion of the alignment tape.

1kHz : LINE OUT=Ref. level−10dB
⊘AUDIO PB level controls
(The PB level preset control is used to adjust A3 for the PS-A4 model.)

50Hz : LINE OUT=Ref. level$-10 {}^{+1.5}_{-3.0}$dB
⊘RV107 ⊘RV307 ⊘RV509 ⊘RV707/AU-88
100Hz : LINE OUT=Ref. level$-10 {}^{+1.5}_{-3.0}$dB
If the specifications are not satisfied, re-adjust 50Hz so that both the 50Hz and 100Hz frequencies satisfy the specifications.

10kHz : LINE OUT=Ref. level$-10 {}^{+1.5}_{-3.0}$dB
⊘RV106 ⊘RV306 ⊘RV508 ⊘RV706/AU-88
15kHz : LINE OUT=Ref. level$-10 {}^{+1.5}_{-3.0}$dB
If the specifications are not satisfied, re-adjust 10kHz so that both the 10kHz and 15kHz frequencies satisfy the specifications.

(3) Set the AUDIO PB level control to preset.
Adjust the PB level preset controls for each channel while playing back the 1kHz/0VU (or +8dBm) signal portion on the alignment tape. These controls are located on the bottom of the level control panel. Refer to section 2-4-2 in the operation manual.
LINE OUTPUT=Ref. level±0.1dB
⊘AUDIO PB level preset controls

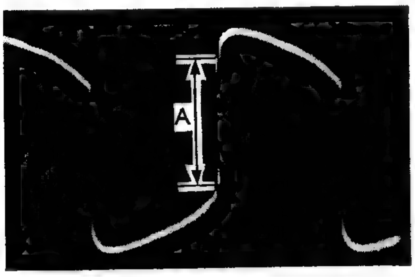
(4) After the adjustments, set the REC INHIBIT switches to OFF.

11-5. CTL PLAYBACK LEVEL ADJUSTMENT

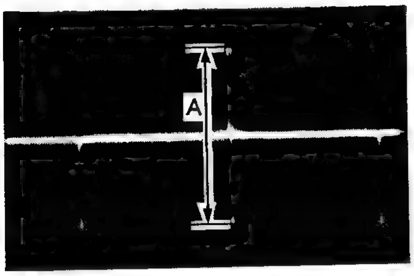
Connection :	See section 11-1.
Menu/switch settings :	See section 11-1 and text.
Mode of VTR :	PLAY
Instruments :	Oscilloscope
AUDIO LINE IN signal :	Don't care.

(1) Set the REC INHIBIT switches to ON.

(2) Conduct the following adjustment while playing back the 100% white section of the alignment tape.
For NTSC/PAL-M
TP505-E502/AP-15

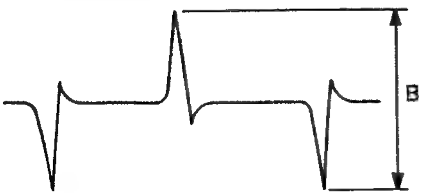


A=4±0.2V
⊘RV504/AP-15
For PAL/SECAM
TP505-E502/AP-15



A=3±0.2V
⊘RV504/AP-15

(3) This step applies only to the PAL/SECAM models.
Perform the following adjustment while playing back at VAR +50 the 100% white portion of the alignment tape.
TP505-E502/AP-15



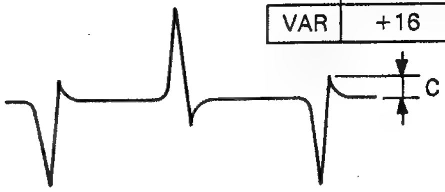
$$B = A \times \frac{4.5 \pm 0.3}{6}$$

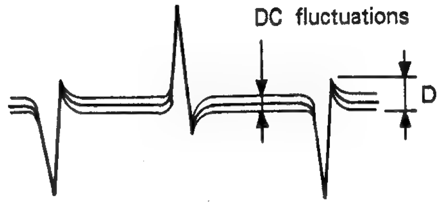
(A is the measurement value of step 2.)
⊘CT501/AP-15 (board suffix-11)
⊘RV505/AP-15 (board suffix-12)

Next, play back the portion at VAR (*1) and check the CTL waveforms as follows.
TP505-E502/AP-15

*1

	AP-15	
	suffix-11	suffix-12
VAR	+16	−32





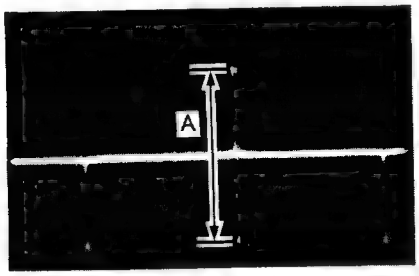
C≦0.18V
D≦0.25V
If the specifications are not satisfied, re-adjust ⊘ (*2) /AP-15 at the following specifications.

$$B = A \times \frac{4.2}{6}$$

*2

	AP-15	
	suffix-11	suffix-12
⊘	CT501	RV505

Perform the following confirmation while playing back the 100% white section of the alignment tape.
TP505-E502/AP-15



If this specifications are not satisfied, perform readjust from stop (2).

(4) Set the REC INHIBIT switches to OFF.

11-6. BIAS AMPLIFIER ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1.
Mode of VTR :	REC
Instruments :	Oscilloscope
AUDIO LINE IN signal :	Don't care.

Thread a recording tape, set the machine to the REC mode and proceed with the following adjustment.

TP1-E1/AP-15 : 4.0±0.5Vp-p
⊘RV1/AP-15
Note : LV1/AP-15 should not be touched.

11-7. ERASE CURRENT ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1.
Mode of VTR :	See text.
Instruments :	Oscilloscope
AUDIO LINE IN signal :	Don't care.

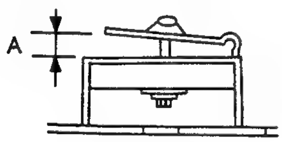
<u>(1) Audio erase current adjustment</u>

(1-1) Thread a recording tape, set the machine to the REC mode and adjust the levels at the following points to the maximum.

A1 TP101-E2 ⊘CT101 ⊘LV101/AP-15
A2 TP201-E2 ⊘CT201 ⊘LV201/AP-15
A3 TP301-E2 ⊘CT301 ⊘LV301/AP-15
A4 TP401-E2 ⊘CT401 ⊘LV401/AP-15

If "A" of CT101/201/301/401 in the figure below is more than 3mm, replace C101/201/301/401 with a 150pF or 330pF capacitor and re-adjust. If "A" is zero, replace C101/201/301/401 with a 470pF or 330pF capacitor and re-adjust.

CT101, 201, 301, 401



0<A<3mm

C101, 201, 301, 401
150pF/500V 1-109-627-00
330pF/500V 1-109-631-00
470pF/500V 1-109-633-00

(1-2) With the machine still in the REC mode, proceed with the following adjustments.

Level at points below=230±10Vp-p
A1 TP101-E2 ⊘RV101/AP-15
A2 TP201-E2 ⊘RV201/AP-15

(1-3) Play back the recorded portion and set the machine first to the A2 INSERT mode and then to the A1 INSERT mode. Adjust ⊘L206/AP-15 so that the following specifications are satisfied in each mode. If adjustment cannot be made by L206, use ⊘RV202/AP-15 also for the adjustment.

A2 INSERT mode : TP101-E2/AP-15 : ≦20Vp-p
A1 INSERT mode : TP201-E2/AP-15 : ≦20Vp-p

Repeat steps (1-2) and (1-3) and adjust.

(1-4) Proceed with the following adjustments in the REC mode :

Level of following points=230±10Vp-p
A3 TP301-E2 ⊘RV301/AP-15
A4 TP401-E2 ⊘RV401/AP-15

(1-5) Proceed with the following adjustments for the PS-A4 model.

Play back the recorded portion and set the machine first to the A4 INSERT mode and then to the A3 INSERT mode. Adjust ⊘L306/AP-15 so that the following specifications are satisfied in each mode. If adjustment cannot be made by L306, use ⊘RV302/AP-15 also for the adjustment.

A4 INSERT mode : TP301-E2/AP-15 : ≦20Vp-p
A3 INSERT mode : TP401-E2/AP-15 : ≦20Vp-p

Repeat steps (1-4) and (1-5) and adjust.

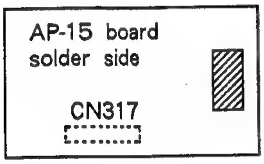
(2) Full erase or video erase current adjustment

Thread a recording tape, set the machine to the REC mode and proceed with the following adjustment.

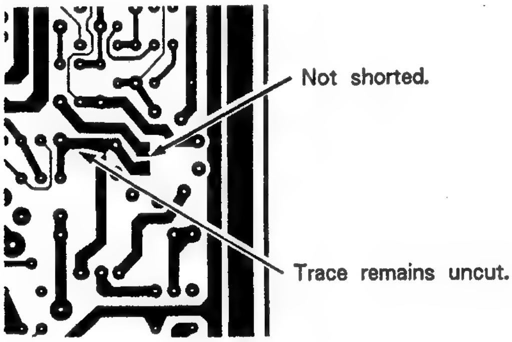
TP501-E501/AP-15 : Frequency=118±5kHz

(AP-15 board suffix-11)

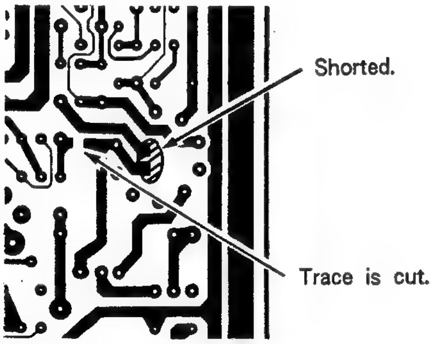
If the specifications are not satisfied, change the C501 or C505 constant. Only C501 or C505 is valid. Reference should be made to the figures below.



C501 is valid :



C505 is valid :



C501 or C505/AP-15

1800pF/500V 1-109-587-00
2000pF/500V 1-109-641-00
2200pF/500V 1-109-642-00
2400pF/500V 1-109-590-00
2700pF/500V 1-109-591-11

Next, adjust the level.

TP501-E501/AP-15 : Level=450±10mVp-p

⊘ RV501/AP-15

(AP-15 board suffix-12)

If the specifications are not satisfied, change the jumper socket JP501 to JP504.

(3) Sync erase current adjustment

This adjustment applies only to the PS (A3/A4) models.

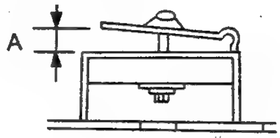
(3-1) Proceed with the following adjustments in the REC mode.

TP405-E401/AP-15 : Set to maximum level.

⊘ CT402/AP-15

If "A" of CT402 in the figure below is more than 3mm, replace C470/AP-15 with a 470pF or 680pF capacitor and re-adjust. If "A" is zero, replace C470 with a 750pF or 680pF capacitor and re-adjust.

CT402/AP-15



0<A<3mm

C470/AP-15

470pF/500V 1-109-633-00
680pF/500V 1-109-635-00
750pF/500V 1-109-636-00

(3-2) With the machine still in the REC mode, proceed with the following adjustments.

TP405-E401/AP-15 : 240±10mVp-p

(AP-15 board suffix-11)

If the specifications are not satisfied, change the R465 and R466/AP-15 constant. Make the resistance the same for both R465 and R466. The TP405 level is reduced when the resistance of R465 and R466 is increased.

R465, R466/AP-15

1 Ω	¼W	1-249-381-11	30 Ω	¼W	1-247-094-00
2.2 Ω	¼W	1-249-385-11	82 Ω	¼W	1-249-404-11
3.3 Ω	¼W	1-249-387-11	100 Ω	¼W	1-249-405-11
4.7 Ω	¼W	1-249-389-11	120 Ω	¼W	1-249-406-11
6.8 Ω	¼W	1-249-391-11	130 Ω	¼W	1-247-110-00
10 Ω	¼W	1-249-393-11	150 Ω	¼W	1-249-407-11
20 Ω	¼W	1-247-090-00			

(AP-15 board suffix-11)

If the specifications are not satisfied, perform the following adjustment.

⊘ RV401/AP-15 (PSA3)

⊘ RV402/AP-15 (PSA4)

11-8. CTL BIAS CURRENT ADJUSTMENT

Connection : 1	See section 11-1.
Menu/switch settings :	See section 11-1.
Mode of VTR :	REC
Instruments :	Oscilloscope
AUDIO LINE IN signal :	Don't care.

Thread a recording tape and proceed with the following adjustments in the REC mode.

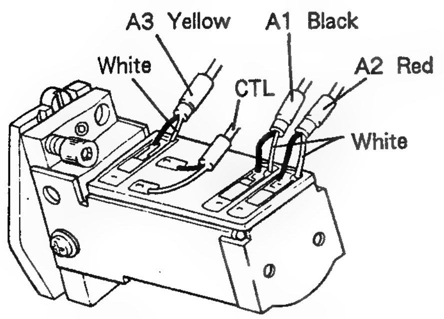
TP507-E503/AP-15 : Set the bias leak to minimum.
⊘LV504/AP-15
TP503-E2/AP-15 : Set the level to maximum.
⊘LV501/AP-15
TP502-E2/AP-15 : Set the level to maximum.
⊘L502/AP-15
TP502-E2/AP-15 : 150±10Vp-p
⊘RV502/AP-15

11-9. AUDIO BIAS ADJUSTMENT

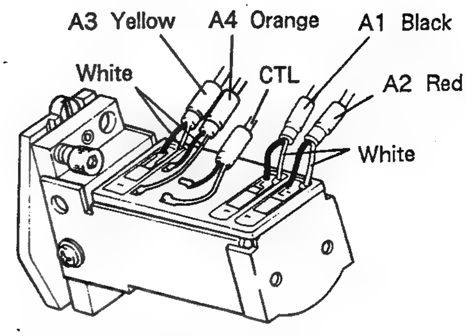
Connection :	See section 11-1.
Menu/switch settings :	See section 11-1.
Mode of VTR :	REC→PB
Instruments :	Oscilloscope
	Audio level meter
AUDIO LINE IN signal :	No signal
	→1kHz/ref. level

(1) Set the line input to the no-signal state, thread a recording tape and proceed to adjust the bias leak to the minimum in the REC mode.
A1 TP101-E503 ⊘LV104/AP-15
A2 TP202-E503 ⊘LV204/AP-15
A3 TP302-E503 ⊘LV304/AP-15
A4 TP402-E503 ⊘LV404/AP-15

(2) Proceed with the following adjustments in the REC mode with the line input still in the no-signal state.
Connect the oscilloscope to the white wire of the AUDIO R/P head and to the chassis and adjust the level to the maximum.
AUDIO R/P head
A3 model

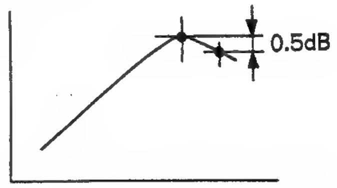


PS-A4 model



A1 ⊘L102/AP-15
A2 ⊘L202/AP-15
A3 ⊘L302/AP-15
A4 ⊘L402/AP-15

(3) Supply a 1kHz (reference level) signal to the AUDIO LINE IN connector. Rotate the bias level control on the BC-12 board counterclockwise as far as it will go and then proceed with recording while turning the control slowly clockwise. Play back the recorded portion, measure the AUDIO LINE OUT level, locate the point at which the peak is exceeded by 0.5dB, and then set the bias level control on the BC-12 board to the appropriate position.



A1 ⊘RV1/BC -12
A2 ⊘RV2/BC -12
A3 ⊘RV3/BC -12
A4 ⊘RV4/BC -12
(AP-15 board suffix-12 Only)
If you can't find the excess point by 0.5dB peak, change the following jumper sockets.
A1 : (JP101), JP102, JP103/AP-15
A2 : (JP201), JP202, JP203/AP-15
A3 : (JP301), JP302 /AP-15
A4 : (JP401), JP402, JP403/AP-15
( ) .... Factory sptting position.

11-10. RECORDING LEVEL ADJUSTMENT

Connection : See section 11-1.
Menu/switch settings : See section 11-1 and text.
Mode of VTR : See text.
Instruments : Audio level meter
AUDIO LINE IN signal : 1kHz/reference level

(1) Refer to steps (1) and (2) in section 11-3, check the REC level presettings and the line output levels and proceed to adjust them if they do not satisfy the specifications.

(2) Refer to step (3) in section 11-4, check the playback output levels and proceed to adjust them if they do not satisfy the specifications.

(3) Thread a recording tape, record a 1kHz (reference level) signal and measure the line output levels while playing back the recorded portion.
A1/A2/A3/A4
PB line output level=Ref. level±0.1dB
If the specifications are not satisfied, rotate the controls below slightly and measure the playback output levels. Repeat the adjustment (recording) and measurement (playback) until the specifications are satisfied.
A1 ⊘RV101/AU-88
A2 ⊘RV301/AU-88
A3 ⊘RV502/AU-88
A4 ⊘RV701/AU-88

11-11. CONFI. LEVEL ADJUSTMENT

Connection : See section 11-1.
Menu/switch settings : See section 11-1 and text.
Mode of VTR : See text.
Instruments : Audio level meter
AUDIO LINE IN signal : 1kHz/reference level

(1) Refer to steps (1) and (2) in section 11-3, check the REC level presettings and the line output levels, and proceed to adjust them if they do not satisfy the specifications.

(2) Refer to step (3) in section 11-4, check the playback output levels and proceed to adjust them if they do not satisfy the specifications.

(3) Set the $\boxed{\text{TAPE/IN}}$ key to TAPE.

(4) Select AUDIO 1, AUDIO 2 and AUDIO3/4 using the AUDIO MONITOR selectors on the level control panel and proceed with adjustment steps (5) and (6) for A1, A2 and A4.

(5) Set the REC INHIBIT switches to ON and, while playing back the 1kHz/0VU (or +8dBm) portion on the alignment tape, adjust the MONITOR PHONES level control on the level control panel.
AUDIO MONITOR OUTPUT=+8dBm
⊘MONITOR PHONES control

(6) Thread a recording tape, set the REC INHIBIT switches to OFF and, while recording the 1kHz (reference level) signal, proceed with the following adjustments.
AUDIO MONITOR OUTPUT=+8±0.1dBm
A1 ⊘RV110/AU-88
A2 ⊘RV310/AU-88
A4 ⊘RV710/AU-88

(7) Set the $\boxed{\text{TAPE/IN}}$ key to TAPE/EE.

11-12. RECORDING AMPLIFIER FREQUENCY RESPONSE ADJUSTMENT

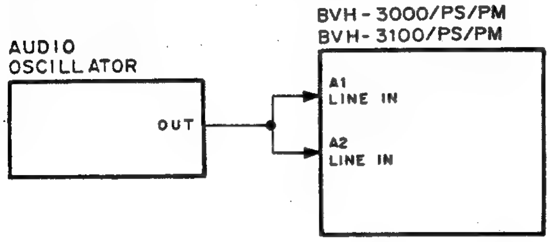
Connection : See section 11-1.
Menu/switch settings : See section 11-1.
Mode of VTR : REC→PB
Instruments : Audio level meter
AUDIO LINE IN signal : 1kHz, 10kHz
(10dB lower than ref. level)

Thread a recording tape, record the 1kHz and 10kHz (10dB lower than reference level) signals and, while playing them back, measure the line output level.
A1/A2/A3/A4 line output level
10kHz level=1kHz level ±0.5dB
If the specifications are not satisfied, rotate the controls below slightly, record the signal and measure the playback output level. Repeat the adjustment (recording) and measurement (playback) until the specifications are satisfied.
A1 ⊘RV102/AU-88
A2 ⊘RV302/AU-88
A3 ⊘RV503/AU-88
A4 ⊘RV702/AU-88

11-13. A1/A2 PHASE DIFFERENCE ADJUSTMENT

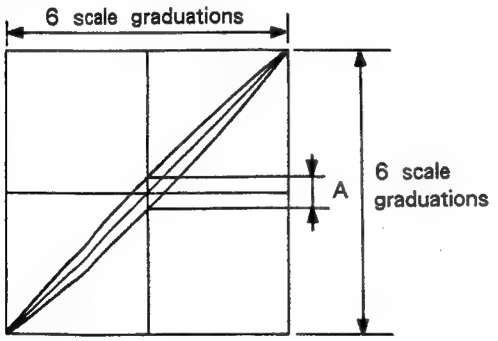
Connection :	See text.
Menu/switch settings :	See section 11-1.
Mode of VTR :	REC→PB
Instruments :	Oscilloscope
AUDIO LINE IN signal :	15kHz (reference level)

(1) Supply the 15kHz (reference level) signal to the A1 and A2 LINE IN connectors, as shown in the figure below.



(2) Thread a recording tape, record the signal and, while playing back the recording, and make the following measurements.
Connect the oscilloscope to TP103-E103/AU-88 and TP303-E303/AU-88 and produce the Lissajous figure.

TP103-E103/AU-88
TP303-E303/AU-88



A≦1 scale graduation
(max. 10° phase difference)

If the specifications are not satisfied, rotate ⊘RV313/AU-88 slightly, record the signal and then play it back, and make the same measurement as above. Repeat the adjustment (recording) and measurement (playback) until the specifications are satisfied.

11-14. REC-PB A1/A2, A3/A4 CROSSTALK ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1.
Mode of VTR :	See text.
Instruments :	Audio level meter
AUDIO LINE IN signal :	See text.

(1) REC A1→PB A2 crosstalk adjustment
Disconnect the A2 LINE IN connector and set the machine to the REC mode with no signals supplied to A2. Play back the recorded portion, set the machine to the A1 INSERT mode and adjust as follows.

When 1kHz (reference level) is supplied to A1 LINE IN :
A2 LINE OUT=Minimum level
⊘RV103/AU-88
When 15, 20 or 25kHz (reference level) is supplied to A1 LINE IN :
A2 LINE OUT≦Ref. level−15dB
⊘RV104 ⊘LV101/AU-88

(2) REC A2→PB A1 crosstalk adjustment
Disconnect the A1 LINE IN connector and set the machine to the REC mode with no signals supplied to A1. Play back the recorded portion, set the machine to the A2 INSERT mode and adjust as follows.

When 1kHz (reference level) is supplied to A2 LINE IN :
A1 LINE OUT=Minimum level
⊘RV303/AU-88
When 15, 20 or 25kHz (reference level) is supplied to A2 LINE IN :
A1 LINE OUT≦Ref. level−15dB
⊘RV304 ⊘LV301/AU-88

(3) REC A3→PB A4 crosstalk adjustment
Disconnect the A4 LINE IN connector and set the machine to the REC mode with no signals supplied to A4. Play back the recorded portion, set the machine to the A3 INSERT mode and adjust as follows.

When 1kHz (reference level) is supplied to A3 LINE IN :
A4 LINE OUT=Minimum level
⊘RV504/AU-88
When 15, 20 or 25kHz (reference level) is supplied to A3 LINE IN :
A4 LINE OUT≦Ref. level−15dB
⊘RV505 ⊘LV501/AU-88

(4) REC A4→PB A3 crosstalk adjustment
Disconnect the A3 LINE IN connector and set the machine to the REC mode with no signals supplied to A3. Play back the recorded portion, set the machine to the A4 INSERT mode and adjust as follows.

When 1kHz (reference level) is supplied to A4 LINE IN :
A3 LINE OUT=Minimum level
⊘RV703/AU-88

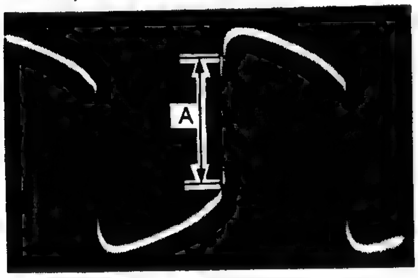
When 15, 20 or 25kHz (reference level) is supplied to A4 LINE IN :
A3 LINE OUT≦Ref. level−15dB
⊘RV704 ⊘LV701/AU-88

11-15. CTL RECORDING LEVEL ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1.
Mode of VTR :	REC→PLAY
Instruments :	Oscilloscope
AUDIO LINE IN signal :	Don't care.

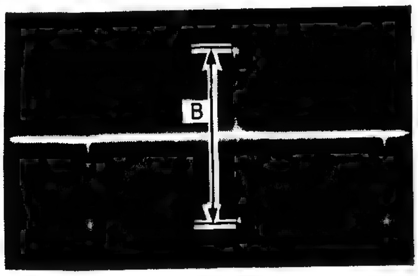
Thread a recording tape, record the signal and, while playing back the recorded portion, measure as below.

TP505-E502/AP-15
NTSC/PAL-M



A=4.0±0.2V

PAL/SECAM



B=3.0±0.2V

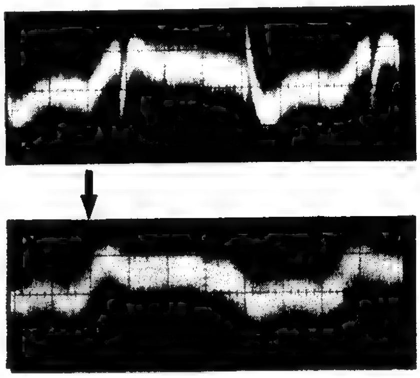
If the specifications are not satisfied, rotate ⊘RV503/AP-15 slightly, record the signals and then play them back, and make the same measurement as above. Repeat the adjustment(recording)and measurement (playback) until the specifications are satisfied.

11-16. AUDIO-CTL CROSSTALK ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1.
Mode of VTR :	See text.
Instruments :	Oscilloscope
AUDIO LINE IN signal :	See text.

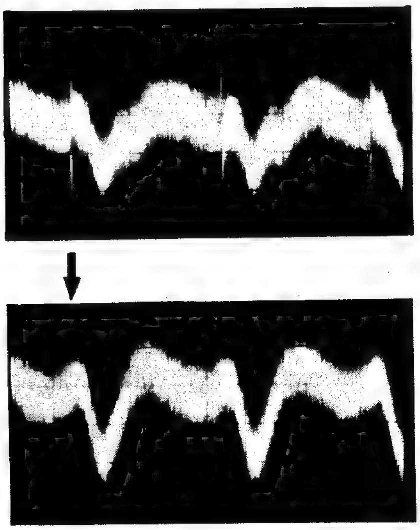
(1) PB CTL→PB A3/A4 crosstalk adjustment
Disconnect the A3 LINE IN connector and set the machine to the REC mode with no signals supplied to A3. Play back the recorded portion and set the machine to the A3 INSERT mode. While playing back the inserted portion, adjust as shown below.

A3 LINE OUT
NTSC/PAL-M



Minimize the crosstalk.
⊘RV716/AU-88

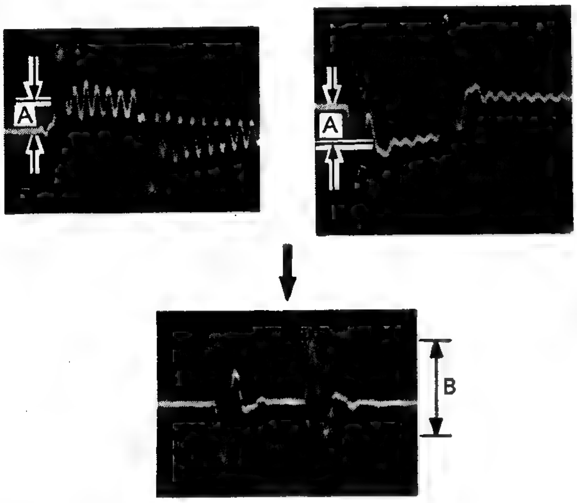
A3 LINE OUT (PS-A3 model)
A4 LINE OUT (PS-A4 model)
PAL/SECAM



Minimize the crosstalk.
⊘RV716/AU-88

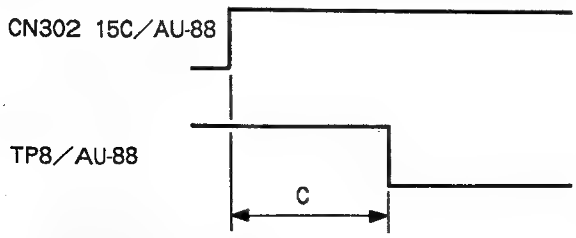
(2) REC CTL→PB A3/A4 crosstalk adjustment
(Note : This adjustment applies only to the PS-A3/A4 models.)
For the PS-A3 model, disconnect the A3 LINE IN connector and set the machine to the REC mode with no signals supplied to A3.
For the PS-A4 model, disconnect the A4 LINE IN connector and set the machine to the REC mode with no signals supplied to A4.
Play back the recorded portion, set the machine to the VIDEO ASSEMBLE mode and adjust as follows.

A3 LINE OUT (PS-A3 model)
A4 LINE OUT (PS-A4 model)



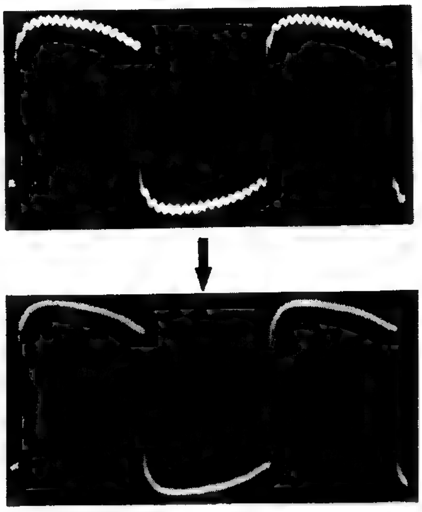
Minimize A (crosstalk).
⊘RV712/AU-88
B≦1.0V
⊘RV713 ⊘LV703/AU-88

(3) A4 cancel timing adjustment
(Note : This adjustment applies only to the PS-A4 model.)
Thread a recording tape and set the machine to the A4 INSERT mode. Every time the AUDIO 4 /SYNC button is now pressed in the INSERT mode, the INSERT mode is switched OFF and ON. Adjust the timing of the TP8/AU-88 pulse which appears when the INSERT mode is ON.

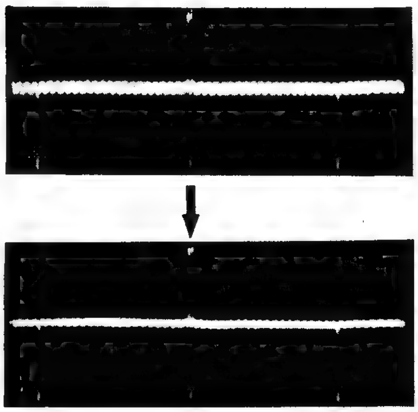


C=25±2ms
⊘RV718/AU-88

(4) REC A3/A4→PB CTL crosstalk adjustment
<u>For NTSC/PAL-M model</u>
Disconnect the A3 LINE IN connector and set the machine to the REC mode with no signals supplied to A3. Play back the recorded portion, supply the 1kHz (10dB higher than reference level) signal to the A3 LINE IN connector, set the machine to the A3 INSERT mode and adjust as below.
TP505-E502/AP-15



Minimize the crosstalk.
⊘RV714/AU-88
<u>For PS models</u>
With the PS-A3 model, disconnect the A3 LINE IN connector and set the machine to the REC mode with no signals supplied to A3. Play back the recorded portion, supply the 1kHz (10dB higher than reference level) signal to the A3 LINE IN connector, next supply the 15kHz (10dB higher than reference level) signal, set the machine to the A3 INSERT mode and adjust as below.
With the PS-A4 model, proceed with the same adjustment for the A4 channel.
TP505-E502/AP-15



Minimize the crosstalk.
1kHz : ⊘RV714/AU-88
15kHz : ⊘RV715 ⊘LV704/AU-88
Non signal : ⊘CT502/AP-15 (board suffix-12 only)

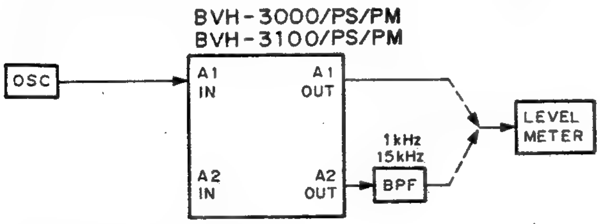
11-17. PB A1-A2, A3-A4 CROSSTALK ADJUSTMENT

Connection :	See text.
Menu/switch settings :	See section 11-1.
Mode of VTR :	See text.
Instruments :	Audio level meter
AUDIO LINE IN signal :	See text.

(1) Provide a bandpass filter with the specifications listed below.
[**Note**] Do not proceed with this adjustment if the band-pass filter cannot be provided.
1kHz bandpass filter
Q : More than 5
Attenuation : More than 12dB/oct
S/N ratio : Better than 70dB
15kHz bandpass filter
Q : More than 5
Attenuation : More than 12dB/oct
S/N ratio : Better than 70dB

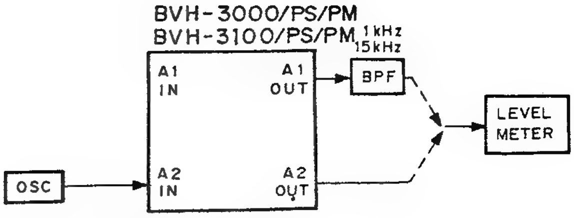
(2) Disconnect the A1 and A2 (and A3 and A4 for PS-A4) LINE IN connectors and set the machine to the REC mode with no signals supplied to either channel.

(3) PB A1→PB A2 crosstalk adjustment
Play back the portion recorded in step 2, set the machine to the A1 INSERT mode, supply the 1kHz and then 15kHz (10dB higher than reference level) signal to the A1 LINE IN connector.
While playing back the insert-recorded portion, measure/adjust the A1 LINE OUT and A2 LINE OUT levels. Measure the A2 LINE OUT level through the bandpass filter provided in step 1.



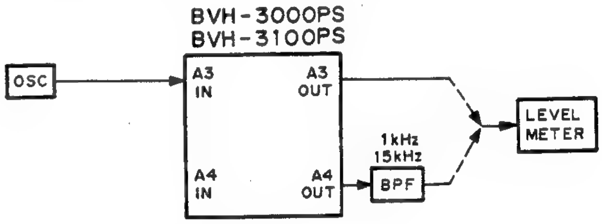
1kHz : A2≦A1−65dB
15kHz : A2≦A1−55dB
⊘RV105/AU-88

(4) PB A2→PB A1 crosstalk adjustment
Play back the portion recorded in step 2, set the machine to the A1 INSERT mode, supply the 1kHz and then 15kHz (10dB higher than reference level) signal to the A2 LINE IN connector.
While playing back the insert-recorded portion, measure/adjust the A1 LINE OUT and A2 LINE OUT levels. Measure the A1 LINE OUT level through the bandpass filter provided in step 1.



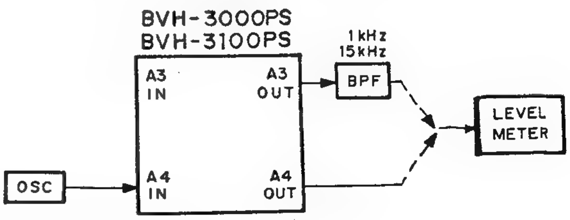
1kHz : A1≦A2−65dB
15kHz : A1≦A2−55dB
⊘RV305/AU-88

(5) PB A3→PB A4 crosstalk adjustment
(Note : This adjustment applies only to the PS-A4 model.)
Play back the portion recorded in step 2, set the machine to the A3 INSERT mode, supply the 1kHz and then 15kHz (10dB higher than reference level) signal to the A3 LINE IN connector.
While playing back the insert-recorded portion, measure/adjust the A3 LINE OUT and A4 LINE OUT levels. Measure the A4 LINE OUT level through the bandpass filter provided in step 1.



1kHz : A4≦A3−65dB
15kHz : A4≦A3−55dB
⊘RV506/AU-88

(6) PB A4→PB A3 crosstalk adjustment
(Note : This adjustment applies only to the PS-A4 model.)
Play back the portion recorded in step 2, set the machine to the A4 INSERT mode, supply the 1kHz and then 15kHz (10dB higher than reference level) signal to the A4 LINE IN connector.
While playing back the insert-recorded portion, measure/adjust the A3 LINE OUT and A4 LINE OUT levels. Measure the A3 LINE OUT level through the bandpass filter provided in step 1.



1kHz : A3≦A4−65dB
⊘RV705/AU-88
15kHz : A3≦A4−55dB
⊘RV507/AU-88

11-18. MONITOR AMPLIFIER FREQUENCY RESPONSE ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1 and text.
Mode of VTR :	See text.
Instruments :	Audio level meter
AUDIO LINE IN signal :	See text.

(1) Set the AUDIO MONITOR selector on the level control panel to AUDIO 1 and proceed with the adjustments from step 2 through step 5 for A1. Next, set the AUDIO MONITOR selector to AUDIO 2 and AUDIO 3/4 and adjust from step 2 through step 5 for A2 and A4.

(2) Set the [TAPE/IN] key to TAPE/EE. Set the REC INHIBIT switches to ON and play back the 1kHz/0VU (or +8dBm) signal on the alignment tape. Adjust AUDIO MONITOR OUT to +8dBm using the MONITOR PHONES control on the level control panel.

(3) Thread a recording tape and set the REC INHIBIT switches to OFF. Supply the 10kHz, 50Hz and 100Hz (10dB lower than reference level) signals to the LINE IN connector, and record and play back each of the signals. Measure the playback level at AUDIO MONITOR OUT.

(4) Set the [TAPE/IN] key to TAPE. Supply the 10kHz (10dB lower than reference level) signal to the LINE IN connector and, while recording it, check the AUDIO MONITOR OUT level. Proceed with adjustment if the following specifications are not satisfied.

Level at step 4=Level at step 3 ±1dB
A1 ⊘RV108/AU-88
A2 ⊘RV308/AU-88
A4 ⊘RV708/AU-88

(5) Supply the 50Hz and 100Hz (10dB lower than reference level) signals to the LINE IN connector, and while recording them, check the AUDIO MONITOR OUT level. Proceed with adjustment if the following specifications are not satisfied.

Level at step 5=Level at step 3 ±1dB
(for both 50Hz, 100Hz signals)
A1 ⊘RV109/AU-88
A2 ⊘RV309/AU-88
A4 ⊘RV709/AU-88

(6) After adjusting A1, return to step 1, adjust for A2 and then adjust for A4.

(7) Set the [TAPE/IN] key to TAPE/EE.

11-19. TIME CODE DUTY ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1 and text.
Mode of VTR :	See text.
Instruments :	Oscilloscope
AUDIO LINE IN signal :	1kHz/ref. level (A3)

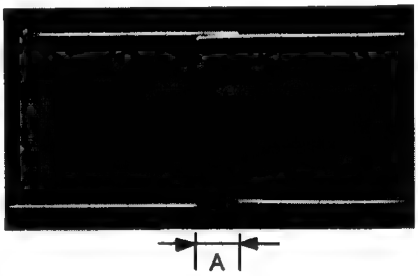
(1) Supply the 1kHz (reference level) signal to the A3 LINE IN connector.

(2) Set the menus and switches as follows :

S50. A3 INPUT SELECT : TC
S51. TIME CODE SOURCE : EXT
TAPE/IN key : TAPE/EE

Set the machine to the STOP mode and press the INPUT button on the control panel. A3 is set to the EE mode.
Connect the oscilloscope to TP505-E503/AU-88.
Set the oscilloscope to 0.1ms/DIV (10μs/DIV/DELAY) and to internal trigger and, while switching the trigger slope between + and −, proceed with the adjustment.

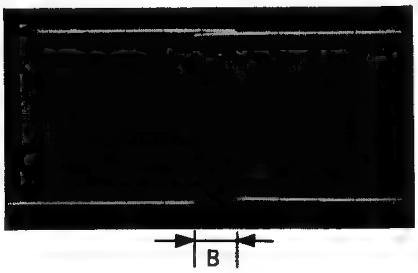
TP505-E503/AU-88



A≦5μs
⊘RV516/AU-88

(3) Set the S50 menu to LINE and set the machine to the REC mode. Set the S50 menu to TC and play back the recorded portion. Connect the oscilloscope to TP508-E503/AU-88 and, while switching the trigger slope between + and −, proceed with the adjustment.

TP508-E503/AU-88



B≦5μs
⊘RV518/AU-88

11-20. TIME CODE LEVEL ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1 and text.
Mode of VTR :	STOP
Instruments :	Audio level meter Oscilloscope
AUDIO LINE IN signal :	1kHz/ref. level (A3)

(1) Supply the 1kHz (reference level) signal to A3 LINE IN.

(2) Set the menus and switches as follows :
S50. A3 INPUT SELECT : TC
S51. TIME CODE SOURCE : EXT
TAPE/IN key : TAPE/EE
Set the machine to the STOP mode and press the INPUT button on the control panel. A3 is set to the EE mode.

(3) Output level adjustment
A3 LINE OUT=Ref. level±0.1dB
RV520/AU-88

(4) Recording level adjustment
TP507-E504 : 150±5mVp-p
RV517/AU-88

(5) Set the menus as follows :
S51. TIME CODE SOURCE : INT
S50. A3 INPUT SELECT : LINE

11-21. REC BIAS LEAK ADJUSTMENT

Connection :	See section 11-1.
Menu/switch settings :	See section 11-1 and text.
Mode of VTR :	See text.
Instruments :	Oscilloscope
AUDIO LINE IN signal :	No-signal

(1) Disconnect the A1, A2, A3 and A4 LINE IN connectors and set the machine to the REC mode.

(2) A1→A2 bias leak adjustment
Play back the portion recorded in step 1, set the machine to the A1 INSERT mode and adjust as follows.
A2 LINE OUT : Bias leak=minimum
LV302/AU-88

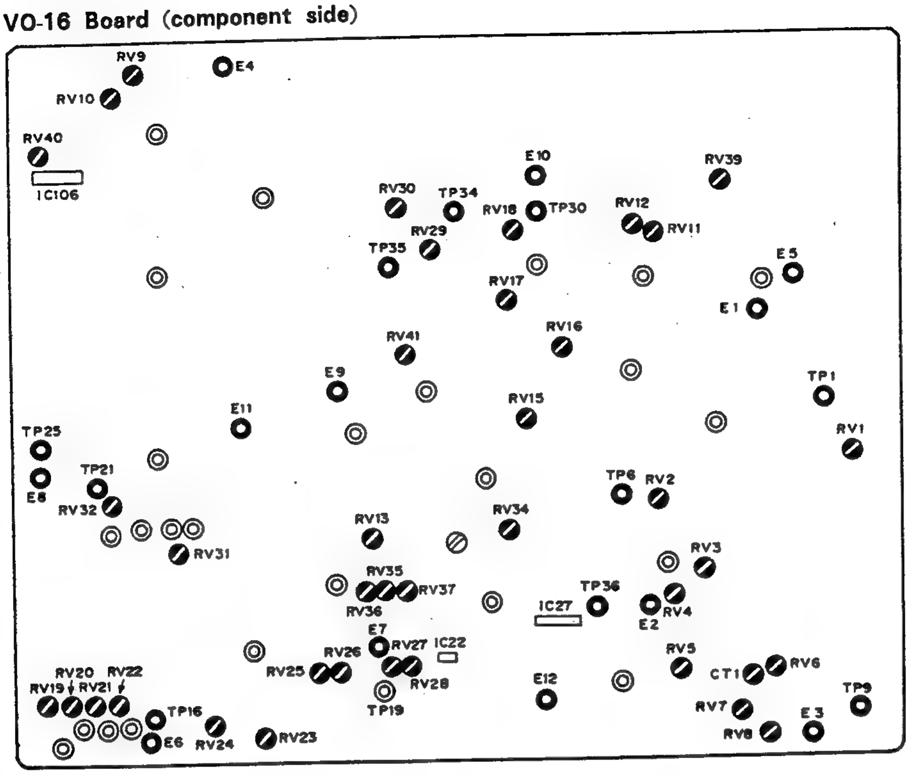
(3) A2→A1 bias leak adjustment
Play back the portion recorded in step 1, set the machine to the A2 INSERT mode and adjust as follows.
A1 LINE OUT : Bias leak=minimum
LV102/AU-88

(4) A1 and 2→A3 bias leak adjustment
Play back the portion recorded in step 1, set the machine to the A1 and 2 INSERT mode and adjust as follows.
A3 LINE OUT : Bias leak=minimum
LV502/AU-88

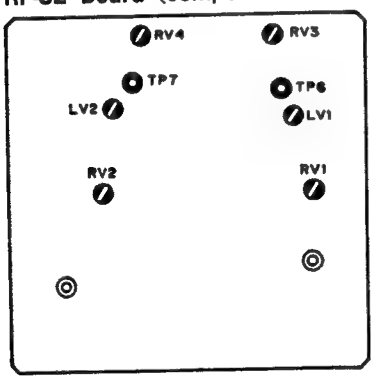
(5) A1, 2 and 3→A4 bias leak adjustment
Play back the portion recorded in step 1, set the machine to the A1, 2 and 3 INSERT mode and adjust as follows.
A4 LINE OUT : Bias leak=minimum
LV702/AU-88

SECTION 12
VIDEO SIGNAL SYSTEM ALIGNMENT

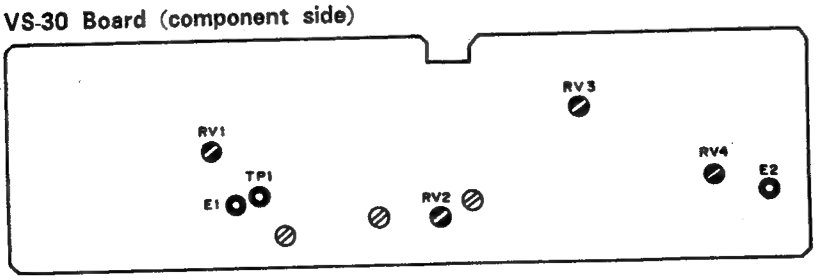
VO-16 Board (component side)



RP-32 Board (component side)

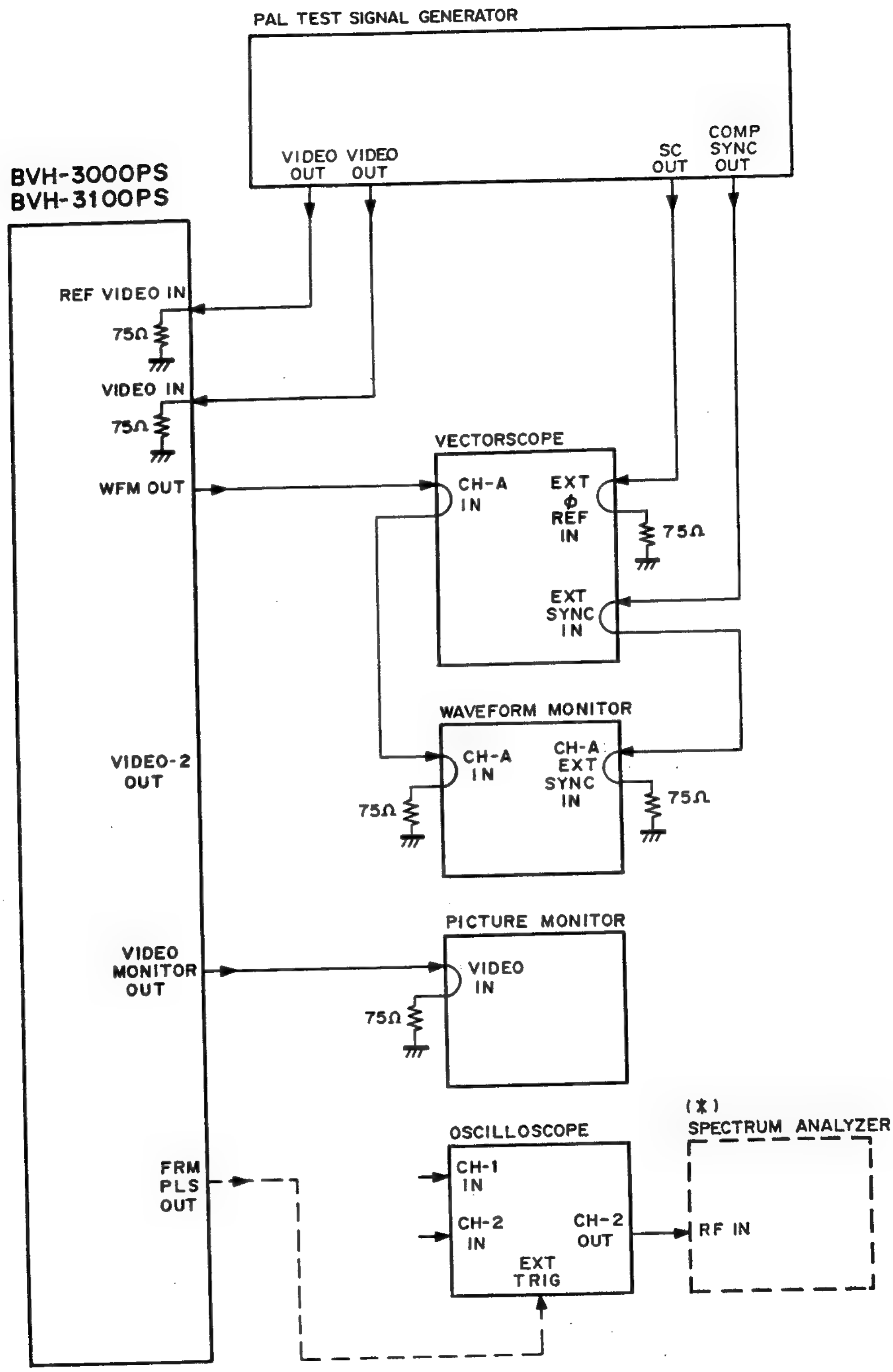


VS-30 Board (component side)



12-1. ADJUSTMENT PREPARATIONS

(1) Equipment connection



* Spectrum analyzer

This is used in sections 12-8, 12-16 and 12-20. When it is not available, the 12-8 adjustment can still be performed using a vectorscope, though the adjustments are not so precise.

(2) **Menu/switch settings**

Level control panel
- VIDEO level control : preset
- TRACKING control : preset
- EQUALIZER control : MANUAL (mechanical center)
- REMOTE/LOCAL switch : LOCAL

Function control panel
- TAPE/IN key : TAPE/EE

Menu

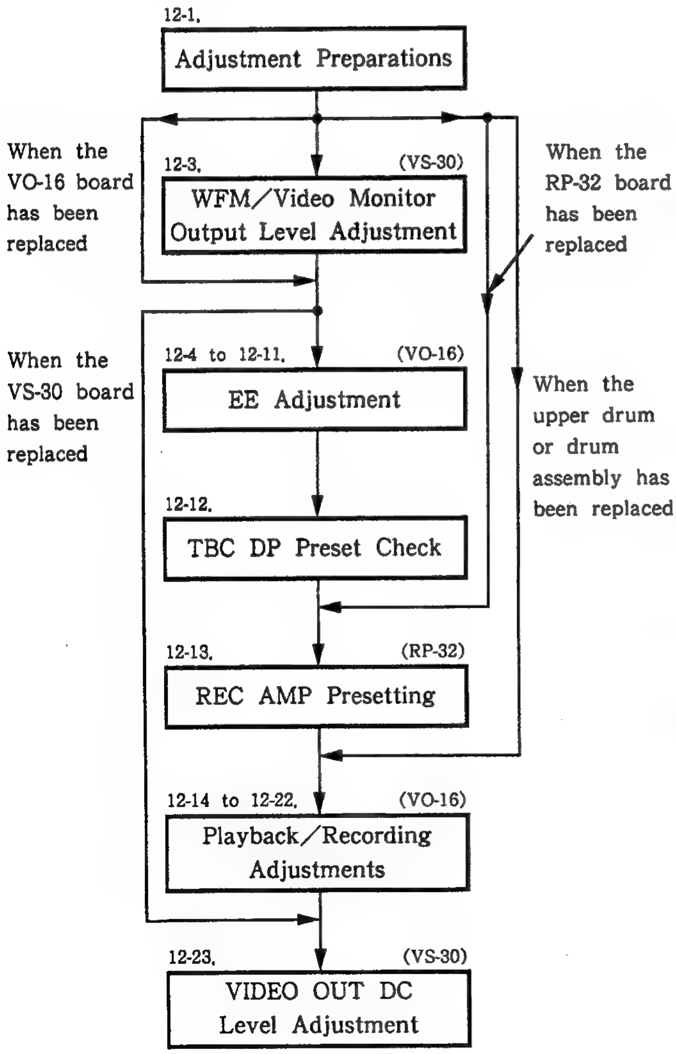
Using the following key operations, load the default menu selection data on the PROM (data in unit at time of shipment) into the RAM.

[SETUP] → [T] → [0] → [SET]

Also, set menu S89 as follows.

S89. TV STANDARD : PAL

12-2. ADJUSTMENT SEQUENCE



12-3. WFM/VIDEO MONITOR OUTPUT LEVEL ADJUSTMENT

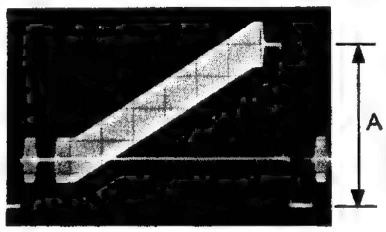
Connection :	See section 12-1 and text.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope Waveform monitor
VIDEO IN signal :	PAL RAMP LINEARITY

(1) Remove the MA-26 board and open the power supply section so that the VS-30 board can be inspected. Refer to section 2-5.

(2) Menu settings
- S02. PICTURE MONITOR : INPUT
- S03. WFM SELECT : SELECT

(3) Input level adjustment

TP1/VS-30



A=0.50±0.01V

⊘ RV1/VS-30

(4) WFM output level adjustment

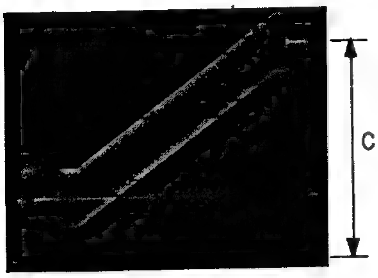
Supply the WFM output signal of the VTR to the waveform monitor. Refer to section 12-1.

WFM OUT/connector panel

B=1.00±0.01V

⊘ RV4/VS-30

(5) Video monitor output level adjustment
Supply the [MONITOR OUT VIDEO] output signal of the VTR to the waveform monitor.
MONITOR OUT VIDEO/connector panel



C=1.00±0.01V
⊘RV3/VS-30

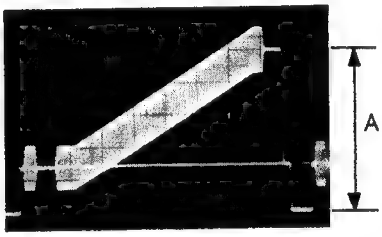
(6) Return the equipment connections to the status indicated in section 12-1.

(7) Close the power supply section and replace the MA-26 board in the VTR.

12-4. VIDEO INPUT LEVEL/METER ADJUSTMENT

Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL RAMP LINEARITY

(1) Draw out the function control panel so that the preset controls on the bottom of the level control panel can be adjusted. Refer to section 2-4-2 of the Operation Manual.
(2) Set the VIDEO level preset control (RV-15/VR-51) on the bottom of the level control panel to the mechanical center point.
Check that the VIDEO level control (RV16/VR-51) on the level control panel has been pushed in.
(3) Use an extension circuit board to draw out the VO-16 board and proceed with the following adjustments.
TP1/VO-16



A=1.00±0.01V
⊘RV39/VO-16

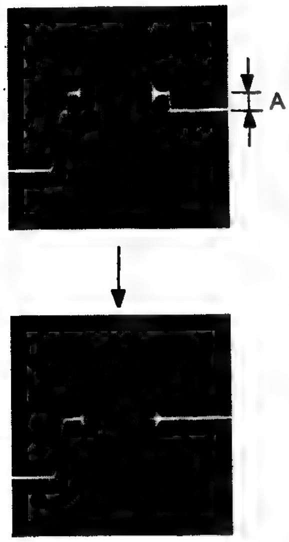
(4) Set the menu [S80: VIDEO METER SELECT] to [INPUT] and adjust as follows :
VIDEO meter pointer indication : 100±3%
⊘RV11/VO-16

(5) Check that the VIDEO meter pointer indicates 100±10% when the VIDEO level control has been set to its mechanical center point and pulled out.
NO : Insert the VO-16 board without the extension circuit board, and adjust the VIDEO level preset control so that the VIDEO meter pointer indicates the same level both when the VIDEO level control has been pushed in and when it is pulled out.
Now return to step (3) and repeat the adjustments in steps (3), (4) and (5).
YES : Keep the VIDEO level control pushed in.

12-5. BURST DC LEVEL ADJUSTMENT

Connection :	See section 12-1.
Menu/switch settings :	See section 12-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL RAMP LINEARITY

Adjustment
TP-6/VO-16

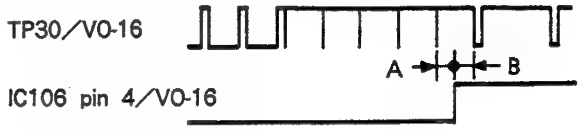


A=0±20mV
⊘RV1/VO-16

12-6. FM DEVIATION ADJUSTMENT

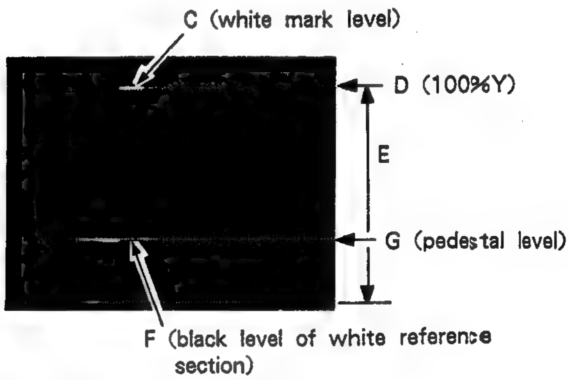
Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope Waveform monitor
VIDEO IN signal :	PAL RAMP LINEARITY

(1) White reference timing adjustment



A=B ⊘RV40/VO-16

(2) FM deviation adjustment
ⓐSet the menu [S02. PICTURE MONITOR] to DEMOD.
ⓑSet the menu [S82. WHITE REFERENCE] to ON.
ⓒAdjust RV2, 16 and 15 as indicated below.
WFM OUT/connector panel



D=C	⊘RV2/VO-16
E=1.0±0.01V	⊘RV16/VO-16
F=G	⊘RV15/VO-16

ⓓReturn the menu [S82. WHITE REFERENCE] to OFF.

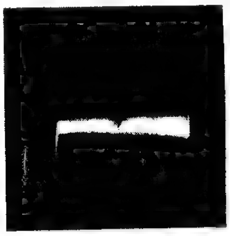
12-7. EE DG/DP ADJUSTMENT

Connection : See section 12-1.
Menu/switch settings : See section 12-1 and text.
Mode of VTR : STOP (EE)
Instrument : Vectorscope
VIDEO IN signal : PAL RAMP LINEARITY

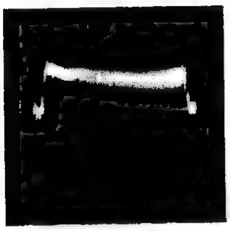
(1) Set the menus as follows :
S02. PICTURE MONITOR : DEMOD
S03. WFM SELECT : SELECT

(2) Adjust as follows.
WFM OUT/connector panel

DG



DP



DG : Less than 1%
DP : Less than 1°
⊘RV4/VO-16

12-8. EE MOIRE ADJUSTMENT

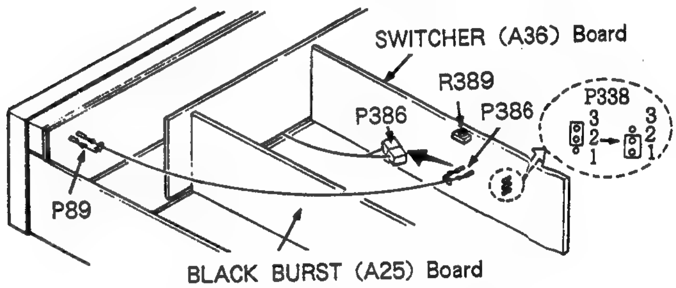
Connection : See section 12-1.
Menu/switch settings : See section 12-1 and text.
Mode of VTR : STOP (EE)
Instrument : Spectrum analyzer (or vectorscope)
VIDEO IN signal : Moire signal (see text) (or PAL RAMP LINEARITY)

When a spectrum analyzer can be used, proceed with the adjustment according to method A ; if such an instrument cannot be used, use a vectorscope and adjust according to method B.

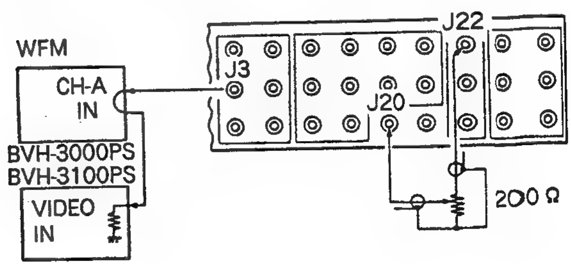
<u>(A) When a spectrum analyzer can be used</u>

(A-1) Generating the moire signal
Change the plug and connector connections inside the Tektronix 1411 test signal generator as instructed below.

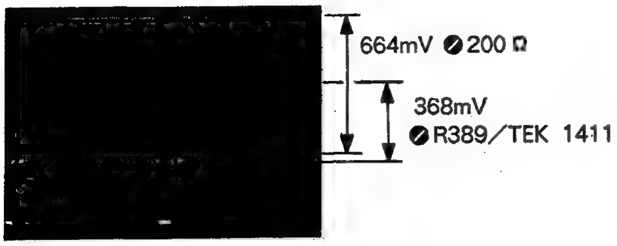
- Disconnect shorting plug P338 on the SWITCHER board from 2-3 and re-connect it to 2-1, as shown in the figure below.
- Disconnect connector P386 on the SWITCHER board, and connect the shielding wire between P386 and P89, as shown in the figure below.



Make the connections as shown in the figure below.

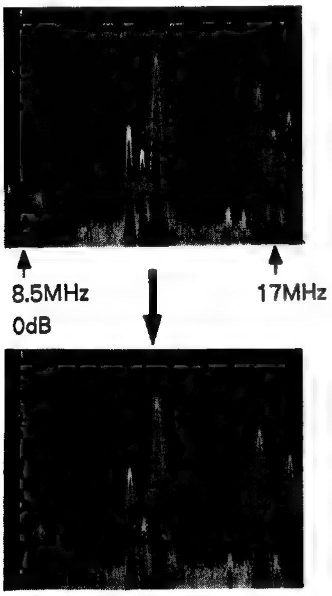


Set the signal selector of the Tektronix TSP1 unit to BLACK BURST and observe the resulting waveforms on the waveform monitor. Use R389 on the SWITCHER board (Tektronix 1411/TSP11) and the 200 Ω control in the above figure to adjust the moire signal so that it appears as shown below.
Moire signal (on waveform monitor)



(A-2) Equipment connections
Refer to section 12-1 and connect the equipment, and then supply the moire signal to the VIDEO IN connector. Supply the output signal of the oscilloscope to the spectrum analyzer.

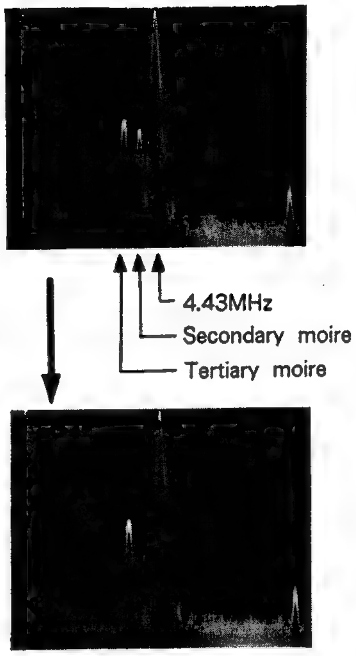
(A-3) Modulator secondary moire adjustment
TP36 (=pin 3/IC27) /VO-16

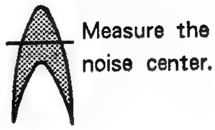


Adjust and set the spectrum analyzer so that the 8.5MHz level is brought to 0dB, then adjust as follows.

Set the 17MHz level to its minimum (less than −48dB).
⊘RV3/VO-16

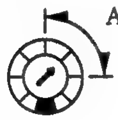
(A-4) Demodulator moire adjustment
TP30/VO-16





Adjust and set the spectrum analyzer so that the 4.43MHz level is brought to 0dB, then adjust as follows.

Reduce the secondary moire to the minimum (less than −45dB). Repeatedly adjust ⊘RV34 and ⊘RV37/VO-16 to minimize the secondary moire. Finally, reduce it even further by rotating ⊘RV3/VO-16 within a range of not more than ±1 gradation.



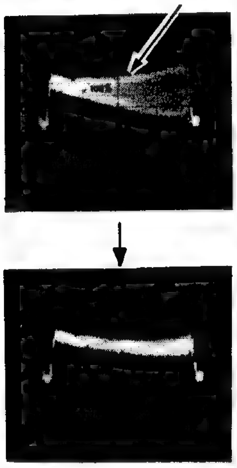
(B) When a spectrum analyzer cannot be used

(B-1) Menu settings
Set the menus as follows :

S02. PICTURE MONITOR :	DEMOD
S03. WFM SELECT :	SELECT

(B-2) Equipment connections
Refer to section 12-1 and connect the equipment, and then supply the RAMP LINEARITY signal to the VIDEO IN connector. Set the vectorscope to the DP mode and observe the WFM OUT signal.

(B-3) Adjustments
WMF OUT/connector panel

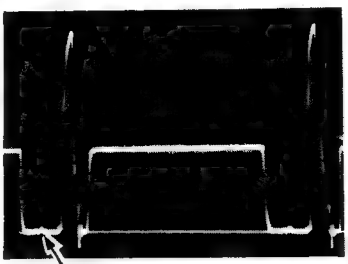


First set ⊘RV3, ⊘RV34 and ⊘RV37/VO-16 to their mechanical center points and then repeatedly adjust these three controls so that the moire is reduce to the minimum.

12-9. BURST DETECTION ADJUSTMENT

Connection :	See section 12-1.
Menu/switch settings :	See section 12-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL video signal

Adjustment
TP34/VO-16



⊘RV18/VO-16

TP35/VO-16
2.0±0.05Vdc
⊘RV17/VO-16

12-10. DE-EMPHASIS ADJUSTMENT

Connection : See section 12-1.
Menu/switch settings : See section 12-1 and text.
Mode of VTR : STOP (EE)
Instrument : Waveform monitor
VIDEO IN signal : PAL MULTIBURST

(1) Menu settings
Set the menus as follows :
S02. PICTURE MONITOR : DEMOD
S03. WFM SELECT : SELECT

(2) Adjustment
Although the demodulator output signal is output from the WFM OUT connector, the input video signal will be output when the [INPUT] button on the function control panel is pressed and it is output for as long as this button is kept depressed.
Pay attention to the 100% white section of the multiburst signal on the waveform monitor screen. While switching the [INPUT] button to ON and OFF, adjust ⊘ RV41/VO-16 so that the waveforms of the demodulator output signal and the waveforms of the input video signal are made the same.

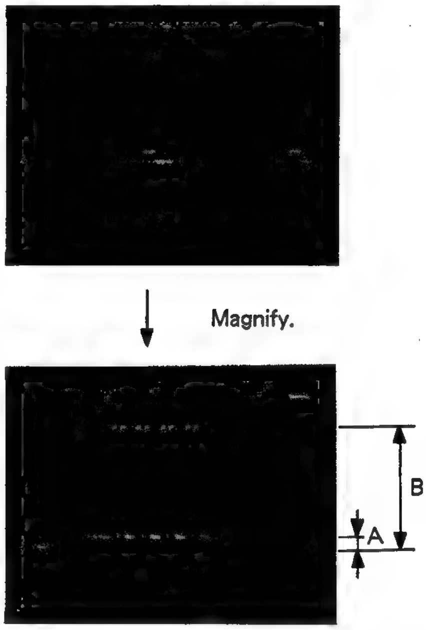
When RV41 is rotated, the waveforms change as shown in the figures below.
WFM OUT/connector panel

12-11. CHARACTER LEVEL ADJUSTMENT

Connection : See section 12-1.
Menu/switch settings : See section 12-1 and text.
Mode of VTR : STOP (EE)
Instrument : Waveform monitor
VIDEO IN signal : PAL RAMP LINEARITY

(1) Menu settings
Set the menus as follows :
S59. MIXED CHARA OUTPUT : MONITOR
S02. PICTURE MONITOR : DEMOD
S03. WFM SELECT : SELECT

(2) Adjustment
WFM OUT/connector panel



A=0.05±0.01V ⊘RV10/VO-16
B=0.57±0.05V ⊘RV9/VO-16

(3) Menu resetting
Set the menu [S59. MIXED CHARA OUTPUT] to DISABLE.

12-12. TBC DP PRESET CHECK

Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Vectorscope
VIDEO IN signal :	PAL RAMP LINEARITY

(1) Menu settings
Set the menus as follows :
S02. PICTURE MONITOR : TBC OUT
S03. WFM SELECT : SELECT

(2) TBC DP preset check
Set the menu to the test mode. Check the difference in the TBC OUT DP/DG between when the test menu [T11. DP VIDEO] is set ON and when it is set OFF.
DG : Less than 1%
DP : Less than 1°

(3) Set the test menu T11 to OFF.
Measure the TBC OUT differential gain and phase.
DG : Less than 2%
DP : Less than 1°
If the values are within the specifications, proceed to section 12-13. If they are not, inspect and adjust the TBC system (see section 14).

12-13. REC AMP PRESETTING

Leave the following controls set in the positions applying before the VTR was shipped from the factory. Set them to their mechanical center point when they have been adjusted in error or replaced.
⊘RV1/RP-32 Mechanical center point
⊘RV2/RP-32 Mechanical center point
(RV2 is provided only on the BVH-3000PS.)

12-14. PROVISIONAL RF LEVEL ADJUSTMENT

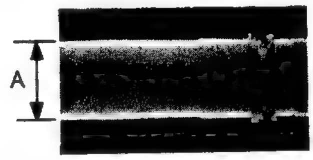
Note : This provisional adjustment is conducted to facilitate the adjustments outlined in section 12-15 and following. Proceed according to the instructions in section 12-21 for the final adjustment.

Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	PLAY
Instrument :	Oscilloscope
VIDEO IN signal :	PAL video signal

(1) Set the REC INHIBIT switches on the level control panel to the following positions.
REC INHIBIT switch, VIDEO : ON
REC INHIBIT switch, AUDIO : ON

(2) Proceed with the following adjustments while playing back the color bar signal of the alignment tape.

(3) Set the menu [S80. VIDEO METER SELECT] to RF (V), select the R/P head using the PLAY/IN key on the 21-key section and adjust as follows.
TP16/VO-16



A=100±20mV ⊘RV19/VO-16

(4) Change the meter display with menu [S80] as shown in the table below, select the playback head using the PLAY/IN key and adjust the meter indication.

	Meter selection Menu S80.	Playback head selection PLAY/IN key	Meter indication adjustment
1.	RF (V)	R/P	100±3% ⊘RV12/VO-16
2.	RF (V)	PLAY	100±3% ⊘RV21/VO-16
3.	RF (S) (Does not apply to BVH-3100PS)	R/P	100+3/−20% ⊘RV20/VO-16
4.	RF (S) (Does not apply to BVH-3100PS)	PLAY	100+3/−20% ⊘RV22/VO-16

(5) Set menu [S80] to RF (V).

12-15. PLAYBACK FREQUENCY RESPONSE AND DG/DP ADJUSTMENT

Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	PLAY
Instrument :	Waveform monitor Vectorscope
VIDEO IN signal :	PAL video signal

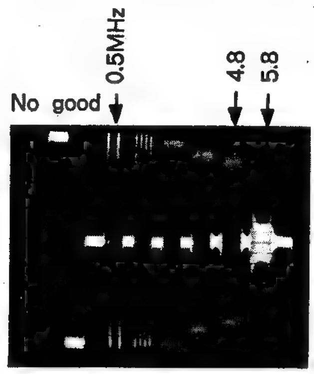
(1) Set the REC INHIBIT switches and EQUALIZER control on the level control panel to the following positions.
REC INHIBIT switch, VIDEO : ON
REC INHIBIT switch, AUDIO : ON
EQUALIZER control : MANUAL (mechanical center point)

(2) Set ⊘RV30/VO-16 to the position shown in the figure below.

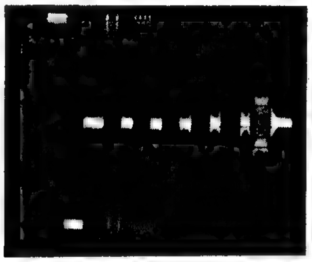
(3) Playback frequency response adjustment (R/P head)
Set the menus and switches as follows :
S02. PICTURE MONITOR : DEMOD
S03. WFM SELECT : SELECT
PB head ($\boxed{\text{PLAY/IN}}$ key) : R/P
Play back the multiburst signal on the alignment tape and adjust the frequency response.

WFM OUT/connector panel

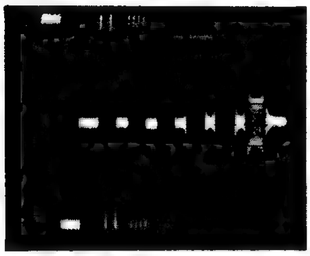
No good



No good



Good



$$\frac{4.8\text{MHz amplitude}}{0.5\text{MHz amplitude}} = \frac{100^{+3}_{-5}}{100}$$

$$\frac{5.8\text{MHz amplitude}}{0.5\text{MHz amplitude}} \leqq \frac{35}{100}$$

⊘RV28/VO-16

(4) Playback DG/DP adjustment (R/P head)
Set menu S02 as follows:
S02. PICTURE MONITOR: TBC OUT
Play back the LINEARITY signal on the alignment tape and adjust the DG/DP.

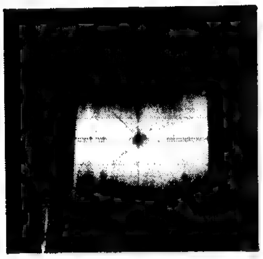
WFM OUT/connector panel

DG

No good

No good

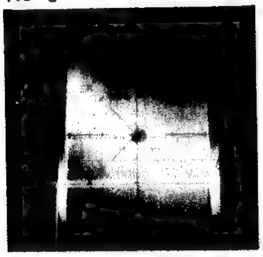
Good



Set the DG to the minimum (less than 4%).
⊘RV23/VO-16

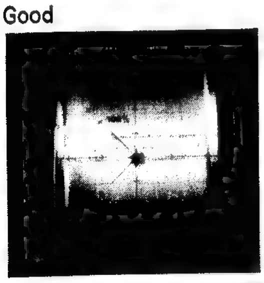
DP

No good



No good

Good



Set the DP to the minimum (less than 4°).
⊘RV26/VO-16

(5) Repeat steps (3) and (4) until the frequency response, DG and DP meet the specifications.

(6) Playback frequency response adjustment (PLAY head)
Set the menus and switches as follows:
S02. PICTURE MONITOR: DEMOD
S03. WFM SELECT: SELECT
PB head ($\boxed{\text{PLAY/IN}}$ key): PLAY
Adjust the frequency response in the same way as instructed in step (3).

$$\frac{4.8\text{MHz amplitude}}{0.5\text{MHz amplitude}} = \frac{100^{+3}_{-5}}{100}$$

$$\frac{5.8\text{MHz amplitude}}{0.5\text{MHz amplitude}} \leq \frac{35}{100}$$

⊘RV27/VO-16

(7) Playback DG/DP adjustment (PLAY head)
Set menu S02 as follows:
S02. PICTURE MONITOR: TBC OUT
Adjust the DG/DP in the same way as instructed in step (4).
Set the DG to the minimum (less than 4%).
⊘RV24/VO-16
Set the DP to the minimum (less than 4°).
⊘RV25/VO-16

(8) Repeat steps (6) and (7) until the frequency response, DG and DP meet the specifications.

12-16. PLAYBACK MOIRE ADJUSTMENT

Connection:	See section 12-1.
Menu/switch settings:	See section 12-1 and text.
Mode of VTR:	PLAY
Instrument:	Spectrum analyzer (or vectorscope)
VIDEO IN signal:	PAL video signal

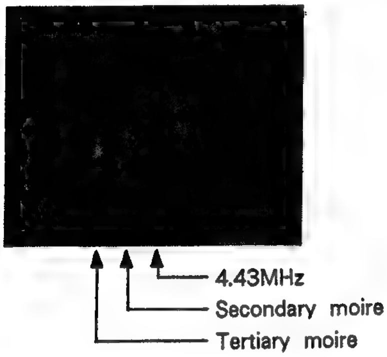
(1) Menu/switch settings
Set the menus and switches as follows:
S02. PICTURE MONITOR: TBC OUT
S03. WFM SELECT: SELECT
REC INHIBIT switch, VIDEO: ON
REC INHIBIT switch, AUDIO: ON

(2) Set the controls below to their mechanical center points.
⊘RV13/VO-16
⊘RV35/VO-16
⊘RV36/VO-16

(3) When a spectrum analyzer can be used, proceed with the adjustment according to method A ; if such an instrument cannot be used, use a vectroscope and adjust according to method B.

(A) When a spectrum analyzer can be used

(A-1) Select the R/P head using the [PLAY/IN] key. Play back the COLOR BAR signal on the alignment tape.
WFM OUT/connector panel



Adjust and set the spectrum analyzer so that the 4.43MHz level is brought to 0dB.

(A-2) Measure the tertiary moire when the COLOR BAR signal is played back both by the R/P head and PLAY head and check that the measured values come within the specifications.

Tertiary moire ≦−35dB

If the measured value does not meet the specifications, turn ⊘RV30/VO-16 clockwise one gradation. If ⊘RV30 is adjusted, the following adjustment must be performed again.
Section 12-15. Playback frequncy response and DG/DP adjustment

(A-3) Select the R/P head and adjust as follows.
Secondary moire=minimum
⊘RV13/VO-16

Secondary moire≦−35dB
⊘RV35/VO-16

(A-4) Select the PLAY head and adjust as follows.
Secondary moire≦−35dB
⊘RV36/VO-16

(B) When a spectrum analyzer cannot be used
(Using a vectorscope)

[CAUTION]
This method cannot give a strict adjustment. Please adjust with this method in an emergency only.

Play back the COLOR BAR signal on the alignment tape and observe the color spots on the vectorscope screen (WFM OUT/connector panel).
Adjust the size of the every spot on the vectorscope screen to its minimum using ⊘RV13, ⊘RV35 and ⊘RV36 in the same way as method A.

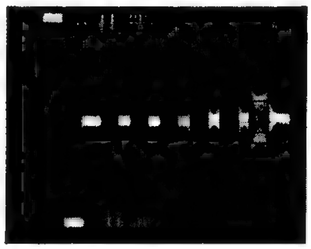
12-17. EQUALIZER PRESET ADJUSTMENT

Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	PLAY
Instrument :	Waveform monitor
VIDEO IN signal :	PAL video signal

(1) Menu/switch settings
Set the menus and switches as follows :

S02. PICTURE MONITOR :	DEMOD
S03. WFM SELECT :	SELECT
PB head ([PLAY/IN] key) :	R/P
REC INHIBIT switch, VIDEO :	ON
REC INHIBIT switch, AUDIO :	ON

(2) Play back the MULTIBURST signal on the alignment tape.
WFM OUT/connector panel



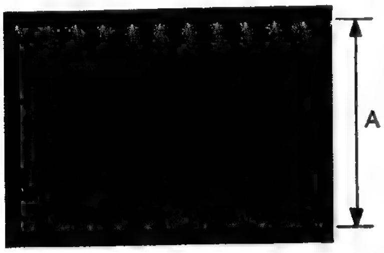
Adjust the EQUALIZER control on the level control panel to its mechanical center point and adjust ⊘RV29/VO-16 so that the waveforms are the same when the control is pulled out (MANUAL) and pushed in (AUTO).

(3) Keep the EQUALIZER control pulled-out.

12-18. ROTARY ERASE CURRENT ADJUSTMENT

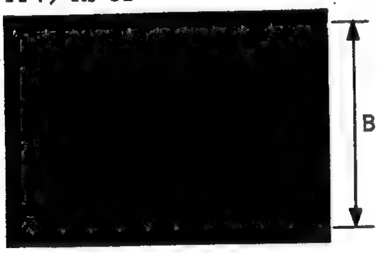
Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL video signal

(1) Remove the tape.
(2) Set the menu and switch as follows :
T16. VIDEO TEST : ON
REC INHIBIT switch, VIDEO : OFF
(3) VIDEO channel adjustment
TP6/RP-32



Period=62.5±2ns (Freq=16±0.5MHz)
⊘LV1/RP-32
A=32±0.5V ⊘RV3/RP-32
Repeatedly adjust the period and amplitude.

(4) SYNC channel adjustment (BVH-3000PS only)
TP7/RP-32



Period=62.5±2ns (Freq=16±0.5MHz)
⊘LV2/RP-32
B=32±0.5MHz ⊘RV4/RP-32
Repeatedly adjust the period and amplitude.

(5) Set test menu [T16. VIDEO TEST] to OFF.

12-19. RECORDING SYSTEM FREQUENCY RESPONSE AND DG/DP ADJUSTMENT

Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	REC (CONFI), PLAY
Instrument :	Vectorscope Waveform monitor
VIDEO IN signal :	PAL RAMP LINEARITY PAL MULTIBURST

(1) Set the menus and switches as follows :
REC INHIBIT switch, VIDEO : OFF
REC INHIBIT switch, AUDIO : OFF
Menu S03. WFM SELECT : SELECT
Menu I17. REC CONFI MODE : CONFI
TAPE/EE ($\boxed{\text{TAPE/IN}}$ key) : TAPE

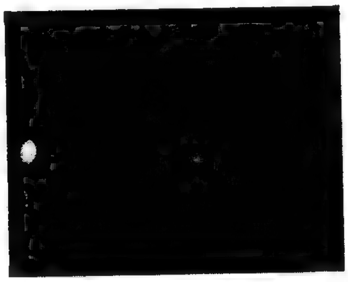
(2) Install a recording tape and adjust in the REC (CONFI) mode. After about 3 minutes have elapsed in the REC mode, start the adjustment.

(3) Set ⊘RV8/VO-16 to its mechanical center point. Supply the RAMP LINEARITY signal to the VIDEO IN connector.

(4) Recording current level adjustment
Set menu [S80. VIDEO METER SELECT] to RF (V). Adjust ⊘RV7/VO-16 so that the VIDEO/RF meter pointer deflects maximum and then turn ⊘RV7 counterclockwise slightly.

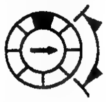
(5) DG/DP adjustment (TBC OUT)
Set menu [S02. PICTURE MONITOR] to TBC OUT.

WFM OUT/connector panel



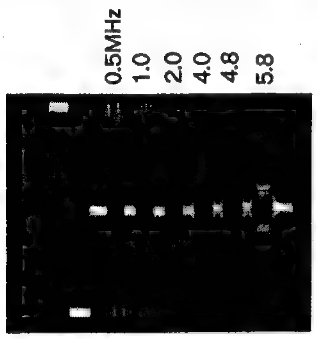
Adjust the size (both gain and phase directions) of the spot on the vectorscope to its minimum using ⊘RV6 and ⊘CT1/VO-16. Then set the vectorscope to the DG mode and DP mode and measure both the differential gain and phase. Repeatedly adjust ⊘RV6 and ⊘CT1 until the measured values come

within the specifications.
DG (TBC OUT) : Less than 4%
DP (TBC OUT) : Less than 4°
Adjust ⊘RV6 within the range in the figure below.



(6) Frequency response adjustment (DEMOD OUT)
Set menu [S02. PICTURE MONITOR] to DEMOD.
Supply the MULTIBURST signal to the VIDEO IN connector.

WFM OUT/connector panel



$$\frac{\text{4.8MHz amplitude}}{\text{0.5MHz amplitude}} = \frac{100^{+3}_{-5}}{100}$$

$$\frac{\text{5.8MHz amplitude}}{\text{0.5MHz amplitude}} \leqq \frac{35}{100}$$

⊘RV8/VO-16

(7) Repeat steps (5) and (6) until the value comes within the specifications.

(8) After the above adjustment, record the RAMP LINEARITY and MULTIBURST signals, measure the differential gain and phase as well as the frequency response when this signal section is played back both by the R/P head and PLAY head, and check that the measured values come within the specifications.

DG (TBC OUT) : Less than 4%
DP (TBC OUT) : Less than 4°
Frequency response (DEMOD) :

$$\frac{\text{4.8MHz amplitude}}{\text{0.5MHz amplitude}} = \frac{100^{+3}_{-5}}{100}$$

$$\frac{\text{5.8MHz amplitude}}{\text{0.5MHz amplitude}} \leqq \frac{35}{100}$$

12-20. RECORDING SYSTEM MOIRE ADJUSTMENT

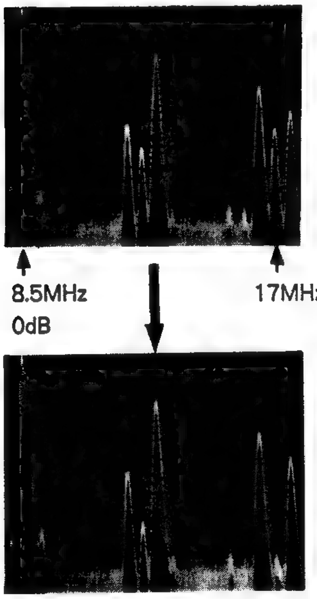
[CAUTION]
There is no need to change the adjustment that was made when the unit was originally shipped from the factory.

Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	REC
Instrument :	Spectrum analyzer
VIDEO IN signal :	Moire signal (see section 12-8)

(1) Set the menus and switches as follows :
REC INHIBIT switch, VIDEO :OFF
REC INHIBIT switch, AUDIO :OFF
TAPE/EE ([TAPE/IN] key) :TAPE

(2) Supply the moire signal to the VIDEO IN connector. Refer to section 12-8. Supply the output signal of the oscilloscope to the spectrum analyzer.

(3) Install a recording tape, set the VTR to the REC mode and adjust as follows.
TP9/VO-16



Adjust and set the spectrum analyzer so that the 8.5MHz level is brought to 0dB, then adjust as follows.
Set the 17MHz level to the minimum.
⊘RV5/VO-16

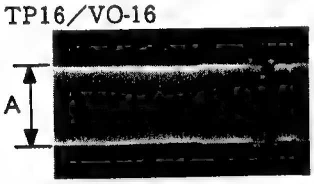
12-21. RF LEVEL/METER ADJUSTMENT

Connection : See section 12-1.
Menu/switch settings : See section 12-1 and text.
Mode of VTR : REC → PLAY
Instrument : Oscilloscope
VIDEO IN signal : PAL 50% FLAT FIELD

(1) Set the REC INHIBIT switches to OFF.

(2) Install a recording tape, record the 50% FLAT FIELD signal and make the adjustments while playing back it.

(3) Set menu [S80. VIDEO METER SELECT] to RF (V), select the R/P head with the PLAY/IN key and adjust as follows.
TP16/VO-16



A=100±10mV ⊘RV19/VO-16

(4) Select the meter display with menu [S80] as shown in the table below, select the playback head using the PLAY/IN key and adjust the meter indication. If the meter indication fluctuates, make the adjustment so that the pointer is positioned in the center of the fluctuation.

	Meter selection Menu S80.	Playback head selection PLAY/IN key	Meter indication adjustment
1.	RF (V)	R/P	100±3% ⊘RV12/VO-16
2.	RF (V)	PLAY	100±3% ⊘RV21/VO-16
3.	RF (S) (Does not apply to BVH-3100PS)	R/P	100+3/−20% ⊘RV20/VO-16
4.	RF (S) (Does not apply to BVH-3100PS)	PLAY	100+3/−20% ⊘RV22/VO-16

(5) Set menu [S80] to RF (V).

12-22. DROPOUT SENSITIVITY ADJUSTMENT

Connection : See section 12-1.
Menu/switch settings : See section 12-1 and text.
Mode of VTR : REC → PLAY, JOG (STILL)
Instrument : Oscilloscope
VIDEO IN signal : PAL COLOR BAR

(1) Set the menus and switches as follows :
REC INHIBIT switch, VIDEO : OFF
REC INHIBIT switch, AUDIO : OFF
Menu S10. PLAY MODE : 1 HD
PB head (PLAY/IN key) : R/P

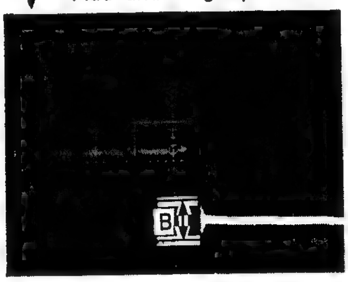
(2) Install a recording tape, record the color bar signal and make the adjustment while playing back it.

(3) Set the oscilloscope to the ADD mode and observe the IC22 pin 4 waveforms and TP25 waveforms. Keep the oscilloscope adjusted so that the amplitude of the IC22 pin 4 waveforms is set to 6 gradations.

Pin 4/IC22/VO-16 TP25/VO-16

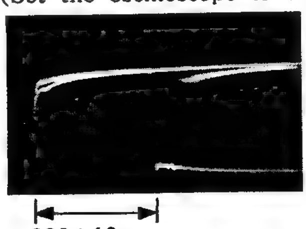
A=6 gradations ⊘Oscilloscope

↓ Add and magnify.



B=1 gradation ⊘RV31/VO-16

(4) Set the VTR to the JOG (STILL) mode.
TP21/VO-16
(Set the oscilloscope to the internal sync mode.)



200±10nsec
⊘RV32/VO-16

12-23. VIDEO OUT DC LEVEL ADJUSTMENT

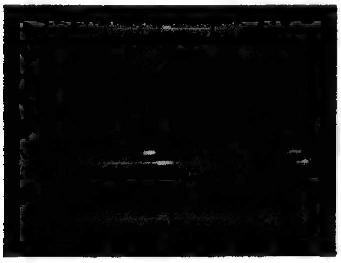
Connection :	See section 12-1.
Menu/switch settings :	See section 12-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Waveform monitor
VIDEO IN signal :	PAL RAMP LINEARITY

(1) Supply the VIDEO-2 OUT signal to the waveform monitor.

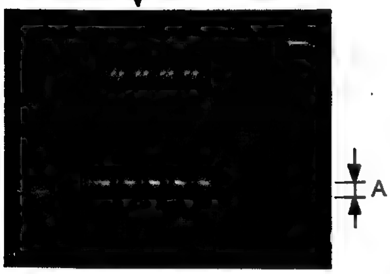
(2) Remove the MA-26 assembly and open the power supply unit. Refer to sections 2-5 and 2-2 (page 2-11).

(3) Set menu [S59. MIXED CHARA OUTPUT] to VD2+TBC.

(4) Adjustment
VIDEO-2 OUT/connector panel



Magnify.



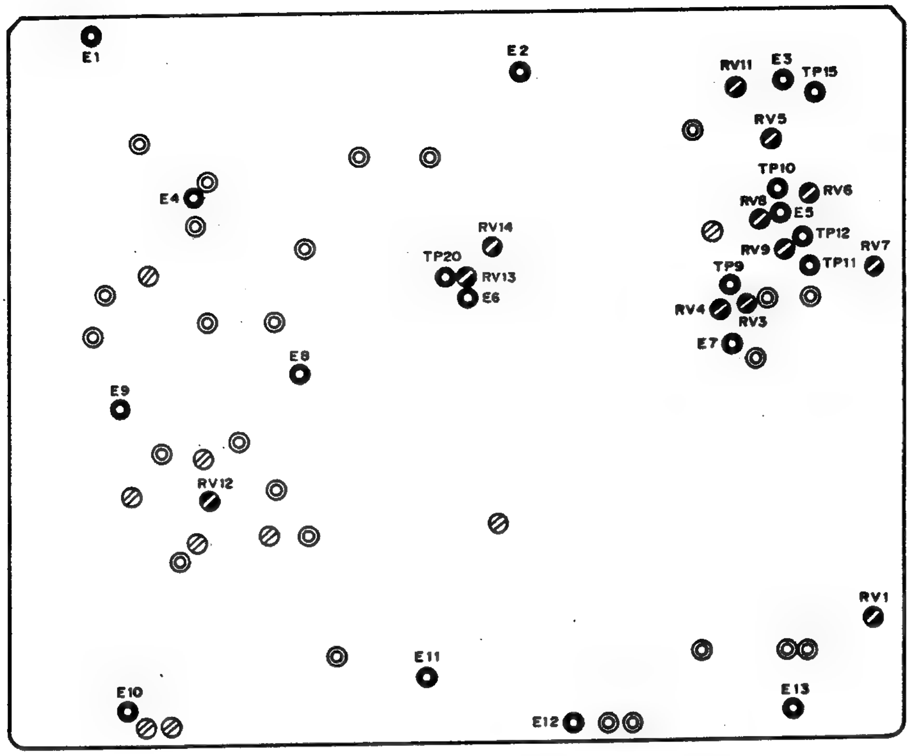
A=0.05±0.01V
RV2/VS-30

(5) Return menu [S59] to DISABLE.

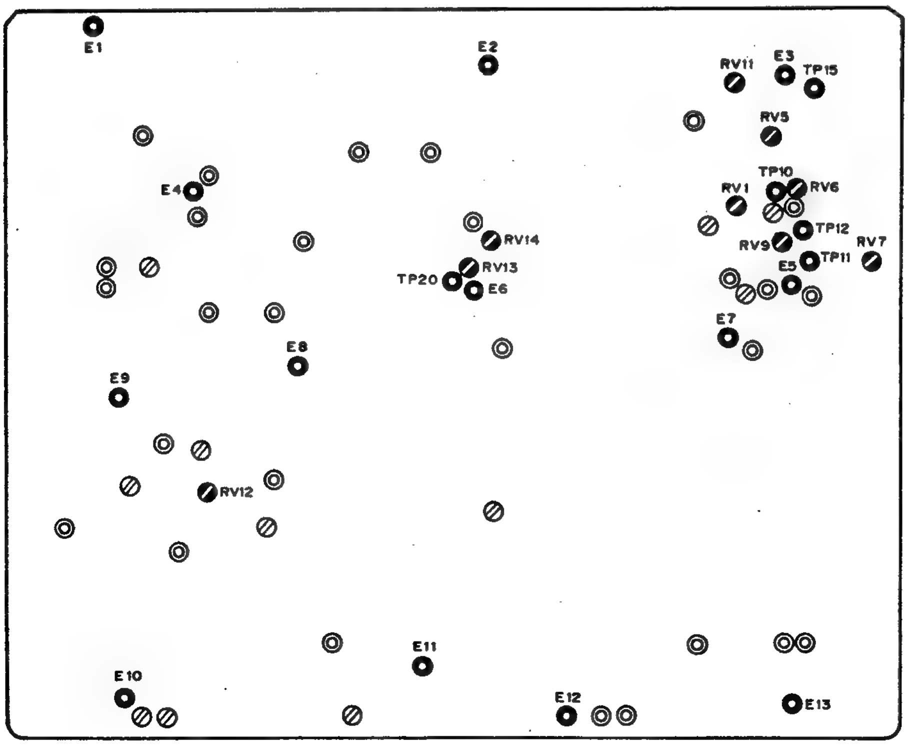
(6) Return the power supply unit and MA-26 assembly to their original positions.

SECTION 13
DT SYSTEM ALIGNMENT

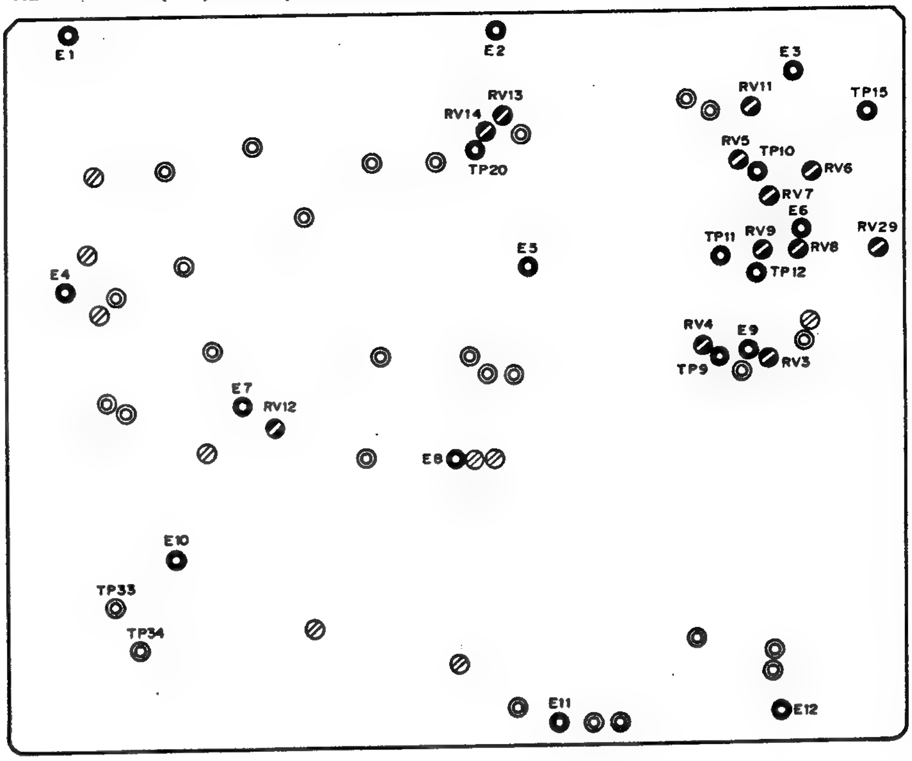
RD-6 Board (-11) Component Side



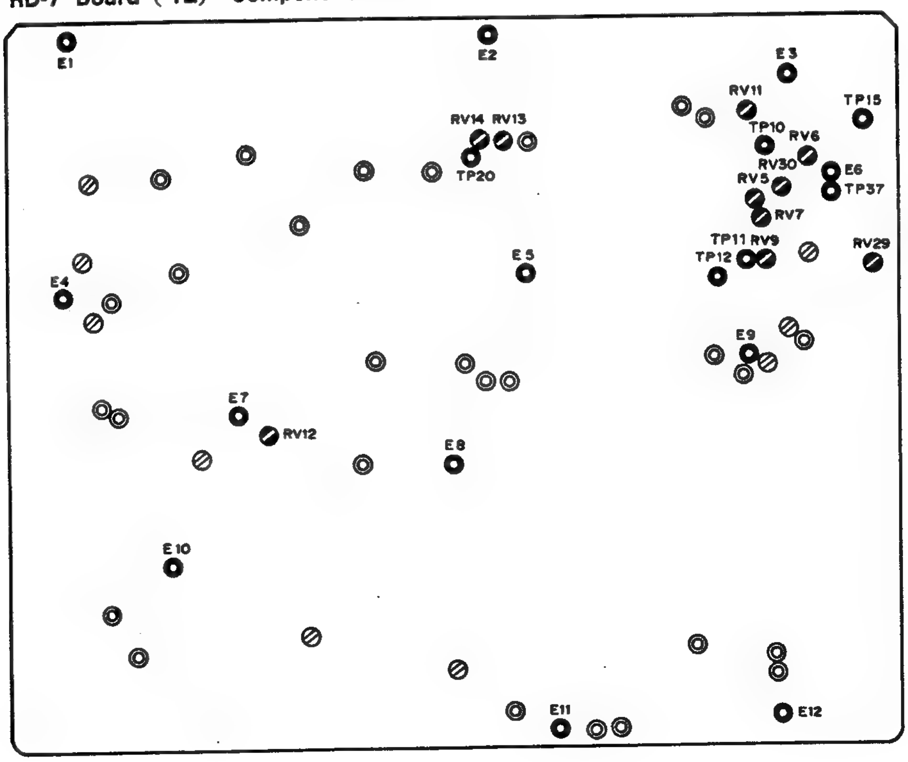
RD-6 Board (-12) Component Side



RD-7 Board (-11) Component Side

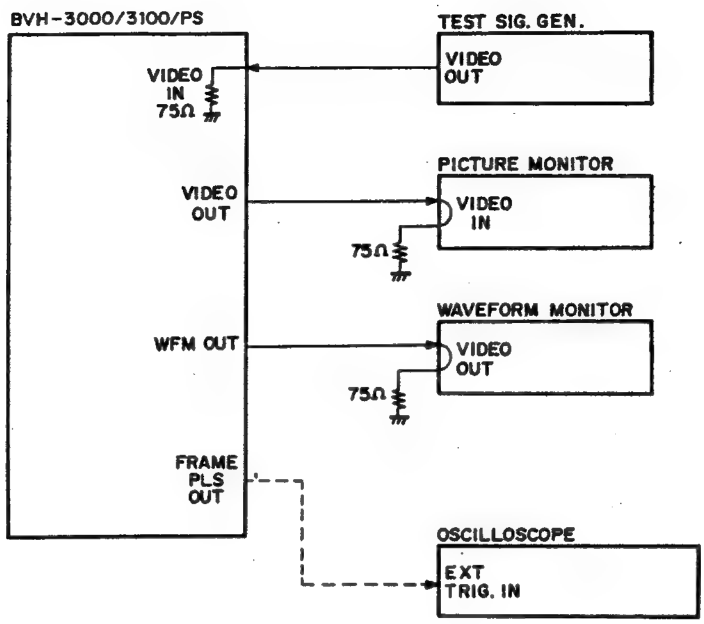


RD-7 Board (-12) Component Side



13-1. ADJUSTMENT PREPARATIONS

Equipment Connection



Menu/Switch Settings

Level control panel	REMOTE/LOCAL :	LOCAL
Function control panel	HEAD SELECT (PLAY/IN key) :	PLAY
	TAPE/EE SELECT (TAPE/IN key) :	TAPE/EE
Menu	S02 PICTURE MONITOR :	TBC OUT
	S03 WFM SELECT :	RF
	S40 SERVO REF SELECT :	INPUT
	S44 DT FIELD/FRAME MODE :	FIELD
	I09 FRAME PULSE OUTPUT :	REF 2

Oscilloscope settings

Trigger :	EXT (from FRAME PLS OUTPUT/connector panel)
TIME/DIV :	2 msec/div
VOLT/DIV :	Suitable setting

13-2. ADJUSTMENT SEQUENCE

Precaution : The DT head control circuit employs a complicated feedback loop, hence unless the entire VTR system is operating normally, the DT system cannot be expected to operate normally. For this reason, before adjusting the DT system, completely perform the various adjustments in the tape path, PG phase, CTL phase, and the video signal system. Do not needlessly turn any of the potentiometers.

For RD-6 (RD-7) board with suffix -11 (Numbers in parenthesis apply to RD-7 board.)

Make a recording for about 3 minutes. Playing back recorded portion, perform the following adjustments.

↓

Adjustments in PLAY mode
- 13-4. RV4 : Wobbling Level Adjustment
- 13-5. RV11 : Strain Gauge Level Adjustment
- 13-6. RV7 : Tracking Error Offset Adjustment
- 13-7. RV5 : RF Envelope Level Adjustment
- 13-8. RV6 : Multiplexer Balance Adjustment

↓

Adjustments in STILL mode
- 13-9. RV8 : Feedback Loop Gain Adjustment
  - RV3 : ΔF Level Adjustment
  - RV1 (RV29) : DT Jump Signal Level Adjustment

↓

Adjustments in VAR+3 and VAR−1 modes
- 13-10. RV3 : ΔF Level Adjustment
  - RV9 : Feedback Loop Balance Adjustment
  - RV8 : Feedback Loop Gain Adjustment

↓

Adjustment in STILL mode
- 13-11. RV1 (RV29) : DT Jump Signal Level Adjustment

↓

Adjustments in VAR−1 to VAR+3 modes
- 13-12. Auto Jump Adjustment

↓

VAR−1 to +3 and JOG modes
- 13-13. Confirmation after Adjustment

For RD-6 (RD-7) board with suffix -12 or higher (Numbers in parenthesis apply to RD-7 board.)

Adjustments in STOP/EE mode
- 13-3. RV2 (RV30) : A/D Reference Voltage Adjustments

↓

Make a recording for about 3 minutes. Playing back the recorded portion, perform the following adjustments.

↓

Adjustments in PLAY mode
- 13-5. RV11 : Strain Gauge Level Adjustment
- 13-6. RV7 : Tracking Error Offset Adjustment
- 13-7. RV5 : RF Envelope Level Adjustment
- 13-8. RV6 : Multiplexer Balance Adjustment

↓

Adjustments in STILL mode
- 13-9. RV1 (RV29) : DT Jump Signal Level Adjustment

↓

Adjustment in VAR+3 mode
- 13-10. RV9 : Feedback Loop Balance Adjustment

↓

Adjustments in VAR−1 to VAR+3 modes
- 13-12. Auto Jump Adjustment

↓

VAR−1 to +3 and JOG modes
- 13-13. Confirmation after Adjustment

13-3. A/D REFERENCE VOLTAGE ADJUSTMENTS (RD-6/RD-7 Board with Suffix -12)

Connection: See section 13-1.
Menu/Switch settings:
See section 13-1.
Mode of VTR: STOP/EE

Adjustment

TP36/RD-6 (-12): +5.00±0.02Vdc
⊘RV2/RD-6 (-12)
TP37/RD-7 (-12): +5.00±0.02Vdc
⊘RV30/RD-7 (-12)

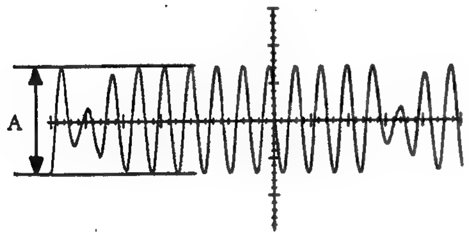
13-4. WOBBLING LEVEL ADJUSTMENT (RD-6/RD-7 Board with Suffix -11)

Connection: Same as previous section
Menu/Switch settings:
Same as previous section
Mode of VTR: RECORD → PLAY

(1) Record a colored signal such as a color bar signal for about 3 minutes. While playing back this self-recorded portion, perform the following adjustment.

(2) Adjustment

TP9/RD-6 (RD-7) (-11)



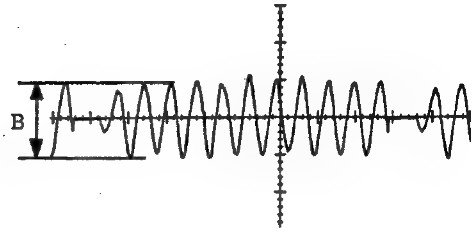
A=300±10mV
⊘RV4/RD-6 (RD-7) (-11)

13-5. STRAIN GAUGE LEVEL ADJUSTMENT

Connection: Same as previous section
Menu/Switch settings:
Same as previous section
Mode of VTR: PLAY
See section 13-4 (1).

Adjustment

TP15/RD-6 (RD-7)



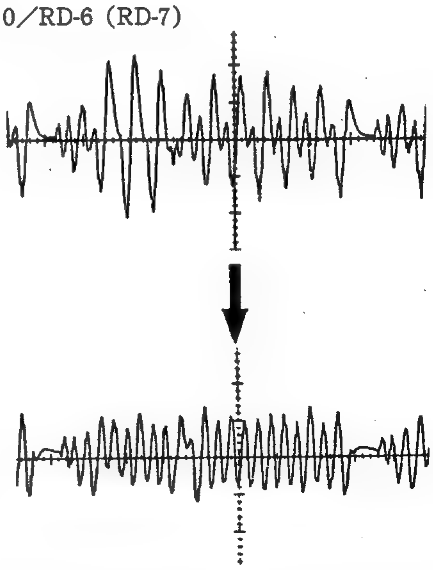
B=200±10mV
⊘RV11/RD-6 (RD-7)

13-6. TRACKING ERROR OFFSET ADJUSTMENT

Connection: Same as previous section
Menu/Switch settings:
Same as previous section
Mode of VTR: Same as previous section
See section 13-4 (1).

Adjustment

TP10/RD-6 (RD-7)



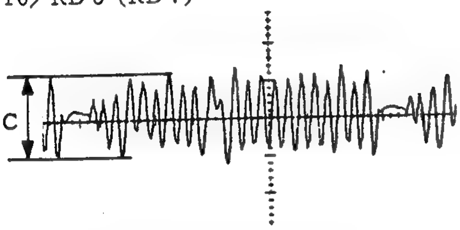
Perform adjustment so that the waveform has good vertical symmetry.
⊘RV7/RD-6 (RD-7)

13-7. RF ENVELOPE LEVEL ADJUSTMENT

Connection : Same as previous section
Menu/Switch settings :
Same as previous section
Mode of VTR : Same as previous section
See section 13-4 (1).

Adjustment

TP10/RD-6 (RD-7)



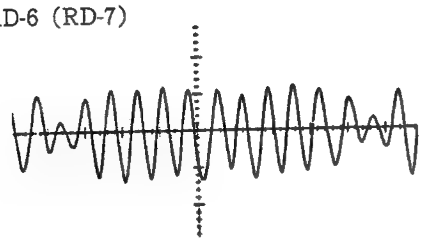
C=200±10mV
⊘RV5/RD-6 (RD-7)

13-8. MULTIPLEXER BALANCE ADJUSTMENT

Connection : Same as previous section
Menu/Switch settings :
Same as previous section
Mode of VTR : Same as previous section
See section 13-4 (1).

Adjustment

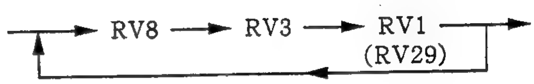
TP11/RD-6 (RD-7)



Perform adjustment so that waveform has minimum amplitude.
⊘RV6/RD-6 (RD-7)

13-9. DT JUMP ADJUSTMENT-1

[Note 1] **For RD-6 (RD-7) board with suffix -11**
(Numbers in parenthesis apply to RD-7 board.)
* Adjust RV8, RV3, and RV1 (RV29) in that sequence, then repeat the adjustments so that each specification is more or less satisfied.



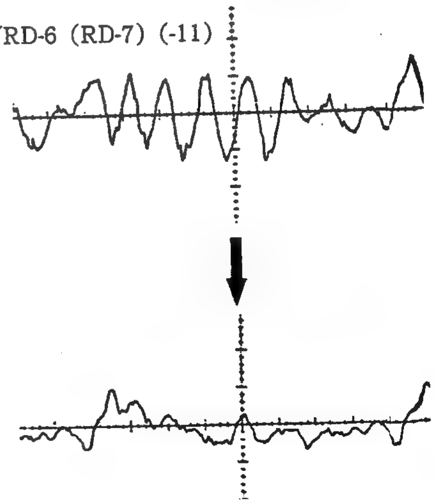
* Readjust RV8 and RV3 according to section 13-10. Perform final adjustment of RV1 (RV29) using section 13-11.
* Before adjusting RV1 (RV29), set test menu T10. AUTO JUMP to OFF.

[Note 2] **For RD-6 (RD-7) board with suffix -12 or higher**
* Adjust RV1 (RV29) only. RV8 and RV3 are exclusively for RD-6 (RD-7) board with suffix -11.
* Before performing adjustment, set test menu T10. AUTO JUMP to OFF.

Connection : Same as previous section
Menu/Switch settings :
Same as previous section
Mode of VTR : STILL
See section 13-4 (1).

(1) RV8 : Feedback loop gain adjustment
(RD-6/RD-7 board with suffix -11)

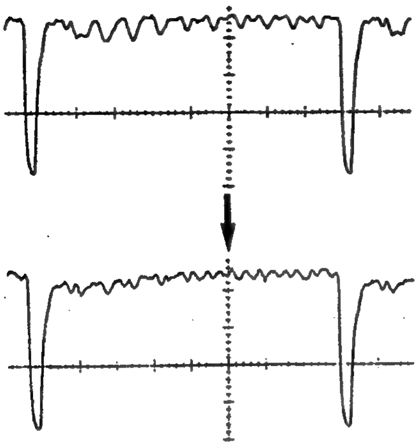
TP12/RD-6 (RD-7) (-11)



Turn ⊘RV8/RD-6 (RD-7) (-11) to a point just before the waveform starts to become disarranged.

(**2**) RV3 : ΔF level adjustment
(RD-6/RD-7 board with suffix -11)

CN-B7c/RD-6
(RD-7) (-11)
(RF envelope)

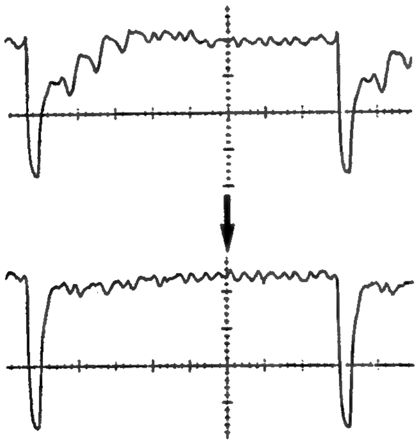


Make the overlap wave of the RF envelope symmetrical in the vertical direction.
➋RV3/RD-6 (RD-7) (-11)

(**3**) RV1 (RV29) : DT jump signal level adjustment

Set test menu T10. AUTO JUMP to OFF.

CN-B7c/RD-6
(RD-7)
(RF envelope)



Perform adjustment so that the level of the beginning of the RF envelope is maximum.
➋RV1/RD-6
➋RV29/RD-7

Return test menu T10. AUTO JUMP to ON.

(**4**) For RD-6 (RD-7) board with suffix -11, repeat adjustments (1), (2), and (3) so that the specifications of (1), (2), and (3) are more or less satisfied.
For RD-6 (RD-7) board with suffix -12 or higher, proceed to section 13-10.

13-10. FEEDBACK LOOP ADJUSTMENT

[Note 1] **For RD-6 (RD-7) board with suffix -11**
*Perform adjustment in the sequence RV3, RV9, and RV8, then repeat the adjustments until each specification is more or less satisfied.

→ RV3 → RV9 → RV8 →

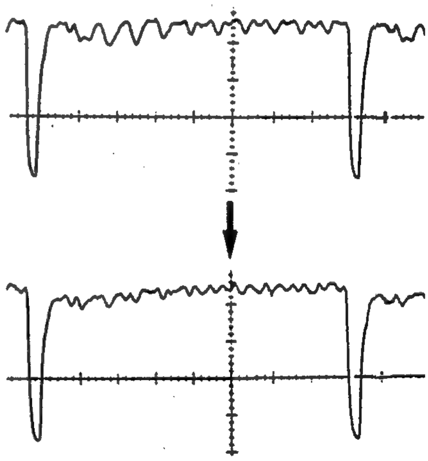
*Perform adjustment in each of the VAR+3 and VAR−1 modes.

[Note 2] **For RD-6 (RD-7) board with suffix -12 or higher**
*Adjust RV9 only. RV3 and RV8 are exclusively for RD-6 (RD-7) board with suffix -11.
*Perform adjustment in the VAR+3 mode.

Connection : Same as previous section
Menu/Switch settings :
Same as previous section
Mode of VTR : VAR+3 and −1
See section 13-4 (1).

(**1**) RV3 : ΔF level adjustment
(RD-6/RD-7 board with suffix -11)

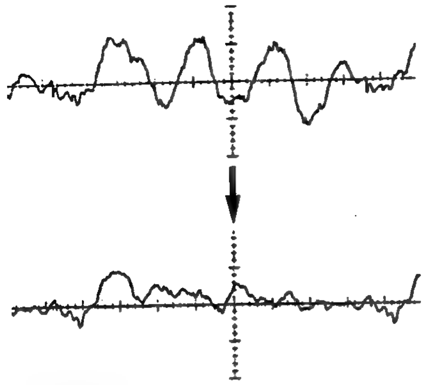
CN-B7c/RD-6
(RD-7) (-11)
(RF envelope)



Perform adjustment so that the overlap wave of the RF envelope is symmetrical in the vertical direction, for each of the VAR+3 and VAR−1 modes.
➋RV3/RD-6 (RD-7) (-11)

(2) RV9 : Feeback loop balance adjustment
(RD-6 board with suffix -11/-12)

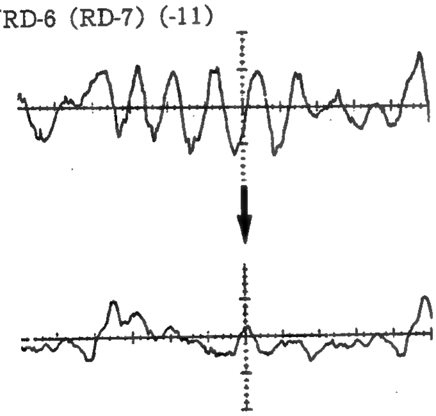
TP12/RD-6 (RD-7)



Set the amplitude to minimum.
⊘RV9/RD-6 (RD-7)
For RD-6 (RD-7) board with suffix -11, perform adjustment in each of the VAR+3 and−1 modes.
Adjustment can be made easier by turning ⊘RV8 slightly to the right (to the left in the case of RD-7 board) so as to slightly disarrange the waveform of TP12.
For RD-6 (RD-7) board with suffix -12 or higher, perform adjustment in the VAR+3 mode, then proceed to section 13-12.

(3) RV8 : Feedback loop adjustment
(RD-6/RD-7 board with suffix -11)

TP12/RD-6 (RD-7) (-11)



Turn ⊘RV8/RD-6 (RD-7) (-11) until just before the waveform starts to become disarranged.
Perform adjustment in each of the VAR+3 and −1 modes.

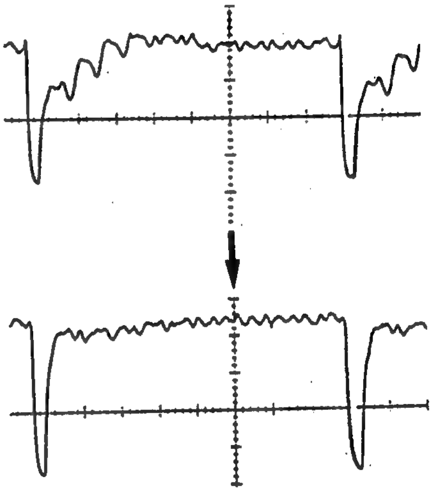
(4) For RD-6 (RD-7) board with suffix -11, repeat adjustments (1), (2), and (3) until specifications (1), (2), and (3) are more or less satisfied.
For RD-6 (RD-7) board with suffix -12 or higher, perform adjustment (2) alone, then proceed to section 13-12.

13-11. DT JUMP ADJUSTMENT-2 (RD-6/RD-7 board with suffix -11)

Connection : Same as previous section
Menu/Switch settings :
Test menu T10. AUTO JUMP OFF
Other settings same as previous section
Mode of VTR : STILL
See section 13-4 (1).

Set test menu T10. AUTO JUMP to OFF.

CN-B7c/RD-6
(RD-7) (-11)
(RF envelope)



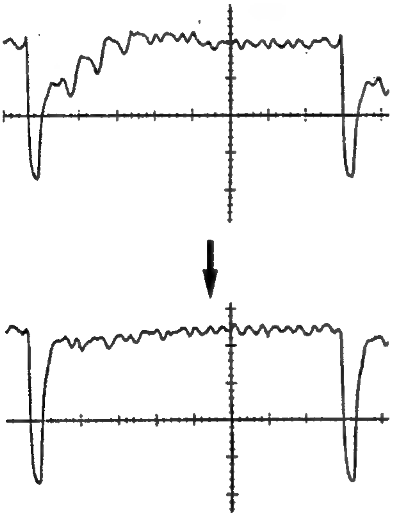
Using ⊘RV1/RD-6 (⊘RV29/RD-7), adjust the level of the beginning of the RF envelope to maximum.

Return test menu T10. AUTO JUMP to ON.

13-12. AUTO JUMP ADJUSTMENT

Connection : Same as previous section
Menu/Switch settings :
See section 13-1
Mode of VTR : VAR −1, 0, +1, +2, and +3
See section 13-4 (1).

(1) Run the tape in the VAR−1 mode until the beginning of the RF envelope becomes maximum. After running the tape for a while, adjustment will take place automatically.



(2) Perform the same adjustment as (1) in each of the VAR 0, +1, +2, and +3 modes.

13-13. CONFIRMATION AFTER ADJUSTMENT

Confirm that the monitor picture is not disturbed and also that there are no black or white horizontal streaks on the top of the monitor screen when playback is performed at VAR −1 to +3 in the JOG mode.

Caution : If the search dial to rotated abruptly in the reverse direction in the JOG mode, the screen may become disturbed. This is because the tape speed will be at least −×1 and the DT follow range will be exceeded.

13-14. REF SC-H ADJUSTMENT

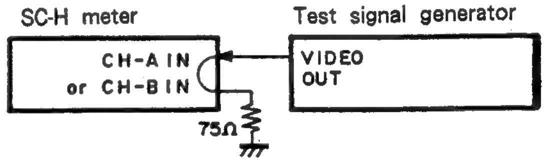
[Caution 1]
Do not perform adjustment if the software in the SV, SY, and RD boards is version 1. Before performing adjustment, confirm that the software is version 2 or higher. The version No. is indicated on the label of the IC as shown below.

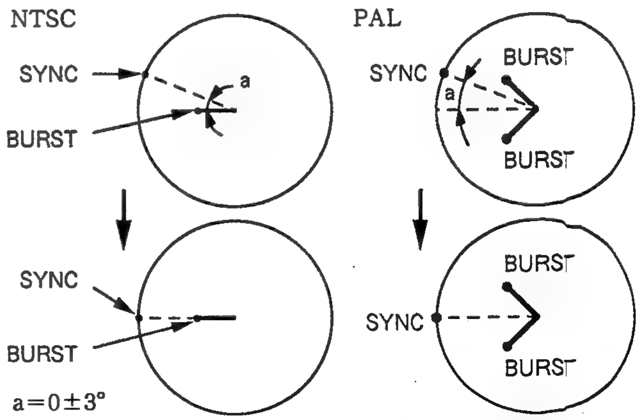
Board	Ref. No.	Version 1	Version 2
SV-90	ICN5	V0U1-*-*	V0U2-*-*
	ICN3	V1U1-*-*	V1U2-*-*
	ICE15	V2U1-*-*	V2U2-*-*
SY-103	ICH12 (NTSC)	Y0U1-*-*	Y0U2-*-*
	(PS)	Y0A1-*-*	Y0A2-*-*
	ICH11 (NTSC)	Y1U1-*-*	Y1U2-*-*
	(PS)	Y1A1-*-*	Y1A2-*-*
RD-6	ICL15 (NTSC)	RDU1-*-*	RDU2-*-*
RD-7	ICM14 (PS)	RDP1-*-*	RDU2-*-*

[Caution 2]
An SC-H meter is necessary for adjustment.
TEKTRONIX 1750 SC-H PHASE MONITOR (NTSC)
TEKTRONIX 1751 SC-H PHASE MONITOR (PAL)
Do not perform adjustment if an SC-H meter is not available.

Connection : See section 13-1 and text.
Menu/switch settings : See section 13-1 and text.
Mode of VTR : STOP

(1) SC-H phase adjustment of test signal
Adjust the signal generator connected as shown below.

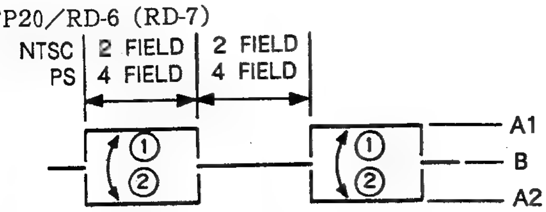




a=0±3°
⊘ HORIZ DELAY control/test signal generator

Disconnect the connector which was connected to the SC-H meter, connect it to the VIDEO IN connector of the VTR, then perform the following adjustments.

(2) Temporary adjustments
TP20/RD-6 (RD-7)

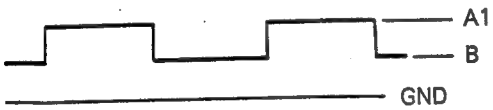


A1=Approx. +5Vdc
B =Approx. +2.5Vdc
A2=Approx. 0Vdc
⊘RV13 ⊘RV14/RD-6 (RD-7)
By rotating RV12/RD-6 (RD-7), the waveform between ① and ② will be reversed. Adjust the DC voltages at A1, B, and A2 while rotating ⊘RV12 to invert the waveform.
Adjust the amplitude using ⊘RV13 and adjust the DC offset using ⊘RV14.

(3) Temporary adjustment of burst shift
TP20/RD-6 (RD-7)

A1=Approx. +5Vdc
B =Approx. +2.5Vdc
Slowly rotate ⊘RV12/RD-6 (RD-7) until the waveform moves from ② to ①. Next, turn ⊘RV12 clockwise from that point by exactly one graduation.

(4) Temporary adjustment of REF SC-H offset
TP20/RD-6 (RD-7)



B=Approx. +1.5Vdc
(A=Approx. +4Vdc)
⊘RV14/RD-6 (RD-7)

(5) REF SC-H gain adjustment
Select [TIP ADJ] of the test menu [T17. MAINTENANCE]. See section 3-3.
Key in $\boxed{C}$, $\boxed{6}$, $\boxed{8}$, then press the $\boxed{SET}$ key. [C68. REF SCH GAIN] will be selected, and the following will be displayed on the control panel.

>C68	> REF SCH GAIN
00**	>_

Adjust ⊘RV13/RD-6 (RD-7) so that the [**] portion of the display becomes one of 7F, 80, and 81.
After adjustment, press the blue $\boxed{IN}$ key while pressing the blue $\boxed{OUT}$ key.

(6) Burst shift adjustment
TP20/RD-6 (RD-7)

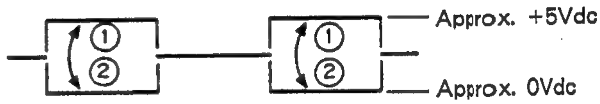
A1=Approx. +5Vdc
B =Approx. +2.5Vdc
A2=Approx. 0Vdc
Slowly rotate ⊘RV12/RD-6 (RD-7) until the waveform moves from ① to ②. Next, turn ⊘RV12 counterclockwise from that point by exactly one graduation.

(7) REF SC-H offset adjustment
Key in $\boxed{C}$, $\boxed{6}$, $\boxed{9}$, and press the $\boxed{SET}$ key. [C69. REF SCH DATA] will be selected, and the following will appear on the control panel.

>C69	> REF SCH DATA
00**	>_

Adjust ⊘RV14/RD-6 (RD-7) so that the [**] portion of the display becomes one of 7F, 80, and 81.
After adjustment, press the blue $\boxed{IN}$ key while pressing the blue $\boxed{OUT}$ key, then press the $\boxed{SET}$ key while pressing the $\boxed{OUT}$ key.

(8) Confirmation after adjustment
TP20/RD-6 (RD-7)



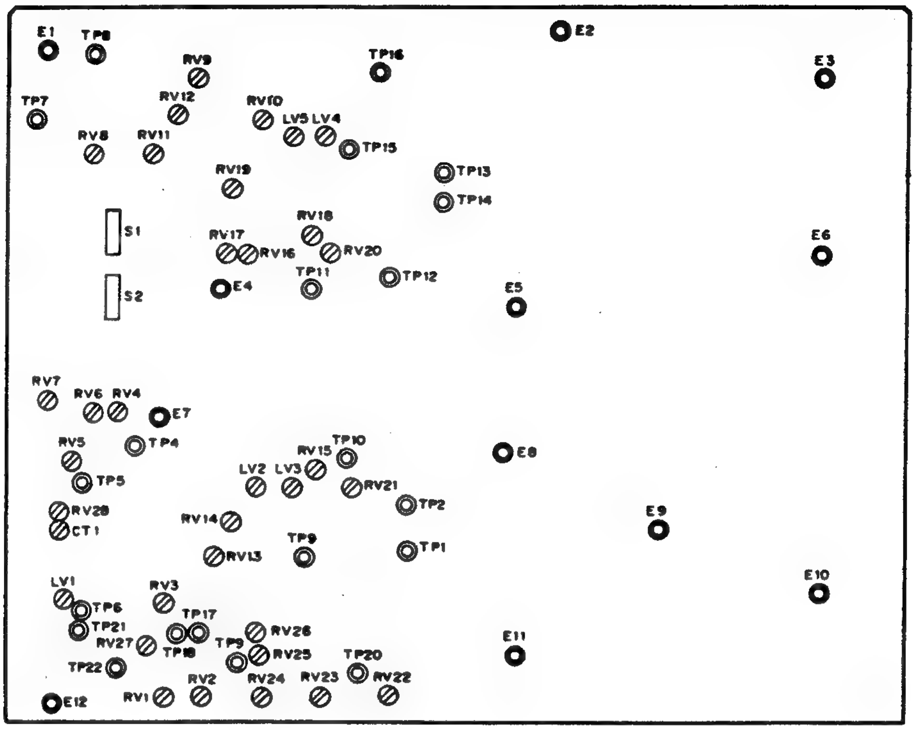
Confirm that the waveform at TP20 is inverted between approx. +5Vdc and approx. 0Vdc when the HORIZ DELAY control on the test signal generator is turned left and right.
If the waveform is inverted between +2.5Vdc and +7.5Vdc, or between −2.5Vdc and +2.5Vdc, adjust ⊘RV14/RD-6 (RD-7) so that it is inverted between approx. 0Vdc and approx. +5Vdc, then return to the burst shift adjustment of step (3), and re-perform the subsequent adjustments.

Next, confirm that the REF SCH LEDs on the level control panel all light in stages when the HORIZ DELAY control of the test signal generator is turned left and right.

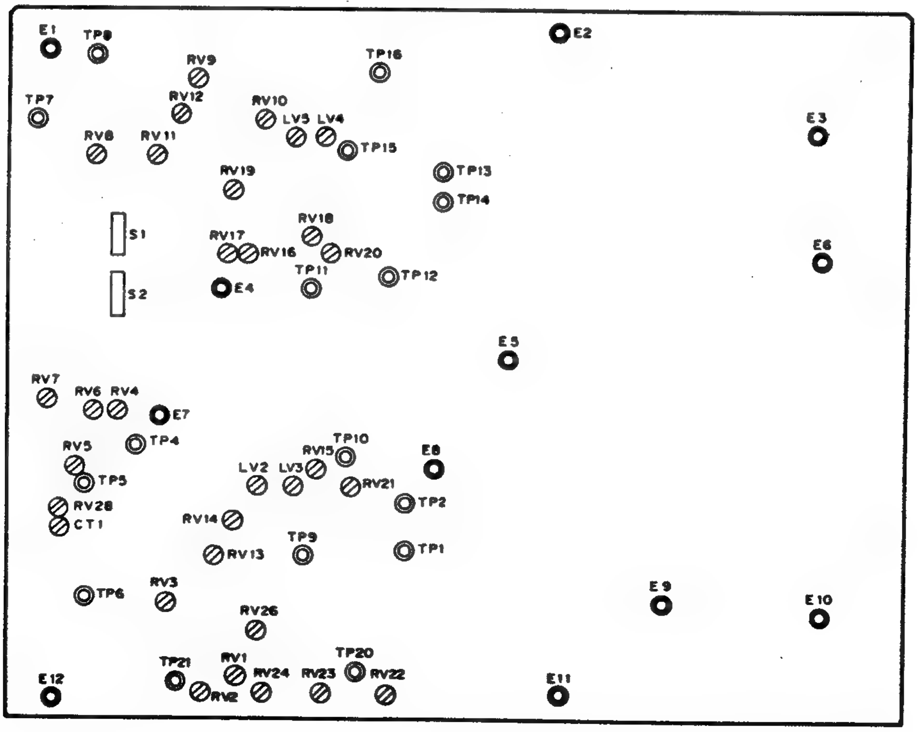
After confirmation, return the SC-H phase of the test signal generator to the intial setting. See step (1).

SECTION 14
TBC SYSTEM ALIGNMENT

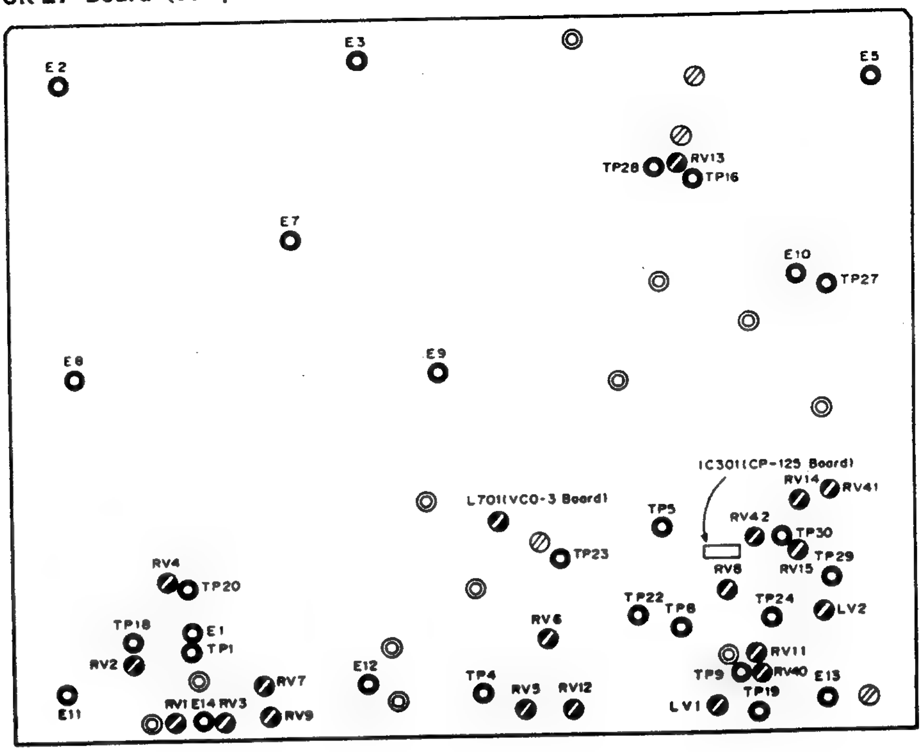
PR-92 Board (component side) /BKH-3020



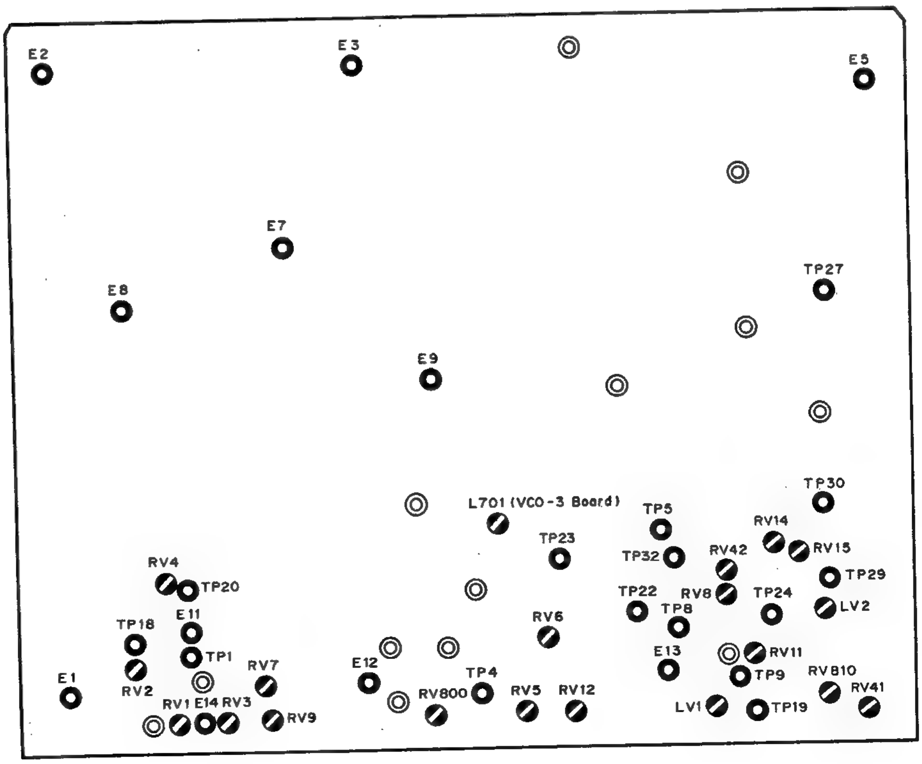
PR-98 Board (component side) /BKH-3060



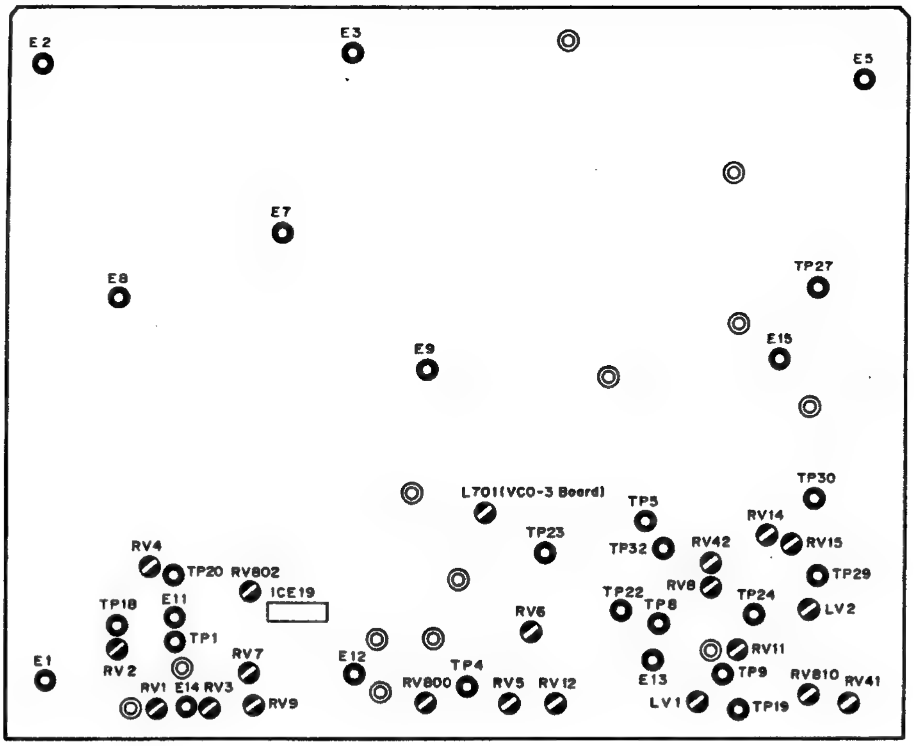
CK-27 Board (component side) -11, -12



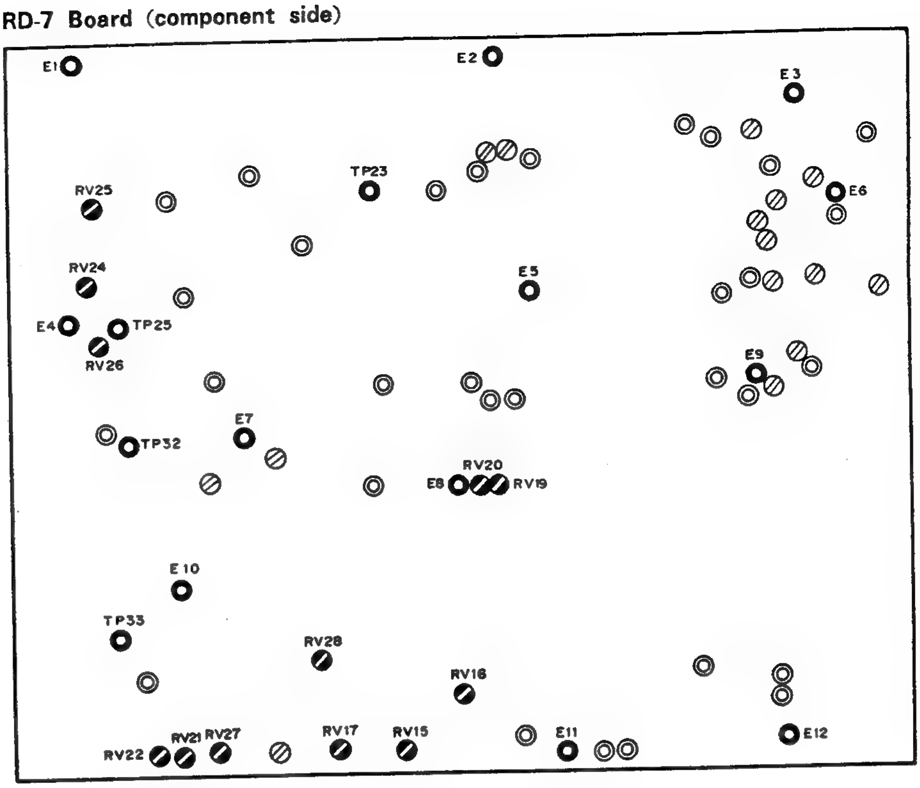
CK-27 Board (component side) -13



CK-27 Board (component side) -14

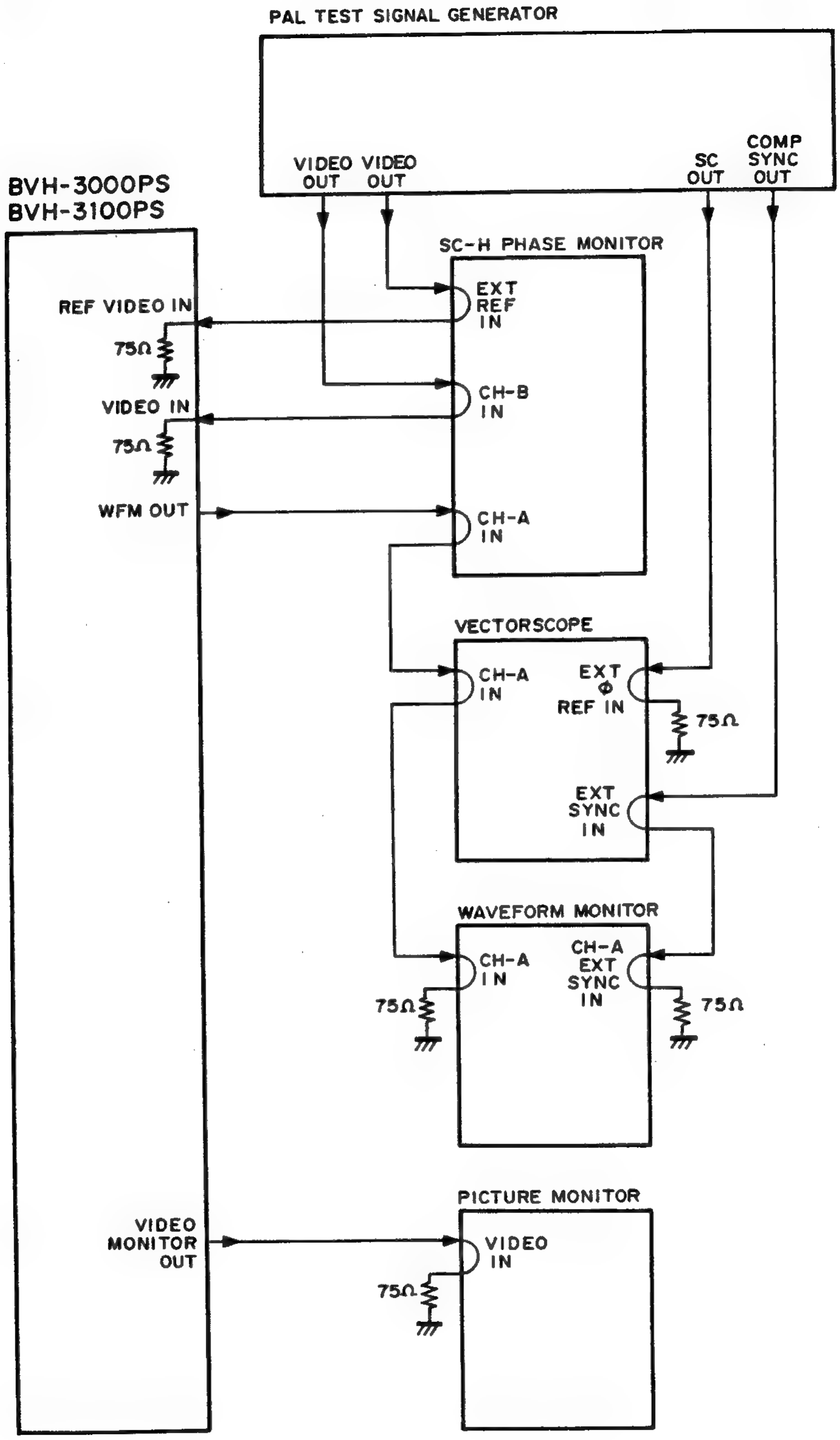


RD-7 Board (component side)



14-1. ADJUSTMENT PREPARATIONS

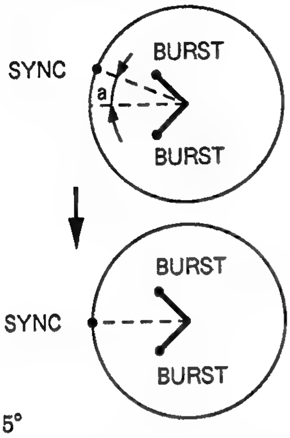
(1) Equipment connection



(2) SC-H phase adjustment of test signal

Adjust the signal generator so that the SC-H phase of the input signal to the VTR is 0±5°.

CH-B/SC-H PHASE monitor



a=0±5°

● HORIZ DELAY control/test signal generator

(3) Menu/switch settings

Level control panel

- VIDEO level control: preset
- TRACKING control: preset
- EQUALIZER control: AUTO
- REMOTE/LOCAL switch: LOCAL

Function control panel

- TAPE/IN key: TAPE/EE
- PLAY/IN key: R/P head

Menu

1. Using the following key operations, load the default menu selection data in the PROM (data in unit at shipment) to the RAM.
   [SETUP] → [T] → [0] → [SET]
2. Also, perform the following settings.
   - Menu S02. PICTURE MONITOR: TBC OUT
   - Menu S03. WFM SELECT: SELECT
   - Menu S40. SERVO REF SELECT: INPUT
   - Menu S41. CAPSTAN LOCK MODE: 4F
3. Also, set menu S89 to PAL or SECAM according as the signal to be recorded or played back.
   Menu S89. TV STANDARD: PAL or SECAM

(4) Setting the remote control unit

When using a TBC remote control unit such as the BK-2007, set the switches and controls as shown below.

- Each PRESET/MANUAL switch: PRESET
- SYSTEM SYNC PHASE control: Mechanical center
- SYSTEM SC PHASE control: Mechanical center

14-2. ADJUSTMENT SEQUENCE

14-3 to 14-6
PR-92/PR-98 board adjustment (1)
(NORMAL)

↓

14-7 to 14-20
CK-27 board adjustment

↓

14-21 to 14-25
RD-7 board adjustment

↓

14-26 to 14-33
PR-92/PR-98 board adjustment (2)
(DT, BIDIREX, SECAM ID)

↓

14-34 to 14-37
Overall adjustment

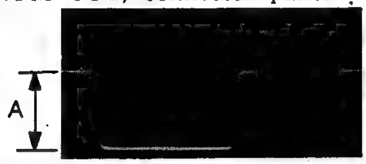
↓

14-38
Y/C delay adjustment

14-3. SYNC SIGNAL ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Waveform monitor
VIDEO IN signal :	PAL or SECAM video signal

WFM OUT/connector panel

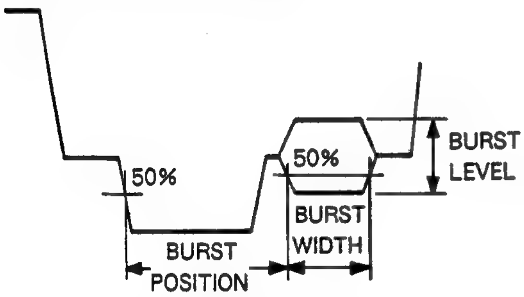


A=300±6mV
⊘RV12/PR-92, PR-98

14-4. PAL BURST SIGNAL ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Waveform monitor
VIDEO IN signal :	PAL video signal

WFM OUT/connector panel



BURST LEVEL=300±6mV ⊘RV11/PR-92, PR-98
BURST POSITION=5.6±0.1 μs ⊘RV9/PR-92, PR-98
BURST WIDTH=2.25±0.23 μs ⊘RV10/PR-92, PR-98

14-5. BLACK LEVEL, VIDEO LEVEL, AND DARK CLIP LEVEL ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Waveform monitor
VIDEO IN signal :	PAL or SECAM video signal

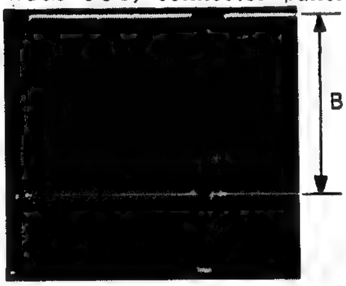
(1) Set test menu [T06] to ON. See section 3-2.
T06. PR TEST 2 : ON

(2) Set test menu [T05] to 0, 100, −10 IRE, and adjust the level as shown below.

(3) Black level preset adjustment
T05. PR TEST 1 : 0 IRE
WFM OUT/connector panel

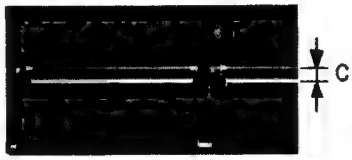
A=0±10mV
⊘RV3/PR-92, PR-98

(4) Video level preset adjustment
T05. PR TEST 1 : 100 IRE
WFM OUT/connector panel



B=700±7mV
⊘RV5/PR-92, PR-98

(5) Dark clip level adjustment
T05. PR TEST 1 : −10 IRE
WFM OUT/connector panel



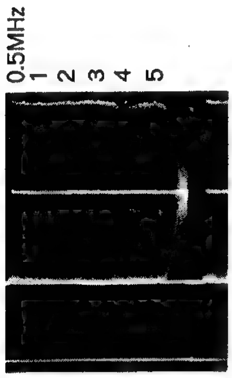
C=50±5mV
⊘RV8/PR-92, PR-98

(6) Return the menus to their initial settings.
T05. PR TEST 1 : OFF
T06. PR TEST 2 : OFF

14-6. TBC OUT FREQ. RESPONSE ADJUSTMENT

Connection : See section 14-1.
Menu/switch settings : See section 14-1.
Mode of VTR : STOP (EE)
Instrument : Waveform monitor
VIDEO IN signal : PAL SWEEP (FIELD RATE)

Taking the amplitude at 0.5MHz as a reference, adjust the amplitude at other frequencies.
WFM OUT/connector panel



$$\frac{\text{Amplitude at each frequency}}{\text{Amplitude at 0.5MHz}} = \frac{100\pm3}{100}$$

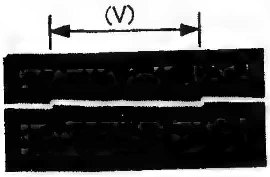
Perform adjustment in the following sequence.
(PR-92/PR-98 board)

1. ⊘RV6 : Turn fully clockwise.
   RV6 will be adjusted at step 4.
2. ⊘CT1 : 4MHz
   Final adjustment will be performed at step 5.
3. ⊘RV7 : 2MHz
4. ⊘RV6 : 0.5MHz to 5MHz : Linear
5. ⊘CT1 : 0.5MHz to 5MHz : Flat

14-7. PAL SYNC SLICE LEVEL ADJUSTMENT

Connection : See section 14-1.
Menu/switch settings : See section 14-1.
Mode of VTR : STOP (EE)
Instrument : Oscilloscope
VIDEO IN signal : PAL video signal

TP9/CK-27

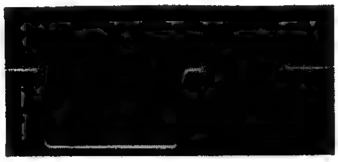


Average DC level = +3.7±0.1Vdc
⊘RV40/CK-27 (board suffix # : -11, -12)
⊘RV810/CK-27 (board suffix # : -13, -14)
Note : RV40, RV810 must be finally adjusted at section 14-15 PAL normal write zero adjustment.

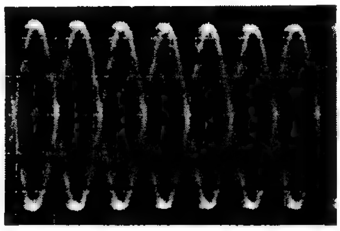
14-8. TAPE PAL H ADJUSTMENT

Connection : See section 14-1.
Menu/switch settings : See section 14-1.
Mode of VTR : STOP (EE)
Instrument : Oscilloscope
VIDEO IN signal : PAL video signal

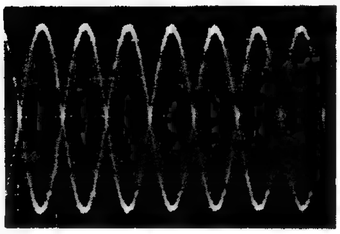
TP1/CK-27
(Trig : from TP22/CK-27, +slope)



Magnify a burst.



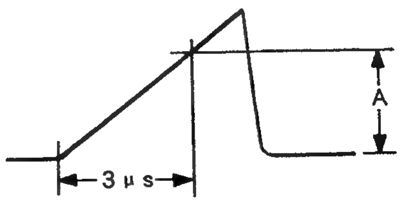
Minimize jitter.
⊘RV11/CK-27



14-9. SYNC GATE ADJUSTMENT

Connection : See section 14-1.
Menu/switch settings : See section 14-1.
Mode of VTR : STOP (EE)
Instrument : Oscilloscope
VIDEO IN signal : PAL or SECAM video signal

TP8/CK-27

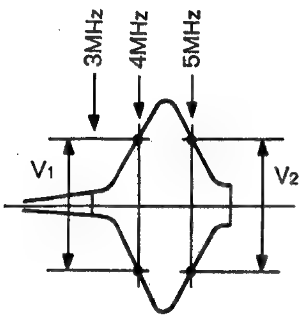


A = 3.0±0.1V
⊘RV8/CK-27

14-10. PAL BURST TUNING ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope (Trig. from VD/TEST SG)
VIDEO IN signal :	PAL SWEEP (FIELD RATE)

TP19/CK-27

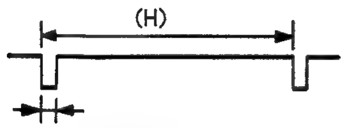


V1=V2
⊘LV1/CK-27

14-11. START PULSE ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL or SECAM video signal

TP4/CK-27



2.7±0.01 μs
⊘RV6/CK-27

14-12. AFC ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL or SECAM video signal

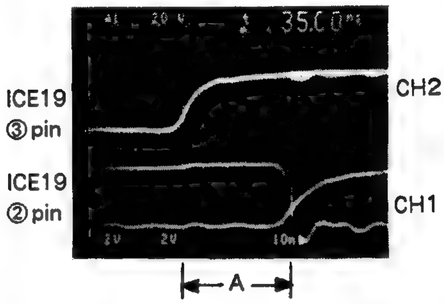
TP24/CK-27 : +1.8±0.1Vdc
⊘LV2/CK-27

14-13. PAL VCO & O/E DET ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL video signal

1. PAL VCO ADJUSTMENT
TP23/CK-27 : +4.25±0.1Vdc
⊘L701/CK-27
(Note) L701 may be installed on the VCO-3 piggy back board on the CK-27 board.

2. PAL O/E DET DELAY ADJUSTMENT
① CONNECT TWO PROBES TO TWO PINS OF IC.
CH-1 ······· PIN② (ICE19) /CK-27
CH-2 ······· PIN③ (ICE19) /CK-27 (TRIG : CH2)
② Adjust ⊘RV801 so that the following time width "A" is 35 μs.

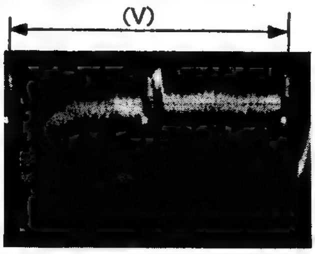


③ After adjusted, when playback tape (color bars) 2 times or 3 times repeatlly at VAL 3 speeds to −1 speed of DT mode, confirm that is not appeared the opposite phase color picture.

14-14. PAL VELOCITY ERROR OFFSET ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL video signal

CN A-14b/CK-27

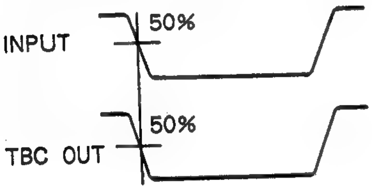


Average level=0±0.1Vdc
⊘RV7/CK-27

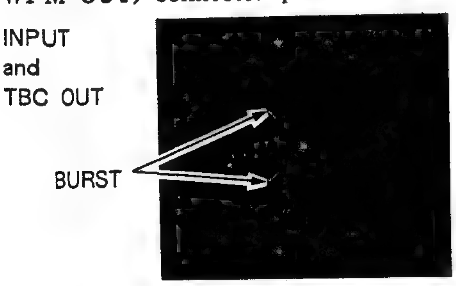
14-15. PAL NORMAL WRITE ZERO ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Waveform monitor Vectorscope Oscilloscope
VIDEO IN signal :	PAL COLOR BARS

(1) TBC OUT sync phase adjustment
Although the TBC output signal is output from the WFM OUT connector, the input video signal will be output when the [INPUT] button on the function control panel is pressed and it is output for as long as this button is kept depressed.
Lock the waveform monitor to the external sync signal and pay attention to the phase of the falling edge of the sync signal on the waveform monitor screen. While setting the [INPUT] button to ON and OFF, adjust ⊘SYNC PHASE control RV15/RD-7 so that the phase of the falling edge of the sync signal in the TBC OUT signal and the phase of the input video signal coincide.
WFM OUT/connector panel



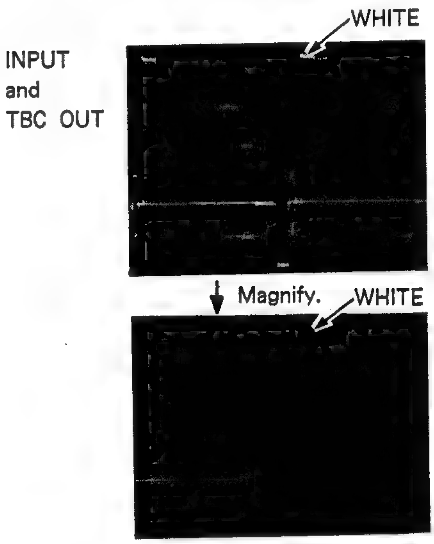
(2) TBC OUT SC phase adjustment
Set the vectorscope to the external ϕ reference mode. While setting the VTR's [INPUT] button to ON and OFF, adjust ⊘SC PHASE control RV17/RD-7 so that the phase of the burst signal in the TBC OUT signal and the phase of the input video signal coincide.
WFM OUT/connector panel



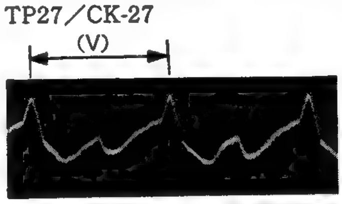
(3) REF CF LED
Adjust ⊘REF CF control RV27/RD-7 so that REF CF LED D2/RD-7 lights.

(4) Video phase adjustment

(4-1) Pay attention to the phase of the leading edge of the WHITE area on the waveform monitor screen. While setting the VTR's [INPUT] button to ON and OFF, adjust ⊘RV40 or RV810/CK-27 so that the leading phase of the WHITE area of the TBC OUT signal and the phase of the input video signal coincide and also so that PB CF LED D10/CK-27 lights.
WFM OUT/connector panel



(4-2) Next, adjust RV40 or RV810 finely.
TP27/CK-27



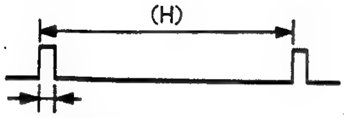
Average level $= -400 \pm 100$mVdc
(CK-27 : suffix-11, 12)
$= -300 \pm 20$mVdc
(CK-27 : suffix-13, 14)
(As a result of this adjustment, the PB CF LED may go off.)

(4-3) Again compare the WHITE leading phase of the TBC OUT signal and the phase of the input video signal on the waveform monitor and if they do not match, repeat the adjustments outlined in steps (4-1) and (4-2).

14-16. BIDIREX WRITE ZERO ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL or SECAM video signal

TP5/CK-27



1.46±0.01 μs
⊘RV12/CK-27

14-17. SECAM/B&W WRITE ZERO ADJUSTMENT

[For CK-27 board suffix -11, -12]

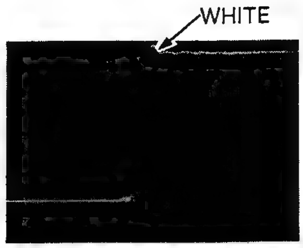
Connection :	See section 14-1.
Menu/switch settings :	See section 14-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Waveform monitor
VIDEO IN signal :	PAL COLOR BARS (burst ON/OFF)

(1) Set menu [S40] as follows :
S40. SERVO REF SELECT : EXT REF

(2) Proceed with the adjustments below while setting to ON and OFF the burst of the color bar signal which is output from the test signal generator.
(Note) : Always keep the PAL video signal with burst supplied to the REF VIDEO IN connector on the VTR.
Pay attention to the WHITE leading phase on the waveform monitor screen. Adjust ⊘RV5/CK-27 so that the WHITE leading phase produced when the burst is OFF coincides with the phase which is produced when the burst is ON.

WFM OUT/connector panel

BURST : ON



BURST : OFF

(3) Set the burst of the signal which is output from the test signal generator to ON.
Set menu [S40] to INPUT.

[For CK-27 board suffix -13, -14~]

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Waveform monitor
VIDEO IN signal :	SECAM COLOR BARS

(1) Set menu [S89] as follows :
S89 TV STANDARD : SECAM

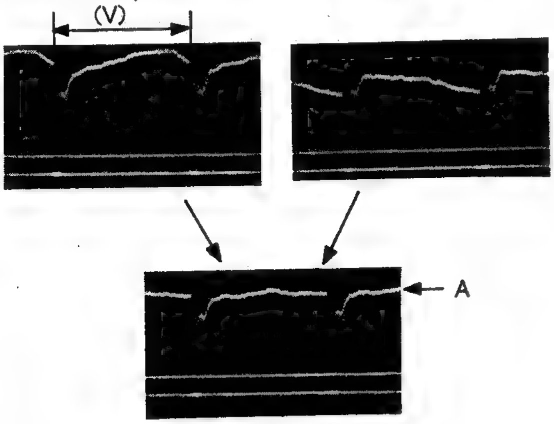
(2) PAY attention to the phase of the leading edge of the WHITE area on the waveform monitor screen. WHITE setting the VTR'S [INPUT] buttun to ON and OFF, adjust ⊘RV800/CK-27 so that the leading phase of the WHITE area of the TBC OUT signal and the phase of the input video signal coincide.

14-18. PAL TAPE SCH ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL video signal

(1) Confirm that the SC-H phase of the input signal to the VTR is 0±5°. See section 14-1.

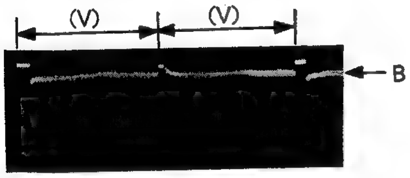
(2) TP29/CK-27



Level : A=1.2±0.1Vdc ⊘RV41/CK-27
Waveform : Flat as possible ⊘RV14/CK-27
Adjust RV41 and RV14 repeatedly.

(3) TP32/CK-27 : 1.2±0.1Vdc
or Pin 7/IC301/Piggy back board CP-125 on early CK-27
⊘RV42/CK-27

(4) TP30/CK-27



B=3.0±0.1Vdc (CK-27 ; suffix -11, -12)
=2.75±0.1Vdc (CK-27 ; suffix -13, -14)
⊘RV15/CK-27

[CAUTION]
If the software used in the SV, SY, and RD boards is version 1, you cannot proceed to the next step. Confirm that the software is version 2 or higher then proceed to the next step. The software version No. is indicated on the IC label as shown below.

Board	Ref. No.	Version 1	Version 2
SV-90	ICN5	V0U1-*-*	V0U2-*-*
	ICN3	V1U1-*-*	V1U2-*-*
	ICE15	V2U1-*-*	V2U2-*-*
SY-103	ICH12	Y0A1-*-*	Y0U2-*-*
	ICH11	Y1A1-*-*	Y1U2-*-*
RD-6	ICL15	RDP1-*-*	RDU2-*-*

(5) Select [TTP ADJ] from the [T17. MAINTENANCE] test menu. Refer to section 3-3.
Key in [C], [6] and press the [0] key while pressing the [SET] key, then press the [SET] key. [C6A. TAPE SCH DATA] will be selected, and the following display will appear on the control panel.

>C6A	> TAPE SCH DATA
00**	>_

Read the [**] part of the display.

For a CK-27 board with suffix -11 or -12, remove the extension board and directly insert the CK-27 board, read off the value of [**] on the display and check the difference between this value and the value obtained when the extension board was used. Extend the CK-27 board using the extension board, then adjust ⊘RV41/CK-27 so that when the CK-27 board is directly inserted without using the extension board the value of [**] becomes one of 7F, 80, or 81.

For a CK-27 board with suffix -13 or higher, perform adjustment without using an extension board. Adujust ⊘RV41/CK-27 so that the value on the [**] part of hte display becomes one of 7F, 80, and 81.

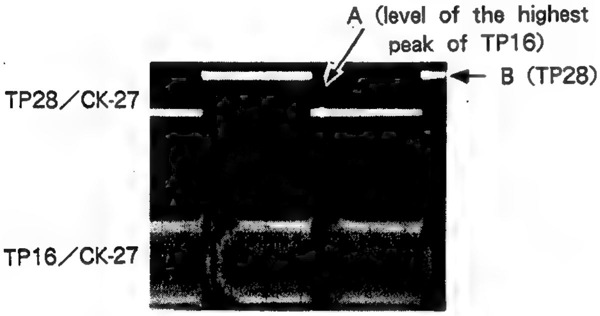
After adjustment, press the blue [IN] key while pressing the blue [OUT] key, then press the [SET] key while pressing the blue [OUT] key.

14-19. SECAM DR/DB DETECTION ADJUSTMENT

Connection : See section 14-1.
Menu/switch settings : See section 14-1 and text.
Mode of VTR : STOP (EE)
Instrument : Oscilloscope
Picture monitor
VIDEO IN signal : SECAM video signal

(1) Set menu [S88] as follows :
S88. PB CF DET MODE : LOC ADJ

(2)



A : Reduce this as much as possible.
⊘PB CF control RV9/CK-27
B=1.1±0.01Vdc
⊘RV13/CK-27

(3) Check that the colors on the picture monitor screen are not reversed when the CHROMA SEQUENCE control on the test signal generator is set from NOR to REV and vice versa. If the colors are reversed, reduce the level of B (TP28, ⊘RV13/CK-27) in step (2).

(4) Return menu [S88] to PRESET.

14-20. A/D OFFSET/GAIN ADJUSTMENT

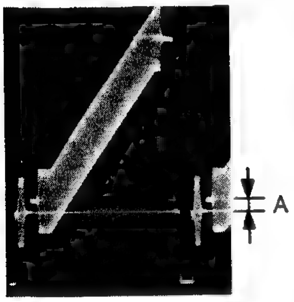
Connection :	See section 14-1.
Menu/switch settings :	See section 14-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Digital voltmeter Waveform monitor Oscilloscope
VIDEO IN signal :	PAL or SECAM video signal

(1) Change the menu settings as shown below.
T06. PR TEST 2 : ON
S82. WHITE REFERENCE : ON
I80. BLANKING LINE : CHANGE
LINE NO.10, 323 : PASS
LINE NO.11, 324 : PASS
LINE NO.12, 325 : PASS
LINE NO.13, 326 : PASS
LINE NO.14, 327 : PASS
LINE NO.15, 328 : PASS

(2) A/D converter reference voltage adjustment
TP20/CK-27 : −2.00±0.01Vdc
(using digital voltmeter)
RV4/CK-27

(3) OFFSET adjustment

WFM OUT/connector panel



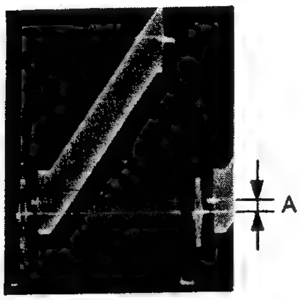
A=0±10mV
RV3/CK-27
RV3 must be readjusted in step 6.

(4) A/D converter operating point adjustment
TP18/CK-27 : 0±1Vdc
RV2/CK-27

(5) Set test menu [T06. PR TEST 2] to "OFF", then switch the power OFF. Remove the extension board, directly insert CK-27 board, and switch the power ON again.
Set menu [T06. PR TEST 2] to "ON".

(6) Adjust OFFSET once again.

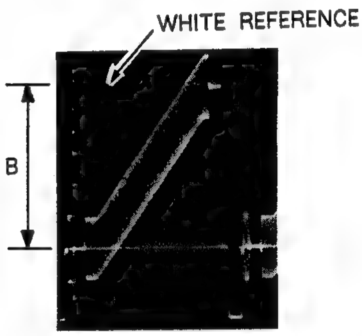
WFM OUT/connector panel



A=0±10mV
RV3/CK-27

(7) Leaving CK-27 board inserted, adjust GAIN.

WFM OUT/connector panel



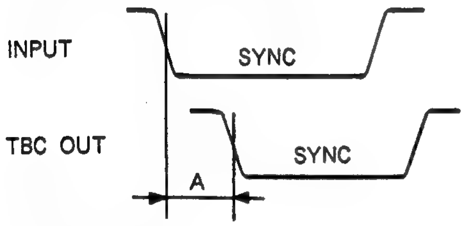
B=700±7mV
RV1/CK-27

(8) Return the menus to their initial settings.
I80. BLANKING LINE : CHANGE
LINE NO.10, 323 : BLANKED
LINE NO.11, 324 : BLANKED
LINE NO.12, 325 : BLANKED
LINE NO.13, 326 : BLANKED
LINE NO.14, 327 : BLANKED
LINE NO.15, 328 : BLANKED
S82. WHITE REFERENCE : OFF
T06. PR TEST 2 : OFF

14-21. SYNC PHASE PRESET ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Waveform monitor
VIDEO IN signal :	PAL or SECAM video signal

Although the TBC output signal is output from the WFM OUT connector, the input video signal will be output when the [INPUT] button on the function control panel is pressed and it is output for as long as this button is kept depressed.
Lock the waveform monitor to the external sync signal and while setting the [INPUT] button to ON and OFF, pay attention to the falling edge phase of the sync signal on the waveform monitor screen.
Rotate SYNC PHASE control RV15/RD-7 clockwise as far as it will go and adjust as follows.
WFM OUT/connector panel

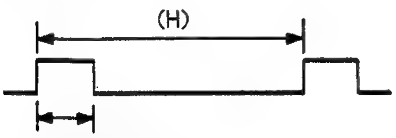


A=1.60±0.1 μs
⊘RV16/RD-7

14-22. PAL H BLANKING PULSE WIDTH ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL video signal

CN A-22a/RD-7



11.6±0.1 μs
⊘RV20/RD-7

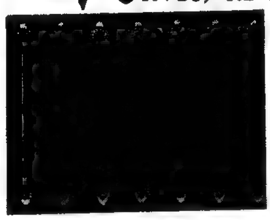
14-23. REF PAL H ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL video signal

TP23/RD-7
(Trig : from TP33/RD-7, +slope)

Magnify a burst.

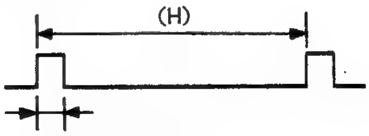
Minimize jitter.
⊘RV28/RD-7



14-24. SECAM H BLANKING PULSE WIDTH ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	SECAM video signal

CN A-22a/RD-7



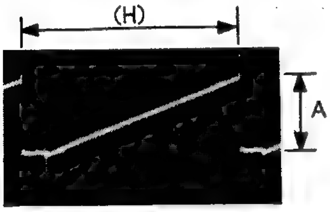
5.6±0.1 μs
⊘RV19/RD-7

14-25. PAL SC PHASE SHIFTER ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL video signal

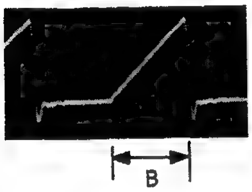
(1) Remove the CK-27 board.

(2) Extend the RD-7 board using the extension board, short circuit between GND and CN A-14b on the extension board, then adjust as shown below.
TP32/RD-7



Minimize A.
⊘RV21/RD-7
Note : RV21 must be adjusted finally at section 14-35 velocity error offset adjustment.

TP25/RD-7



B = 120±5ns
⊘RV26/RD-7

(3) Open the short circuit between GND and CN A-14b on the extension board.
Return the CK-27 board to its home position.

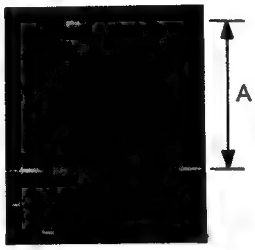
14-26. BIDIREX VIDEO GAIN ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1 and text.
Mode of VTR :	REC → PLAY, VAR +1
Instrument :	Waveform monitor
VIDEO IN signal :	PAL or SECAM COLOR BARS

(1) Record a color bar signal.

(2) Using PLAY/IN key, select the PLAY (DT) head.

(3) Play back the recorded portion in the PLAY mode and in the VAR +1 mode.
WFM OUT/connector panel



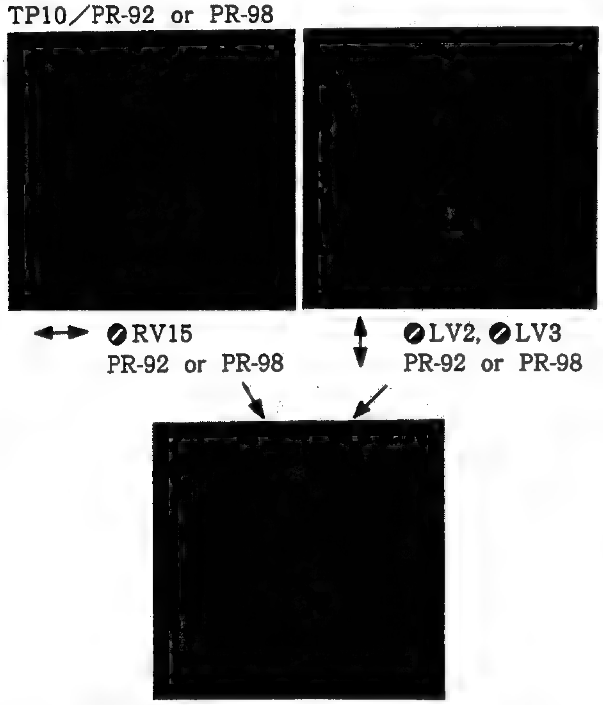
A in VAR +1 = A in normal PLAY
⊘RV4/PR-92, PR-98

14-27. PAL U/V SEPARATION ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Vectorscope
VIDEO IN signal :	PAL COLOR BARS

(1) Connect the vectorscope to TP10/PR-92 or PR-98 through the oscilloscope.

(2) Align the U and V spots in a straight line on the vectorscope screen and superimpose them over each other.
TP10/PR-92 or PR-98



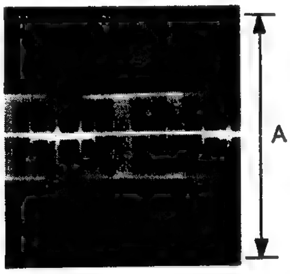
Note : If the spots are not aligned in a straight line but form a curve, proceed with the adjustments below and then adjust as above.
14-35. Velocity error offset adjustment
14-36. Velocity error gain adjustment

14-28. PAL DECODED CHROMA ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1 and text.
Mode of VTR :	STOP(EE)→ REC → VAR +1
Instrument :	Oscilloscope
VIDEO IN signal :	PAL HALF-RED COLOR BARS

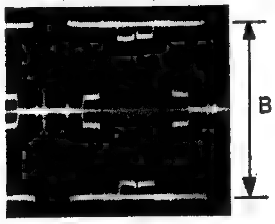
(1) Set ⊘RV26/PR-92 or PR-98 to its mechanical center.
Note : RV26 must be adjusted finally at section 14-30 PAL chroma gain adjustment.

(2) Adjust as shown below in the STOP (EE) mode.
TP10/PR-92, PR-98



A=0.7±0.01V
⊘RV13/PR-92, PR-98

(3) Record a PAL half-red color bar signal.
(4) Using PLAY/IN key, select the PLAY (DT) head.
(5) Adjust as shown below while playing back the recorded portion in the VAR +1 mode.
TP11/PR-92, PR-98



Maximize B.
⊘RV14/PR-92, PR-98

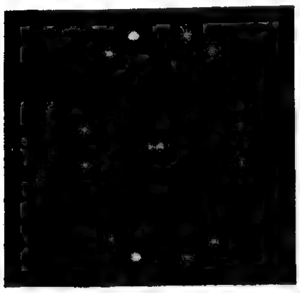
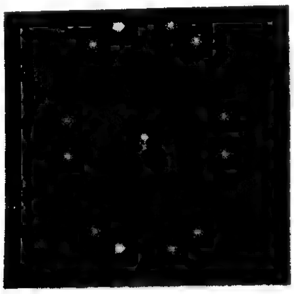
14-29. PAL ENCODED CHROMA ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1 and text.
Mode of VTR :	REC → DT STILL → PLAY
Instrument :	Vectorscope
VIDEO IN signal :	PAL (HALF-RED) COLOR BARS

(1) Record a PAL (half-red) color bar signal.

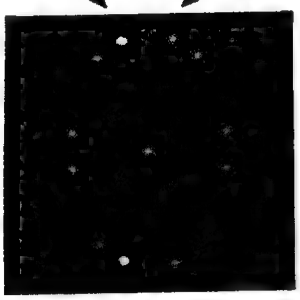
(2) Using [PLAY/IN] key, select the PALY (DT) head.

(3) Offset adjustment
Play back the recorded portion in the DT STILL mode. Adjust RV20 and RV17 so that the center of the vector waveform is located on the center of the vectorscope screen.
WFM OUT/connector panel

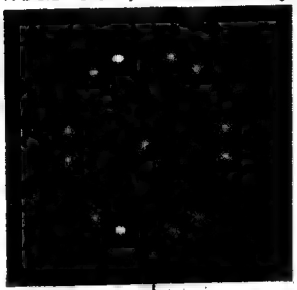
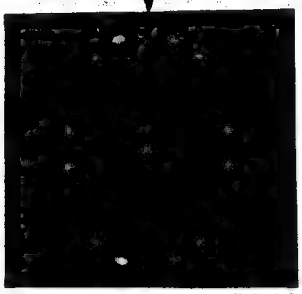



↔ U AXIS
⊘RV20
PR-92 or PR-98

↕ V AXIS
⊘RV17
PR-92 or PR-98



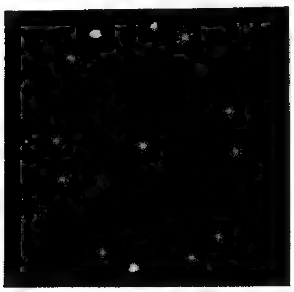
(4) Gain adjustment
Play back the recorded portion in the DT STILL mode. Adjust the gain and phase of the vectorscope so that the yellow spot is located in the center of its target on the vectorscope screen.
Then, adjust RV16 so that every spot is located in the center of its target on the vectorscope screen.
WFM OUT/connector panel

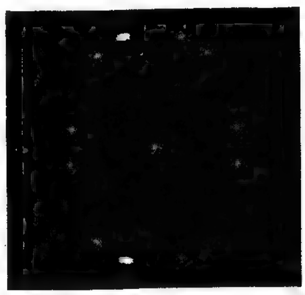
⊘RV16/PR-92 or PR-98

(5) Level and phase adjustment
Play back the recorded portion in the normal PLAY mode and then in the DT STILL mode. Adjust the chroma level and phase in the DT STILL mode as shown below.

WFM OUT/connector panel
DT STILL mode



normal PLAY mode



Level in DT STILL=Level in normal PLAY
⊘RV18/PR-92 or PR-98
Phase in DT STILL=Phase in normal PLAY
⊘RV19/PR-92 or PR-98

14-30. PAL CHROMA D/A GAIN ADJUSTMENT

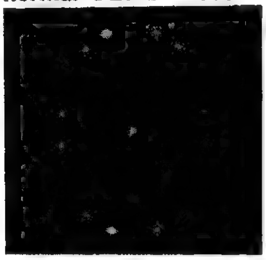
Connection : See section 14-1.
Menu/switch settings : See section 14-1 and text.
Mode of VTR : REC → PLAY → DT STILL
Instrument : Vectorscope
VIDEO IN signal : PAL (HALF-RED) COLOR BARS

(1) Record a PAL (half-red) color bar signal.
(2) Set the menu, switch and control as follows.
Menu I84. VIDEO LEVEL : LOCAL
PB head (PLAY/IN key) : PLAY
VIDEO GAIN control RV24/PR-92 or PR-98 : Counterclockwise fully
(3) Play back the recorded portion in the normal PLAY mode and in the DT STILL mode. Adjust the chroma level in the DT STILL mode as shown below.

WFM OUT/connector panel

DT STILL mode

normal PLAY mode



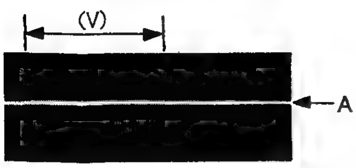
Level in DT STILL=Level in normal PLAY
⊘RV26/PR-92 or PR-98

(4) Set menu I84 to REMOTE.

14-31. PAL DECODER PLL ADJUSTMENT

Connection : See section 14-1.
Menu/switch settings : See section 14-1 and text.
Mode of VTR : REC → STILL
Instrument : Oscilloscope
VIDEO IN signal : PAL video signal

(1) Using PLAY/IN key, select the R/P head.
(2) Record a PAL video signal. While playing back the recorded portion in the STILL mode, adjust as shown below.
TP15/PR-92, PR-98

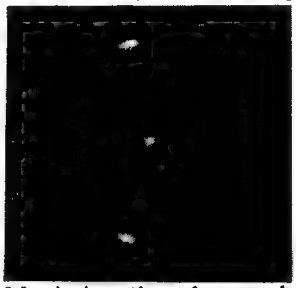


A=−1±0.1Vdc
⊘LV4/PR-92, PR-98
⊘LV5/PR-92, PR-98

14-32. PAL SLOW BIDIREX DECODER AXIS ADJUSTMENT

Connection : See section 14-1.
Menu/switch settings : See section 14-1 and text.
Mode of VTR : REC → SHUTTLE +4
Instrument : Vectorscope
VIDEO IN signal : PAL COLOR BARS

(1) Using PLAY/IN key, select the R/P head.
(2) Record a PAL color bar signal. While playing back the recorded portion in the SHUTTLE +4 mode, adjust as shown below.
WFM OUT/connector panel

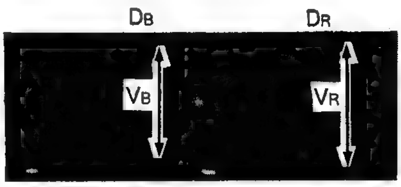


Maximize the chroma level.
⊘RV21/PR-92, PR-98

14-33. SECAM V ID SIGNAL ADJUSTMENT

Connection : See section 14-1.
Menu/switch settings : See section 14-1.
Mode of VTR : STOP (EE)
Instrument : Waveform monitor
VIDEO IN signal : SECAM video signal

WFM OUT/connector panel



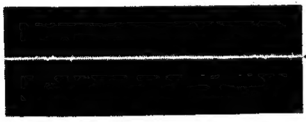
V_B=500±50mV
V_R=500+40/−50mV
⊘RV28/PR-92, PR-98

14-34. PAL DP VIDEO ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Oscilloscope
VIDEO IN signal :	PAL LINEARITY

<u>(A) for PR-92 board with suffix -11 and -12</u>

(A-1) Rotate ⊘RV2 (DP control) /PR-92 so that the waveform at TP21 is as shown below, then adjust the DC voltage.
TP21/PR-92 (-11, -12)



←A

A = 0±50mVdc
⊘RV27/PR-92 (-11, -12)

(A-2) Rotate ⊘RV2 fully clockwise and adjust the pedestal voltage.
TP21/PR-92 (-11, -12)

←B

B = 0±50mVdc
⊘RV1/PR-92 (-11, -12)

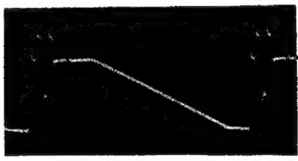
(A-3) Rotate ⊘RV2 until the waveform at TP21 is as shown below.
TP21/PR-92 (-11, -12)

<u>(B) for PR-92 board with suffix -13 or higher and PR-98 board</u>

(B-1) Adjust ⊘RV1/PR-92 or PR-98 so that when ⊘RV2 (DP control) /PR-92 or PR-98 is rotated fully counterclockwise and when rotated fully clockwise, the DC voltages at TP21/PR-92 or PR-98 both fall within the specifications. Repeat adjustment until both voltages fall within the specifications.
TP21/PR-92 (-13 and higher), PR-98
⊘RV1/PR-92 (-13 and higher), PR-98
RV2 : FULLY CLOCKWISE

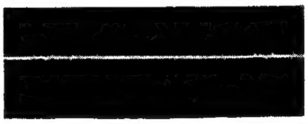
←SPEC : 0±50mVdc

RV2 : FULLY COUNTERCLOCKWISE



←SPEC : 0±50mVdc

(B-2) Rotate ⊘RV2 until the waveform at TP21 is as shown below.
TP21/PR-92 (-13 and higher), PR-98

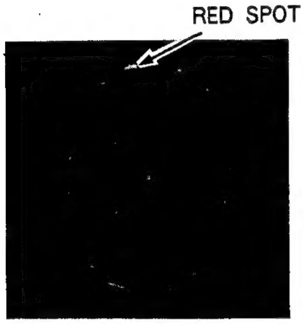


14-35. VELOCITY ERROR OFFSET ADJUSTMENT

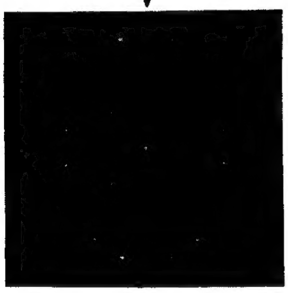
Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	STOP (EE)
Instrument :	Vectorscope
VIDEO IN signal :	PAL HALF-RED COLOR BARS

Note : When performing adjustment, do not extend RD-7 board using an extension board. Leave it inserted.

WFM OUT/connector panel



↓



Adjust so that the size of the phase direction of red spot becomes minimum.
⊘RV21/RD-7

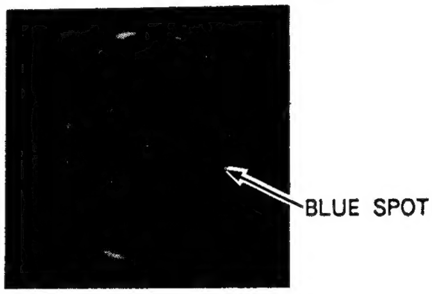
14-36. VELOCITY ERROR GAIN ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1.
Mode of VTR :	REC → PLAY
Instrument :	Vectorscope
VIDEO IN signal :	PAL HALF-RED COLOR BARS

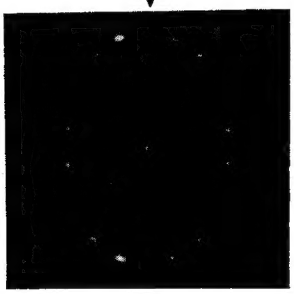
Record a PAL half-red color bar signal and adjust while playing back the recorded portion.

Note : When performing adjustment, do not extend RD-7 board using an extension board. Leave it inserted.

WFM OUT/connector panel



↓



Adjust so that the size of the phase direction of blue spot in minimum.
⊘RV22/RD-7

14-37. PAL BURST/CHROMA PHASE ADJUSTMENT

Connection :	See section 14-1.
Menu/switch settings :	See section 14-1 and text.
Mode of VTR :	REC → PLAY → DT STILL → STOP (EE)
Instrument :	Vectorscope
VIDEO IN signal :	PAL (HALF-RED) COLOR BARS

(1) Record a PAL (half-red) color bar signal.
(2) Using [PLAY/IN] key, select the PLAY (DT) head.
(3) While playing back the recorded portion in the normal PLAY mode and in the STILL mode, adjust the phase relation between burst and chroma on the vectorscope screen.
WFM OUT/connector panel
BURST/CHROMA phase :
in normal PLAY mode=in DT STILL mode
⊘RV25/RD-7

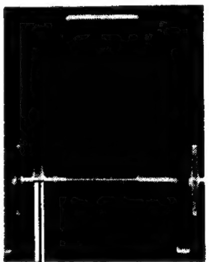
(4) Set the machine to the STOP (EE) mode. While altering the INPUT button on the function control panel, adjust the phase relation between burst and chroma.
WFM OUT/connector panel
BURST/CHROMA phase :
TBC OUT=INPUT
⊘RV24/RD-7

14-38. Y/C DELAY ADJUSTMENT

[CAUTION]
The Y/C delay time can be adjusted finely using S1 and S2 DIP switch settings. Normally, however, there is no need to change the settings that were made when the unit was originally shipped from the manufacturing plant. When the settings have been chenged, the following items must be re-adjusted.
14-4. PAL BURST LEVEL ADJUSTMENT
14-6. TBC OUT FREQUENCY RESPONSE ADJUSTMENT

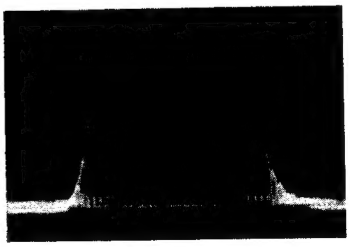
Connection :	See section 14-1.
Menu/switch settings :	See section 14-1 and text.
Mode of VTR :	STOP (EE)
Instrument :	Waveform monitor
VIDEO IN signal :	PAL MOD 20T PULSE

(1) Set menu [I83] as follows :
I83. CHROMA LEVEL : LOCAL
(2) Magnify the 20T pulse section on the waveform monitor and then select the ON channel of the S1 and S2 DIP switches so that the envelope at the bottom of the 20T pulse is made symmetrical at the left and right.
This adjustment is facilitated by using CHROMA level control RV23/PR-92 or PR-98 to set the chroma to the appropriate level.
WFM OUT/connector panel

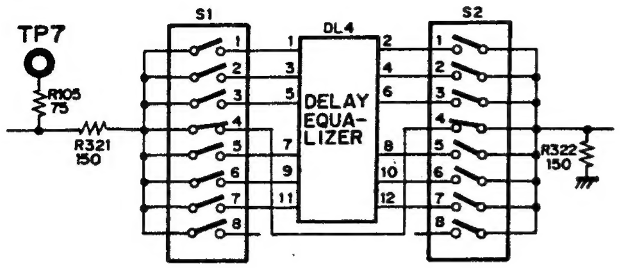


Magnify.

⊘S1, ⊘S2
PR-92 or PR-98



Set only one pair of any channel from 1 through 7 of the S1 and S2 DIP switches to ON and set all the other pairs to OFF.



The amount of delay produced by the delay equalizer in the above figure is shown in the table below. A positive value indicates that the Y signal is delayed from the chroma signal; conversely, a negative value signifies that the Y signal precedes the chroma signal.

SWITCH ON		Relative delay time
S1	S2	
1	1	+21 nsec
2	2	+14
3	3	+7
4	4	0
5	5	−7
6	6	−14
7	7	−21

(3) Set menu [I83] to REMOTE.
(4) Adjust the PAL burst level (⊘ RV11/PR-92, PR-98) referring to section 14-4.
(5) Adjust the TBC OUT frequency response referring to section 14-6.